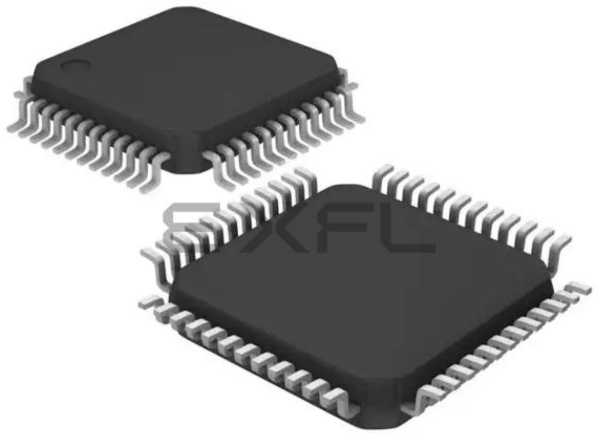
Renesas Electronics America Inc - UPD78F0410GA-GAM-AX Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0410ga-gam-ax

3.4.5 Special function register (SFR) addressing

[Function]

A memory-mapped special function register (SFR) is addressed with 8-bit immediate data in an instruction word. This addressing is applied to the 240-byte spaces FF00H to FFCFH and FFE0H to FFFFH. However, the SFRs mapped at FF00H to FF1FH can be accessed with short direct addressing.

[Operand format]

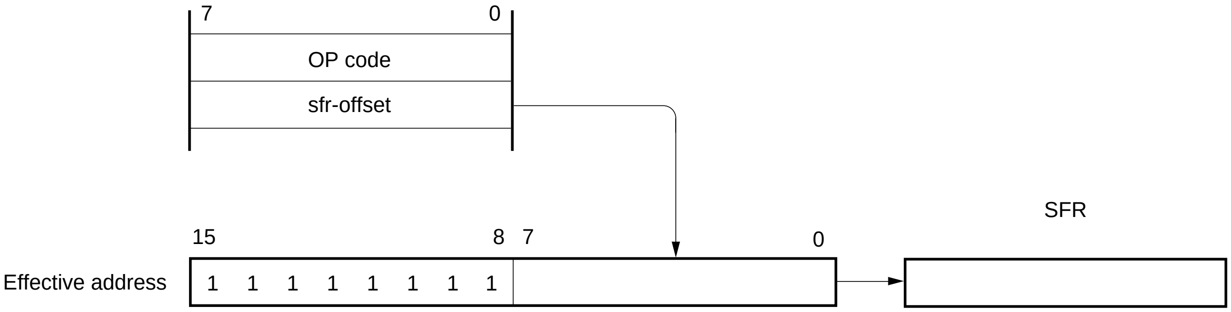
Identifier	Description
sfr	Special function register name
sfrp	16-bit manipulatable special function register name (even address only)

[Description example]

MOV PM0, A; when selecting PM0 (FF20H) as sfr

Operation code	1	1	1	1	0	1	1	0	OP code
	0	0	1	0	0	0	0	0	20H (sfr-offset)

[Illustration]



4.2.5 Port 10

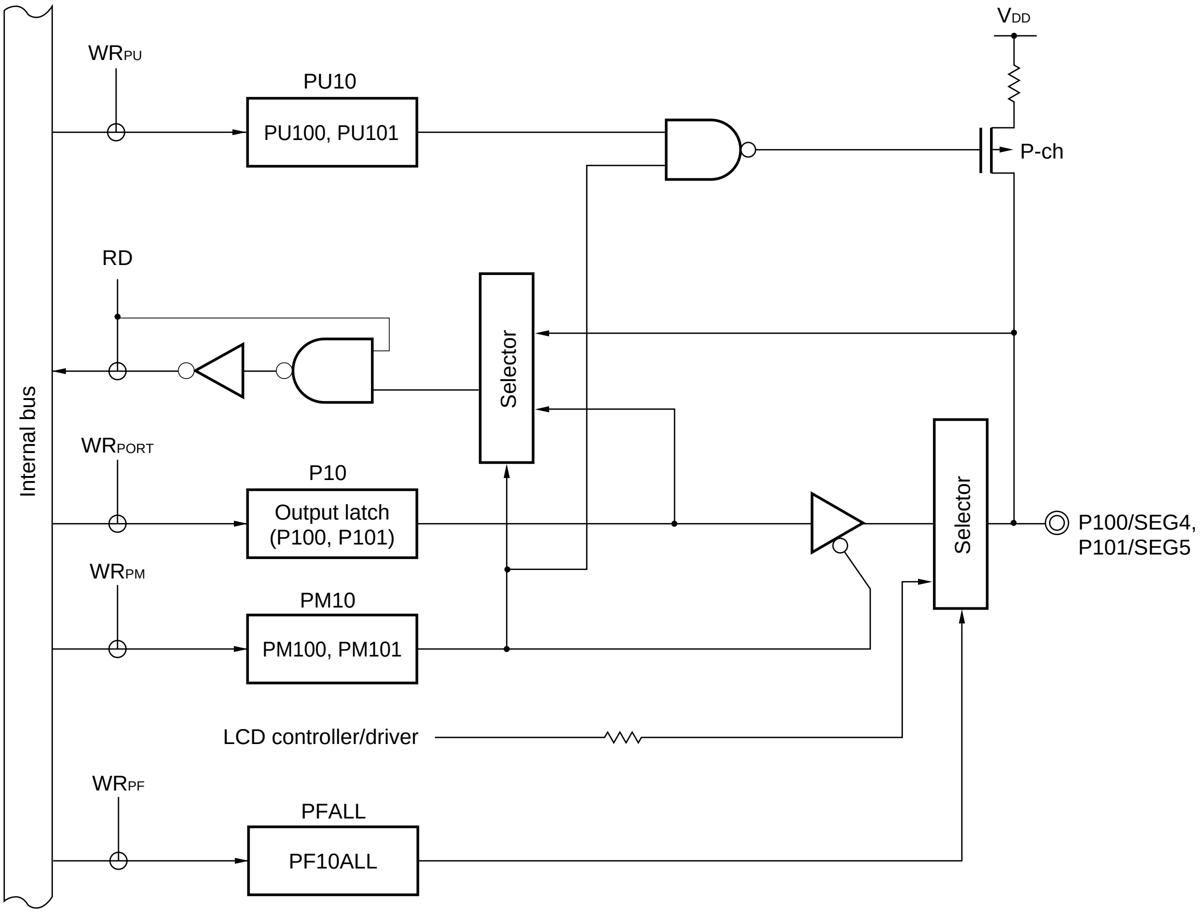
Port 10 is a 2-bit I/O port with an output latch. Port 10 can be set to the input mode or output mode in 1-bit units using port mode register 10 (PM10). When the P100 and P101 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 10 (PU10).

This port can also be used for segment output.

Reset signal generation sets port 10 to input mode.

Figure 4-8 shows a block diagram of port 10.

Figure 4-8. Block Diagram of P100, P101



P10:	Port register 10
PU10:	Pull-up resistor option register 10
PM10:	Port mode register 10
PFALL:	Port function register ALL
RD:	Read signal
WR××:	Write signal

(1) Example of setting procedure when oscillating the XT1 clock

<1> Setting XT1 and XT2 pins and selecting operation mode (PCC and OSCCTL registers)

When OSCSELS is set as any of the following, the mode is switched from port mode to XT1 oscillation mode.

OSCSELS	Operation Mode of Subsystem Clock Pin	P123/XT1 Pin	P124/XT2 Pin
1	XT1 oscillation mode	Crystal/ceramic resonator connection	

<2> Waiting for the stabilization of the subsystem clock oscillation

Wait for the oscillation stabilization time of the subsystem clock by software, using a timer function.

Caution Do not change the value of OSCSELS while the subsystem clock is operating.

(2) Example of setting procedure when using the subsystem clock as the CPU clock

<1> Setting subsystem clock oscillation[Note]

(See **5.6.3 (1) Example of setting procedure when oscillating the XT1 clock**)

Note The setting of <1> is not necessary when while the subsystem clock is operating.

<2> Switching the CPU clock (PCC register)

When CSS is set to 1, the subsystem clock is supplied to the CPU.

CSS	PCC2	PCC1	PCC0	CPU Clock (f_{CPU}) Selection
1	0	0	0	$f_{SUB}/2$
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
	Other than above			Setting prohibited

(3) Example of setting procedure when stopping the subsystem clock

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the subsystem clock.

When CLS = 1, the subsystem clock is supplied to the CPU, so change the CPU clock to the internal high-speed oscillation clock or high-speed system clock.

CLS	MCS	CPU Clock Status
0	0	Internal high-speed oscillation clock
0	1	High-speed system clock
1	×	Subsystem clock

<2> Stopping the subsystem clock (OSCCTL register)

When OSCSELS is cleared to 0, XT1 oscillation is stopped.

Cautions 1. Be sure to confirm that CLS = 0 when clearing OSCSELS to 0. In addition, stop the peripheral hardware if it is operating on the subsystem clock.

2. The subsystem clock oscillation cannot be stopped using the STOP instruction.

Table 5-5. CPU Clock Transition and SFR Register Setting Examples (3/4)

(6) CPU clock changing from high-speed system clock (C) to internal high-speed oscillation clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register Status Transition	RSTOP	RSTS	MCM0
(C) → (B)	0	Confirm this flag is 1.	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

(7) CPU clock changing from high-speed system clock (C) to subsystem clock (D)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register Status Transition	OSCSELS	Waiting for Oscillation Stabilization	CSS
(C) → (D)	1	Necessary	1

Unnecessary if the CPU is operating with the subsystem clock

(8) CPU clock changing from subsystem clock (D) to internal high-speed oscillation clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register Status Transition	RSTOP	RSTS	MCM0	CSS
(D) → (B)	0	Confirm this flag is 1.	0	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

↑ Unnecessary if XSEL is 0

Remarks 1. (A) to (I) in Table 5-5 correspond to (A) to (I) in Figure 5-15.

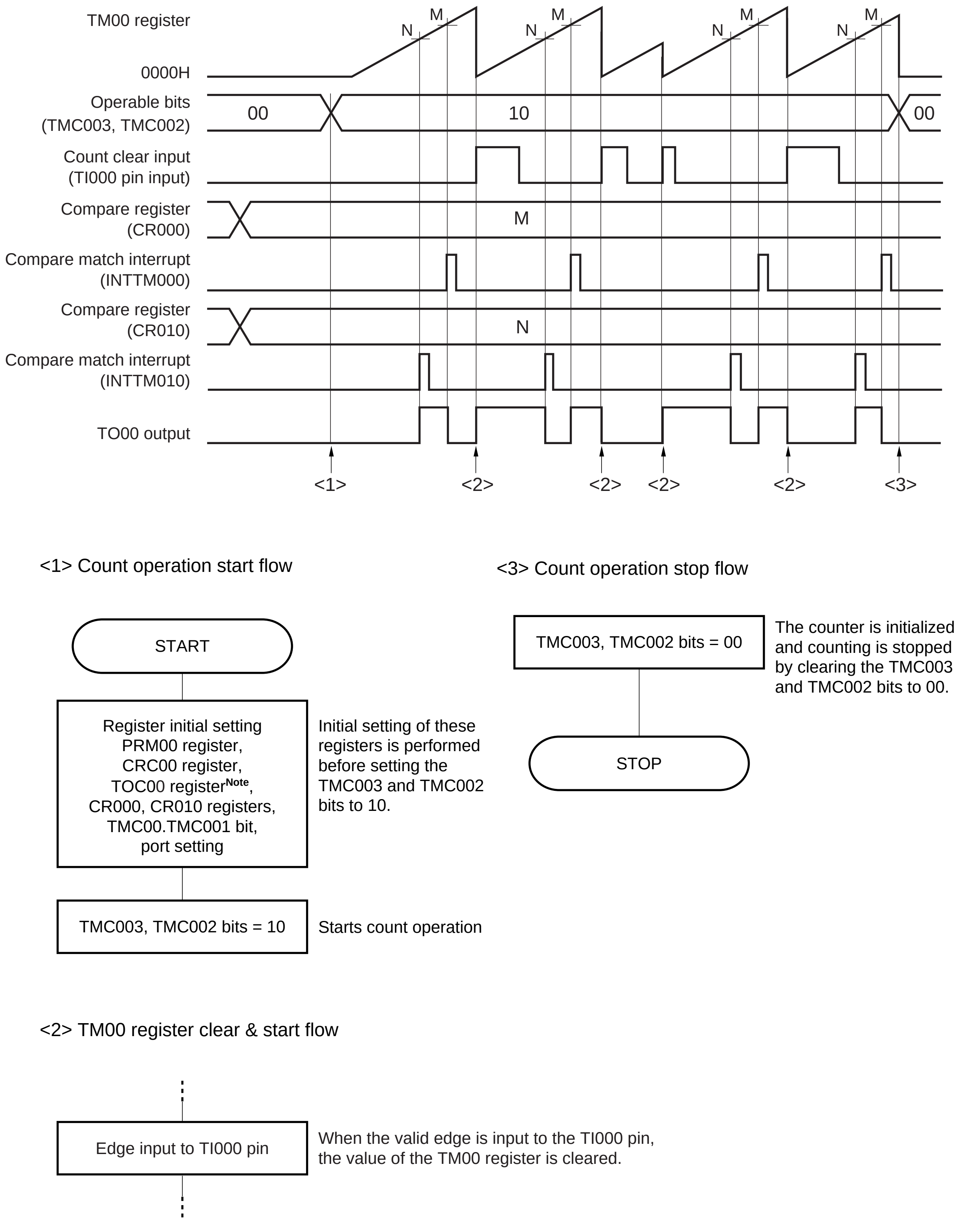
2. MCM0: Bit 0 of the main clock mode register (MCM)

OSCSELS: Bit 4 of the clock operation mode select register (OSCCTL)

RSTS, RSTOP: Bits 7 and 0 of the internal oscillation mode register (RCM)

CSS: Bit 4 of the processor clock control register (PCC)

Figure 6-32. Example of Software Processing in Clear & Start Mode Entered by TI000 Pin Valid Edge Input



<1> Count operation start flow

Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 10.

Starts count operation

<3> Count operation stop flow

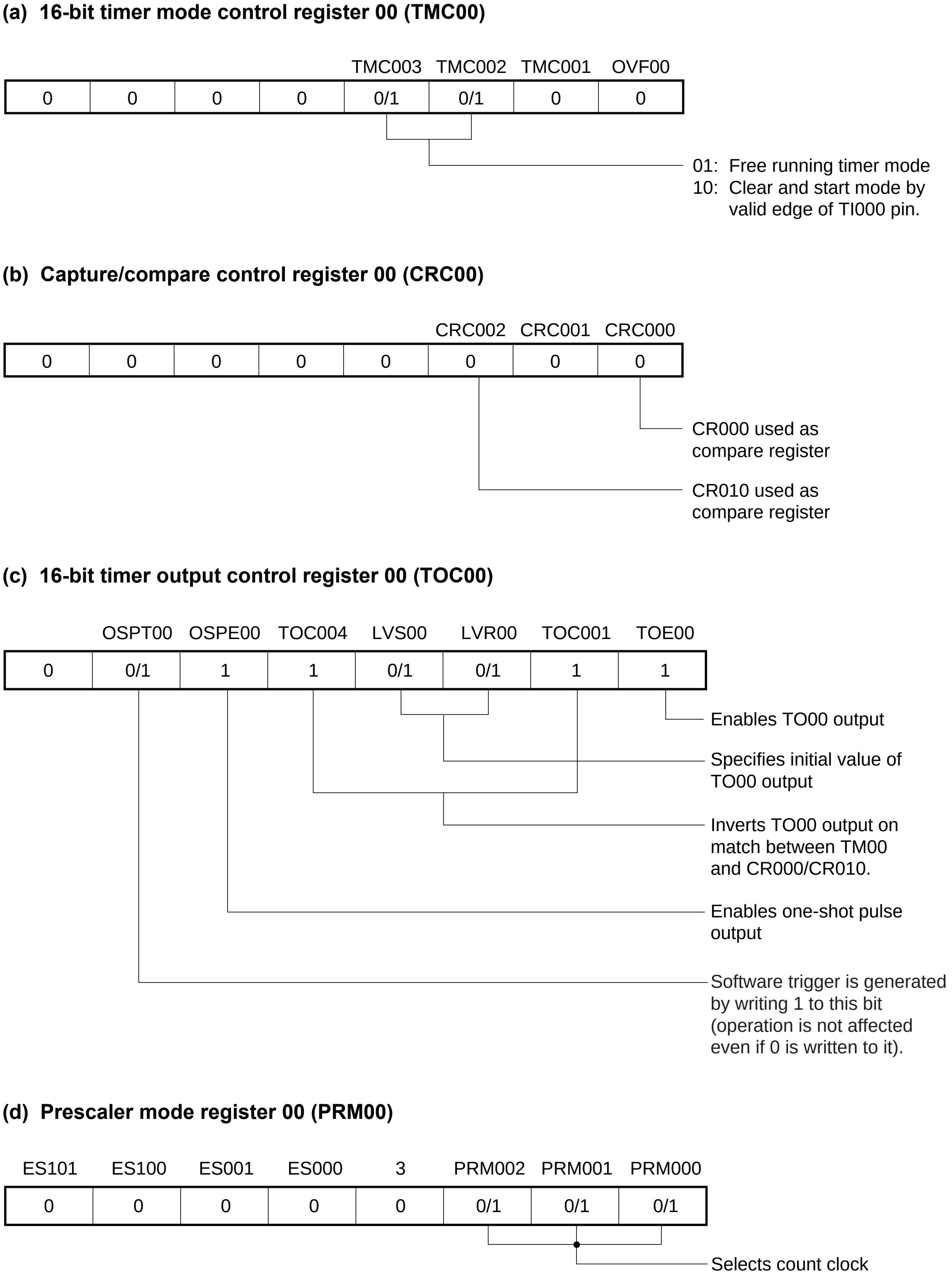
The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

<2> TM00 register clear & start flow

When the valid edge is input to the TI000 pin, the value of the TM00 register is cleared.

Note Care must be exercised when setting TOC00. For details, see **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

Figure 6-45. Example of Register Settings for One-Shot Pulse Output Operation (1/2)



(a) 16-bit timer mode control register 00 (TMC00)

				TMC003	TMC002	TMC001	OVF00
0	0	0	0	0/1	0/1	0	0

TMC003, TMC002:
01: Free running timer mode
10: Clear and start mode by valid edge of TI000 pin.

(b) Capture/compare control register 00 (CRC00)

					CRC002	CRC001	CRC000
0	0	0	0	0	0	0	0

CRC000: CR000 used as compare register

CRC002: CR010 used as compare register

(c) 16-bit timer output control register 00 (TOC00)

	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00
0	0/1	1	1	0/1	0/1	1	1

TOE00: Enables TO00 output

LVS00, LVR00: Specifies initial value of TO00 output

TOC004, TOC001: Inverts TO00 output on match between TM00 and CR000/CR010.

OSPE00: Enables one-shot pulse output

OSPT00: Software trigger is generated by writing 1 to this bit (operation is not affected even if 0 is written to it).

(d) Prescaler mode register 00 (PRM00)

ES101	ES100	ES001	ES000	3	PRM002	PRM001	PRM000
0	0	0	0	0	0/1	0/1	0/1

PRM002, PRM001, PRM000: Selects count clock

Figure 8-1. Block Diagram of 8-Bit Timer H0

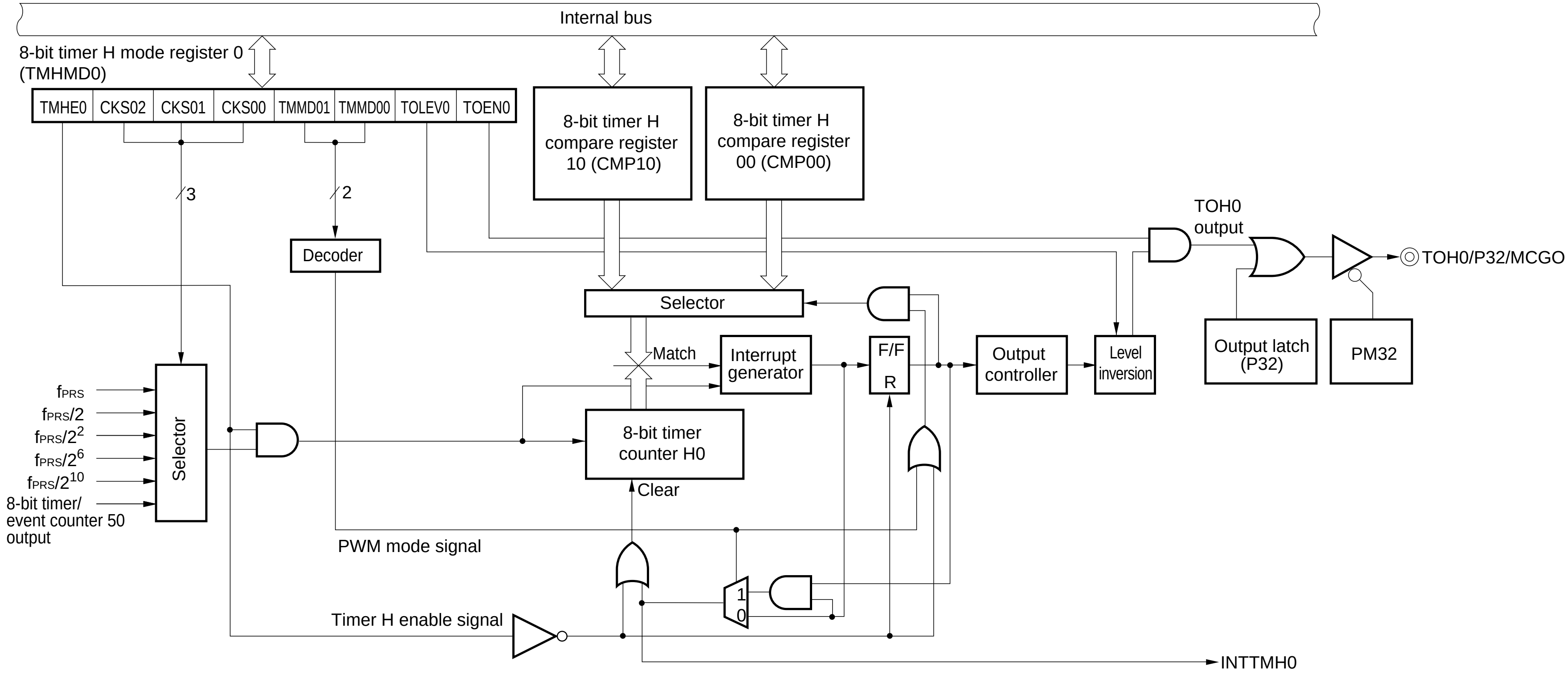


Figure 8-6. Format of 8-Bit Timer H Mode Register 0 (TMHMD0)

Address: FF69H After reset: 00H R/W

	<7>	6	5	4	3	2	<1>	<0>
TMHMD0	TMHE0	CKS02	CKS01	CKS00	TMMD01	TMMD00	TOLEV0	TOEN0

TMHE0	Timer operation enable
0	Stops timer count operation (counter is cleared to 0)
1	Enables timer count operation (count operation started by inputting clock)

CKS02	CKS01	CKS00	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
0	1	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	0	0	$f_{PRS}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz
1	0	1	TM50 output[Note 3]			
Other than above			Setting prohibited			

TMMD01	TMMD00	Timer operation mode
0	0	Interval timer mode
1	0	Input enable width adjust mode for pins (PWM mode)
Other than above		Setting prohibited

TOLEV0	Timer output level control (in default mode)
0	Low level
1	High level

TOEN0	Timer output control
0	Disables output
1	Enables output

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq 10$ MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq 5$ MHz

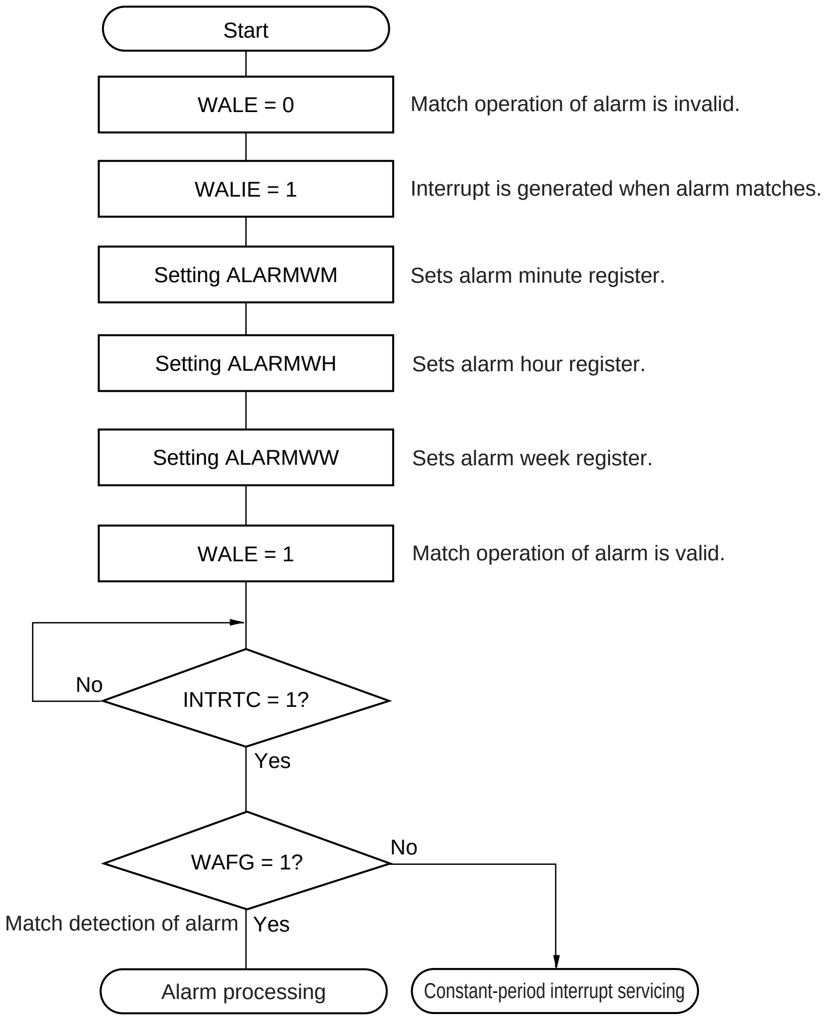
2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V ≤ V_{DD} < 2.7 V, the setting of CKS02 = CKS01 = CKS00 = 0 (count clock: f_{PRS}) is prohibited.

3. When selecting the TM50 output as the count clock, start the operation of the 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).

9.4.3 Setting alarm of real-time counter

Set time of alarm when WALE = 0.

Figure 9-21. Alarm Setting Procedure


Start
WALE = 0
Match operation of alarm is invalid.
WALIE = 1
Interrupt is generated when alarm matches.
Setting ALARMWM
Sets alarm minute register.
Setting ALARMWH
Sets alarm hour register.
Setting ALARMWW
Sets alarm week register.
WALE = 1
Match operation of alarm is valid.
No
INTRTC = 1?
Yes
WAFG = 1?
No
Match detection of alarm
Yes
Alarm processing
Constant-period interrupt servicing

Remarks 1. ALARMWM, ALARMWH, and ALARMWW may be written in any sequence.

2. Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

(7) 8-bit A/D conversion result register (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

Caution When data is read from ADCR and ADCRH, a wait cycle is generated. Do not read data from ADCR and ADCRH when the CPU is operating on the subsystem clock and the peripheral hardware clock is stopped. For details, see CHAPTER 29 CAUTIONS FOR WAIT.

(8) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When A/D conversion has been completed, this controller generates INTAD.

(9) AV_{REF} pin

This pin inputs an analog power/reference voltage to the A/D converter. When using at least one port of port 2 as a digital port or for segment output, set it to the same potential as the V_{DD} pin.

The signal input to ANI0 to ANI5 is converted into a digital signal, based on the voltage applied across AV_{REF} and AV_{SS}.

(10) AV_{SS} pin

This is the ground potential pin of the A/D converter. Always use this pin at the same potential as that of the V_{SS} pin even when the A/D converter is not used.

(11) A/D converter mode register (ADM)

This register is used to set the conversion time of the analog input signal to be converted, and to start or stop the conversion operation.

(12) A/D port configuration register 0 (ADPC0)

This register switches the ANI0/P20 to ANI5/P25 pins to analog input of 10-bit successive approximation type A/D converter or digital I/O of port.

(13) Analog input channel specification register (ADS)

This register is used to specify the port that inputs the analog voltage to be converted into a digital signal.

(14) Port mode register 2 (PM2)

This register switches the ANI0/P20 to ANI5/P25 pins to input or output.

(15) Port function register 2 (PF2)

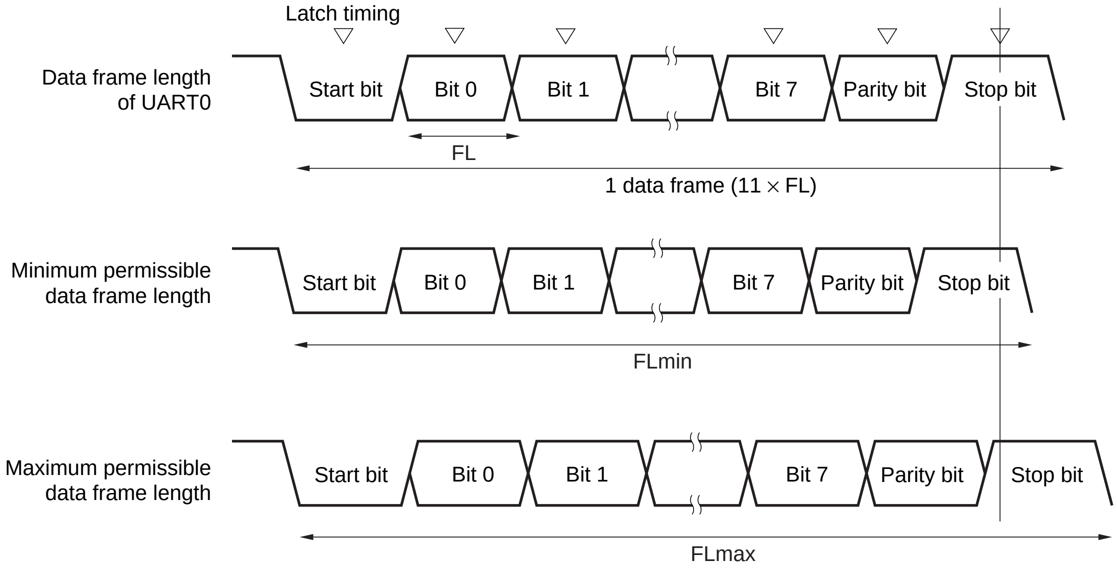
This register switches the ANI0/P20 to ANI5/P25 pins to I/O of port, analog input of A/D converter, or segment output.

(4) Permissible baud rate range during reception

The permissible error from the baud rate at the transmission destination during reception is shown below.

Caution Make sure that the baud rate error during reception is within the permissible error range, by using the calculation expression shown below.

Figure 13-13. Permissible Baud Rate Range During Reception



As shown in Figure 13-13, the latch timing of the receive data is determined by the counter set by baud rate generator control register 0 (BRGC0) after the start bit has been detected. If the last data (stop bit) meets this latch timing, the data can be correctly received.

Assuming that 11-bit data is received, the theoretical values can be calculated as follows.

$FL = (Brate)^{-1}$

Brate: Baud rate of UART0
k: Set value of BRGC0
FL: 1-bit data length
Margin of latch timing: 2 clocks

(i) SBF reception

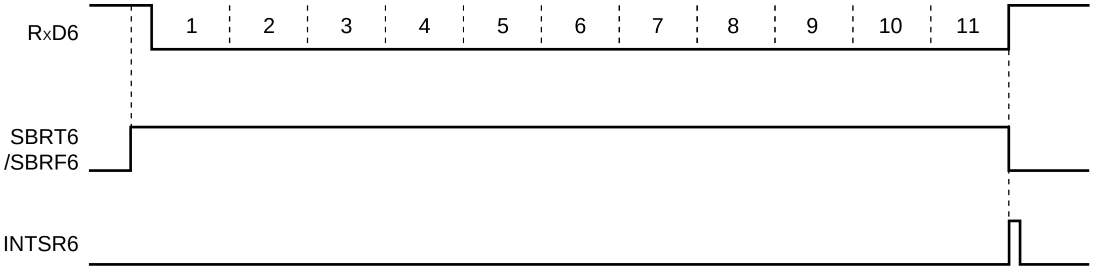
When the device is used in LIN communication operation, the SBF (Synchronous Break Field) reception control function is used for reception. For the reception operation of LIN, see **Figure 14-2 LIN Reception Operation**.

Reception is enabled when bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is set to 1 and then bit 5 (RXE6) of ASIM6 is set to 1. SBF reception is enabled when bit 6 (SBRT6) of asynchronous serial interface control register 6 (ASICL6) is set to 1. In the SBF reception enabled status, the RxD6 pin is sampled and the start bit is detected in the same manner as the normal reception enable status.

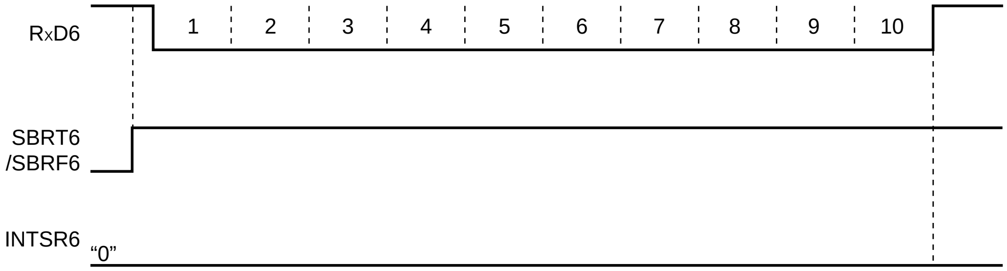
When the start bit has been detected, reception is started, and serial data is sequentially stored in the receive shift register 6 (RXS6) at the set baud rate. When the stop bit is received and if the width of SBF is 11 bits or more, a reception completion interrupt request (INTSR6) is generated as normal processing. At this time, the SBRF6 and SBRT6 bits are automatically cleared, and SBF reception ends. Detection of errors, such as OVE6, PE6, and FE6 (bits 0 to 2 of asynchronous serial interface reception error status register 6 (ASIS6)) is suppressed, and error detection processing of UART communication is not performed. In addition, data transfer between receive shift register 6 (RXS6) and receive buffer register 6 (RXB6) is not performed, and the reset value of FFH is retained. If the width of SBF is 10 bits or less, an interrupt does not occur as error processing after the stop bit has been received, and the SBF reception mode is restored. In this case, the SBRF6 and SBRT6 bits are not cleared.

Figure 14-25. SBF Reception

1. Normal SBF reception (stop bit is detected with a width of more than 10.5 bits)



2. SBF reception error (stop bit is detected with a width of 10.5 bits or less)



Remark	RxD6:	RxD6 pin (input)
	SBRT6:	Bit 6 of asynchronous serial interface control register 6 (ASICL6)
	SBRF6:	Bit 7 of ASICL6
	INTSR6:	Reception completion interrupt request

(4) Port function register 2 (PF2)

This register sets whether to use pins P20 to P25 as port pins (other than segment output pins) or segment output pins.

PF2 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PF2 to 00H.

Figure 15-5. Format of Port Function Register 2

Address: FFB5H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PF2	0	0	PF25	PF24	PF23	PF22	PF21	PF20

PF2n	Port/segment output specification
0	Used as port (other than segment output)
1	Used as segment output

Remark n = 0 to 5

(5) Port function register ALL (PFALL)

This register sets whether to use pins P10, P11, P14 or P15 as port pins (other than segment output pins) or segment output pins.

PFALL is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PFALL to 00H.

Figure 15-6. Format of Port Function Register ALL

Address: FFB6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PFALL	0	PF15ALL	PF14ALL	0	PF11ALL	PF10ALL	0	0

PFnALL	Port/segment output specification
0	Used as port (other than segment output)
1	Used as segment output

Remark n = 10, 11, 14 or 15

Figure 15-18. Three-Time-Slice LCD Drive Waveform Examples (1/2 Bias Method)

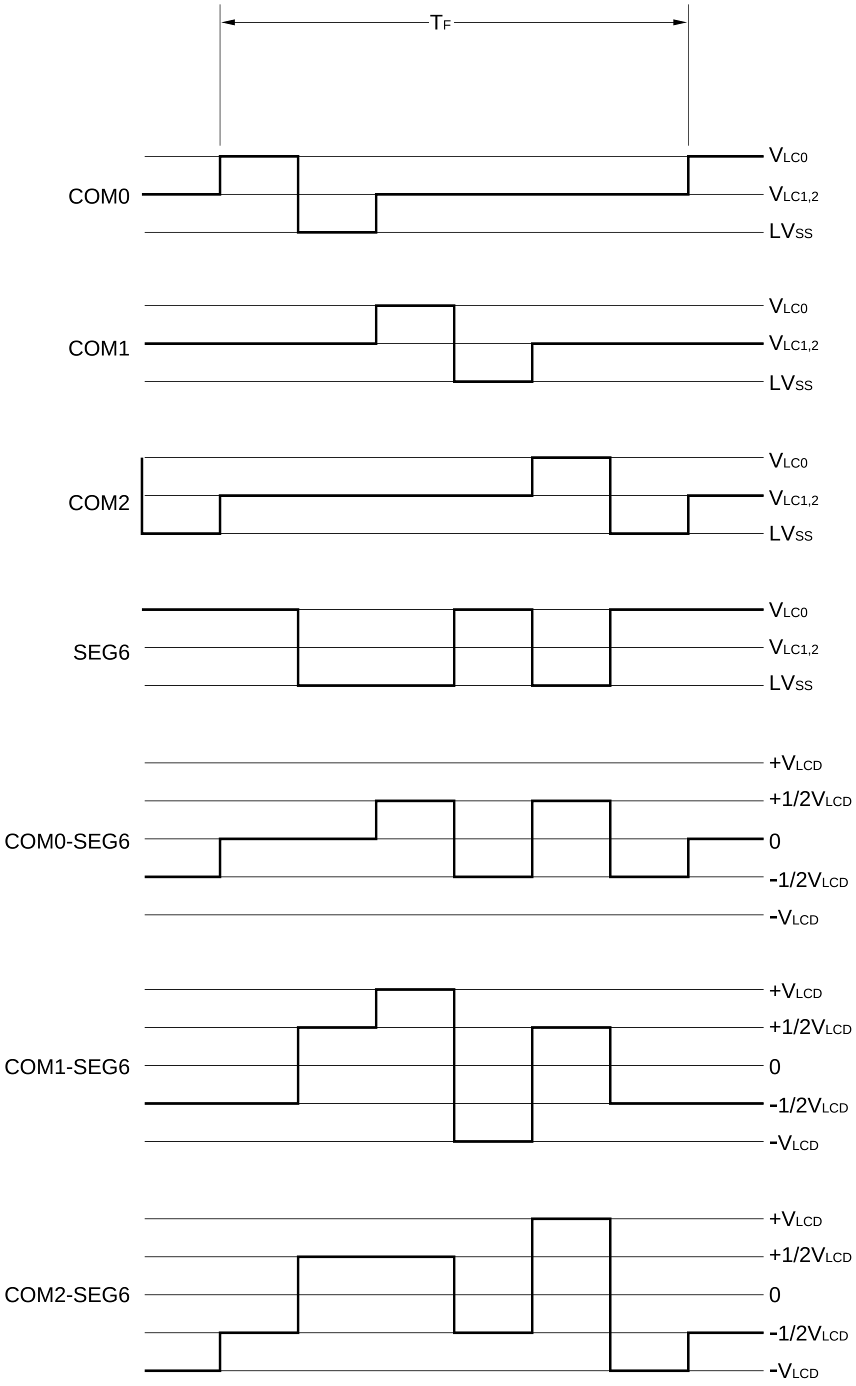
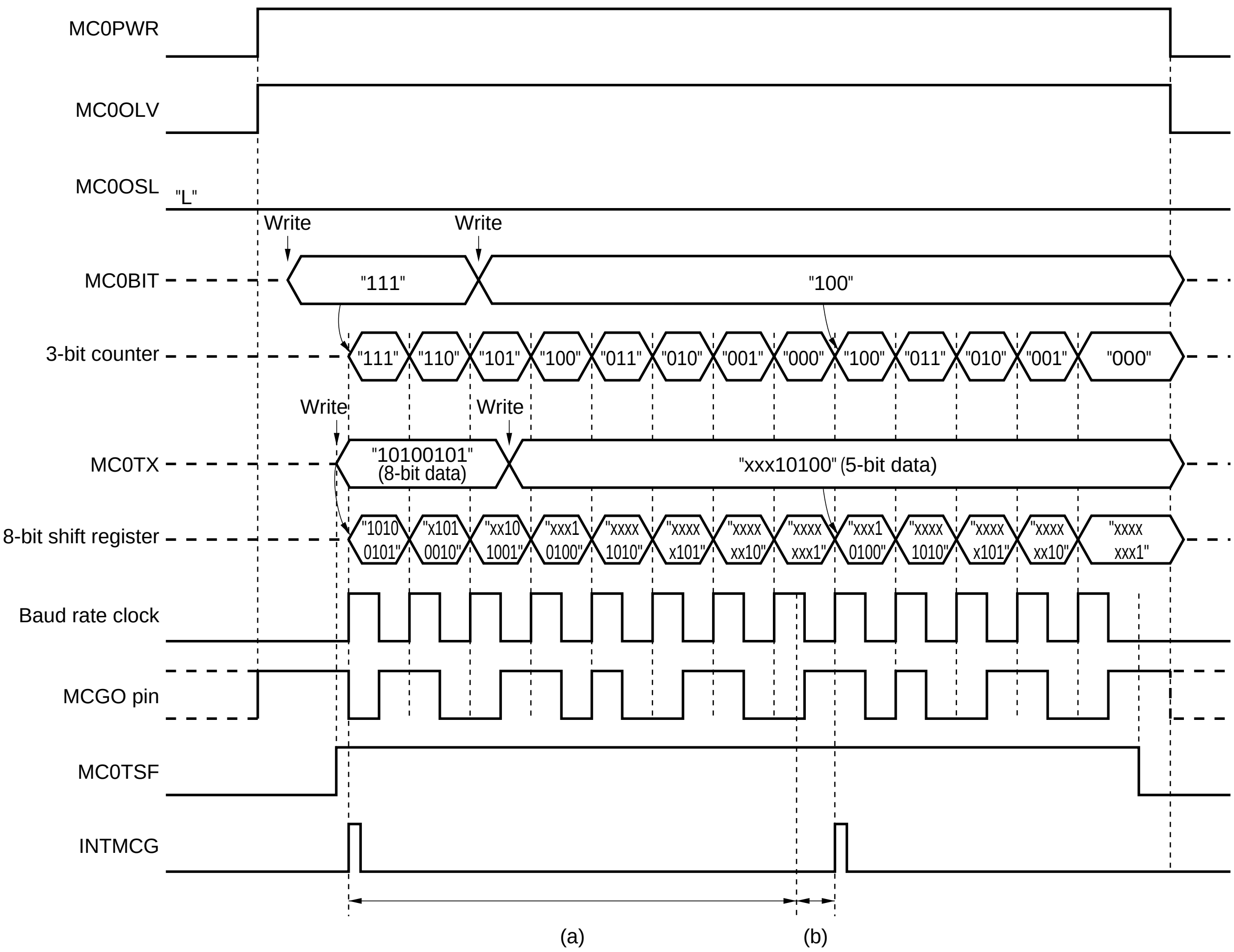


Figure 16-8. Timing of Manchester Code Generator Mode (LSB First) (3/4)

(3) Transmit timing (MC0OLV = 1, total transmit bit length = 13 bits)



(a): “8-bit transfer period” – (b)

(b): “1/2 cycle of baud rate” + 1 clock (fXCLK) before the last bit of transmit data

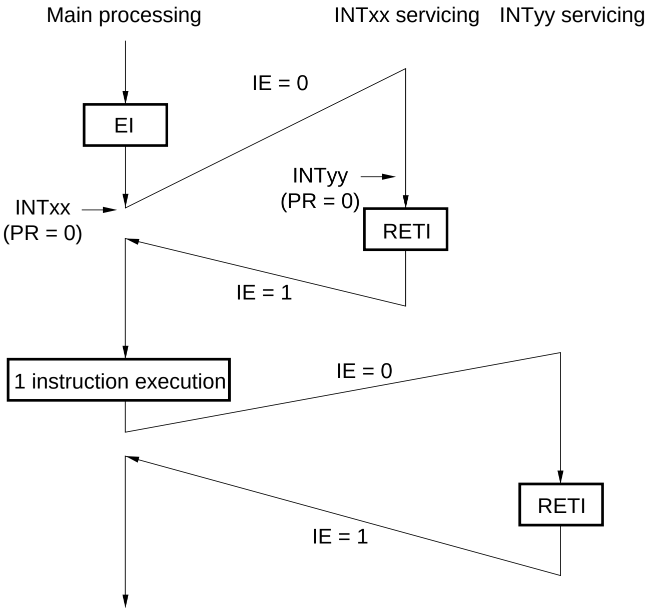
fXCLK: Frequency of the operation base clock selected by using the MC0CKS2 to MC0CKS0 bits of the MC0CTL1 register

Last bit: Transfer bit when 3-bit counter = 000

Caution Writing the next transmit data to MC0TX must be complete within the period (a) during continuous transmission. If writing the next transmit data to MC0TX is executed in the period (b), the next data transmission starts 2 clocks (fXCLK) after the last bit has been transmitted. Rewrite the MC0BIT before writing to MC0TX during continuous transmission.

Figure 17-10. Examples of Multiple Interrupt Servicing (2/2)

Example 3. Multiple interrupt servicing does not occur because interrupts are not enabled



Interrupts are not enabled during servicing of interrupt INTxx (EI instruction is not issued), therefore, interrupt request INTyy is not acknowledged and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 0: Higher priority level
IE = 0: Interrupt request acknowledgment disabled

18.3 Register Controlling Key Interrupt

(1) Key return mode register (KRM)

This register controls the KRM0, KRM3, and KRM4 bits using the KR0, KR3, and KR4 signals, respectively.
KRM is set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation clears KRM to 00H.

Figure 18-2. Format of Key Return Mode Register (KRM)

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	0	0	0	KRM4	KRM3	0	0	KRM0

KRMn	Key interrupt mode control (n = 0, 3, or 4)
0	Does not detect key interrupt signal
1	Detects key interrupt signal

Cautions 1. If any of the KRM0, KRM3, or KRM4 bits used is set to 1, set bit 0 (PU40) of the corresponding pull-up resistor register 4 (PU4), or bits 2 or 3 (PU12 or PU13) of the corresponding pull-up resistor register 1 (PU1) to 1.

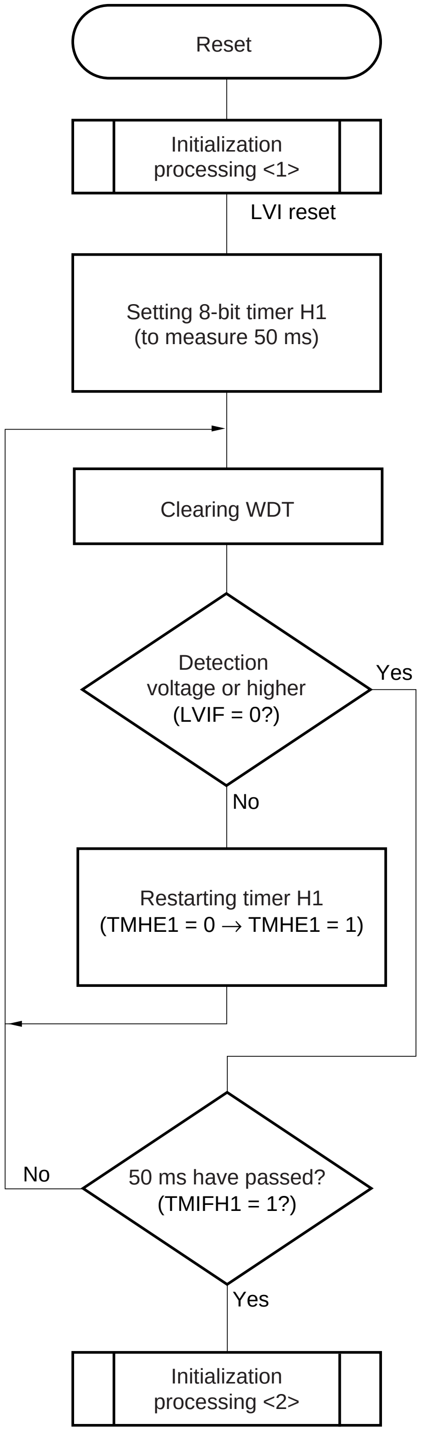
2. If KRM is changed, the interrupt request flag may be set. Therefore, disable interrupts and then change the KRM register. Clear the interrupt request flag and enable interrupts.

3. The bits not used in the key interrupt mode can be used as normal ports.

4. When using the P40/KR0/V_{LC3} pin for the key interrupt function (KR0), set the LCD display mode register (LCDM) to a setting other than the 1/4 bias method. When the pin is set to the 1/4 bias method, it is used as V_{LC3}.

Figure 22-9. Example of Software Processing After Reset Release (1/2)

- If supply voltage fluctuation is 50 ms or less in vicinity of LVI detection voltage


Reset
Initialization processing <1>
LVI reset
Setting 8-bit timer H1 (to measure 50 ms)
Clearing WDT
Detection voltage or higher (LVIF = 0?)
Yes
No
Restarting timer H1 (TMHE1 = 0 → TMHE1 = 1)
No
50 ms have passed? (TMIFH1 = 1?)
Yes
Initialization processing <2>

; Check the reset source[Note]
Initialize the port.

; f_{PRS} = Internal high-speed oscillation clock (8.4 MHz (MAX.)) (default)
Source: f_{PRS} (8.4 MHz (MAX.))/2^{12},
Where comparison value = 102: ≅ 50 ms
Timer starts (TMHE1 = 1).

; The timer counter is cleared and the timer is started.

; Setting of division ratio of system clock,
such as setting of timer or A/D converter

Note A flowchart is shown on the next page.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	**OR**	A, #byte	2	4	–	A ← A ∨ byte	×		
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∨ byte	×		
		A, r Note 3	2	4	–	A ← A ∨ r	×		
		r, A	2	4	–	r ← r ∨ A	×		
		A, saddr	2	4	5	A ← A ∨ (saddr)	×		
		A, !addr16	3	8	9	A ← A ∨ (addr16)	×		
		A, [HL]	1	4	5	A ← A ∨ (HL)	×		
		A, [HL + byte]	2	8	9	A ← A ∨ (HL + byte)	×		
		A, [HL + B]	2	8	9	A ← A ∨ (HL + B)	×		
		A, [HL + C]	2	8	9	A ← A ∨ (HL + C)	×		
	XOR	A, #byte	2	4	–	A ← A ⊻ byte	×		
		saddr, #byte	3	6	8	(saddr) ← (saddr) ⊻ byte	×		
		A, r Note 3	2	4	–	A ← A ⊻ r	×		
		r, A	2	4	–	r ← r ⊻ A	×		
		A, saddr	2	4	5	A ← A ⊻ (saddr)	×		
		A, !addr16	3	8	9	A ← A ⊻ (addr16)	×		
		A, [HL]	1	4	5	A ← A ⊻ (HL)	×		
		A, [HL + byte]	2	8	9	A ← A ⊻ (HL + byte)	×		
		A, [HL + B]	2	8	9	A ← A ⊻ (HL + B)	×		
		A, [HL + C]	2	8	9	A ← A ⊻ (HL + C)	×		
	CMP	A, #byte	2	4	–	A – byte	×	×	×
		saddr, #byte	3	6	8	(saddr) – byte	×	×	×
		A, r Note 3	2	4	–	A – r	×	×	×
		r, A	2	4	–	r – A	×	×	×
		A, saddr	2	4	5	A – (saddr)	×	×	×
		A, !addr16	3	8	9	A – (addr16)	×	×	×
		A, [HL]	1	4	5	A – (HL)	×	×	×
		A, [HL + byte]	2	8	9	A – (HL + byte)	×	×	×
		A, [HL + B]	2	8	9	A – (HL + B)	×	×	×
		A, [HL + C]	2	8	9	A – (HL + C)	×	×	×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

10-bit successive approximation type A/D Converter Characteristics (μPD78F041x only)
(T_A = –40 to +85°C, 2.3 V ≤ AV_{REF} ≤ V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				10	bit
Overall error[Notes 1, 2]	A_{INL}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	6.1		36.7	μs
		2.7 V ≤ AV_{REF} < 4.0 V	12.2		36.7	μs
		2.3 V ≤ AV_{REF} < 2.7 V	27		66.6	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			±0.6	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			±0.6	%FSR
Integral non-linearity error[Note 1]	I_{LE1}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
		2.3 V ≤ AV_{REF} < 2.7 V			±6.5	LSB
Differential non-linearity error [Note 1]	D_{LE1}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±2.0	LSB
		2.3 V ≤ AV_{REF} < 2.7 V			±2.0	LSB
Analog input voltage	V_{AIN1}		AV_{SS}		AV_{REF}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.