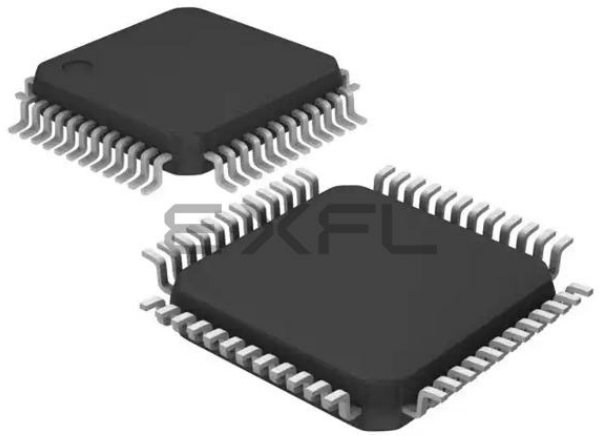

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0411ga-gam-ax

Correspondence between the address values and block numbers in the flash memory are shown below.

Table 3-2. Correspondence Between Address Values and Block Numbers in Flash Memory

Address Value	Block Number	Address Value	Block Number
0000H to 03FFH	00H	4000H to 43FFH	10H
0400H to 07FFH	01H	4400H to 47FFH	11H
0800H to 0BFFH	02H	4800H to 4BFFH	12H
0C00H to 0FFFH	03H	4C00H to 4FFFH	13H
1000H to 13FFH	04H	5000H to 53FFH	14H
1400H to 17FFH	05H	5400H to 57FFH	15H
1800H to 1BFFH	06H	5800H to 5BFFH	16H
1C00H to 1FFFH	07H	5C00H to 5FFFH	17H
2000H to 23FFH	08H	6000H to 63FFH	18H
2400H to 27FFH	09H	6400H to 67FFH	19H
2800H to 2BFFH	0AH	6800H to 6BFFH	1AH
2C00H to 2FFFH	0BH	6C00H to 6FFFH	1BH
3000H to 33FFH	0CH	7000H to 73FFH	1CH
3400H to 37FFH	0DH	7400H to 77FFH	1DH
3800H to 3BFFH	0EH	7800H to 7BFFH	1EH
3C00H to 3FFFH	0FH	7C00H to 7FFFH	1FH

Remark μPD78F0400, 78F0410: Block numbers 00H to 07H
μPD78F0401, 78F0411: Block numbers 00H to 0FH
μPD78F0402, 78F0412: Block numbers 00H to 17H
μPD78F0403, 78F0413: Block numbers 00H to 1FH

4.2.4 Port 4

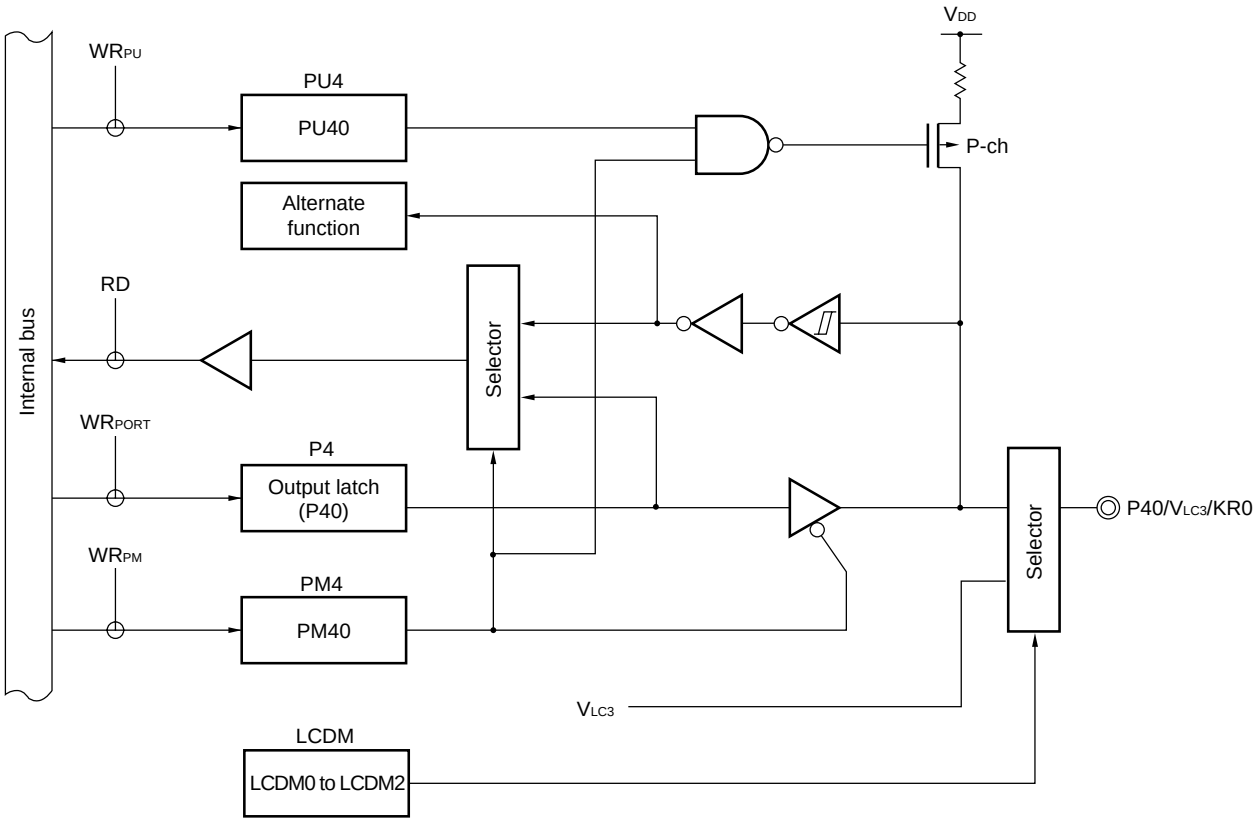
Port 4 is a 1-bit I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). When the P40 pin is used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 4 (PU4).

This port can also be used for power supply voltage pins for driving the LCD and key interrupt input pin.

Reset signal generation sets port 4 to input mode.

Figures 4-7 show a block diagram of port 4.

Figure 4-7. Block Diagram of P40



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
LCDM: LCD display mode register
RD: Read signal
WR××: Write signal

4.3 Registers Controlling Port Function

Port functions are controlled by the following seven types of registers.

- Port mode registers (PM1 to PM4, PM10 to PM12, PM14, PM15)
- Port registers (P1 to P4, P10 to P12, P14, P15)
- Pull-up resistor option registers (PU1, PU3, PU4, PU10 to PU12, PU14, PU15)
- Port function register 1 (PF1)
- Port function register 2 (PF2)
- Port function register ALL (PFALL)
- A/D port configuration register 0 (ADPC0)[Note]

Note μPD78F041x only

(1) Port mode registers (PM1 to PM4, PM10 to PM12, PM14, PM15)

These registers specify input or output mode for the port in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

When port pins are used as alternate-function pins, set the port mode register by referencing **4.5 Settings of Port Mode Register and Output Latch When Using Alternate Function**.

Notes 1. μPD78F041x only.

2. The functions of the P20/ANI0 to P25/ANI5 pins are determined according to the settings of port function register 2 (PF2), A/D port configuration register 0 (ADPC0), port mode register 2 (PM2), analog input channel specification register (ADS).

Table 4-6. Setting Functions of P20/SEG21/ANI0[Note] to P25/SEG16/ANI5[Note] Pins

PF2	ADPC0[Note]	PM2	ADS	P20/SEG21/ANI0[Note] to P25/SEG16/ANI5[Note] Pins
Digital/Analog selection	Analog input selection	Input mode	Does not select ANI.	Analog input (not to be converted)
			Selects ANI.	Analog input (to be converted by successive approximation type A/D converter)
		Output mode	–	Setting prohibited
	Digital I/O selection	Input mode	–	Digital input
		Output mode	–	Digital output
SEG output selection	–	–	–	Segment outpu

Note μPD78F041x only.

3. When using the P121 to P124 pins to connect a resonator for the main system clock (X1, X2) or subsystem clock (XT1, XT2), or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode, XT1 oscillation mode, or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see **5.3 (1) Clock operation mode select register (OSCCTL)** and **(3) Setting of operation mode for subsystem clock pin**). The reset value of OSCCTL is 00H (all of the P121 to P124 are Input port pins).

4. Targeted at registers corresponding to each port.

5. RxD6 can be set as the input source for TI000 by setting ISC1 = 1.

6. Input enable of TM52 via TMH2 can be controlled by setting ISC2 = 1.

7. RxD6 can be set as the input source for INTP0 by setting ISC0 = 1.

8. When the P40/KR0/V_{LC3} pin is set to the 1/4 bias method, it is used as V_{LC3}. When the pin is set to another bias method, it is used for the port function (P40) or the key interrupt function (KR0).

9. Set PF13 = 0 when using as port function.

Remarks 1. ×: Don't care
–: Does not apply.
PM××: Port mode register
P××: Port output latch

2. The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

3. X1, X2 pins can be used as on-chip debug mode setting pins (OCD0A, OCD0B) when the on-chip debug function is used. For detail, see **CHAPTER 25 ON-CHIP DEBUG FUNCTION.**

Table 5-5 shows transition of the CPU clock and examples of setting the SFR registers.

Table 5-5. CPU Clock Transition and SFR Register Setting Examples (1/4)

(1) CPU operating with internal high-speed oscillation clock (B) after reset release (A)

Status Transition	SFR Register Setting
(A) → (B)	SFR registers do not have to be set (default status after reset release).

(2) CPU operating with high-speed system clock (C) after reset release (A)

(The CPU operates with the internal high-speed oscillation clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLK	OSCSEL	MSTOP	OSTC Register	XSEL	MCM0
(A) → (B) → (C) (X1 clock)	0	1	0	Must be checked	1	1
(A) → (B) → (C) (external main clock)	1	1	0	Must not be checked	1	1

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 27 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS)).

(3) CPU operating with subsystem clock (D) after reset release (A)

(The CPU operates with the internal high-speed oscillation clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

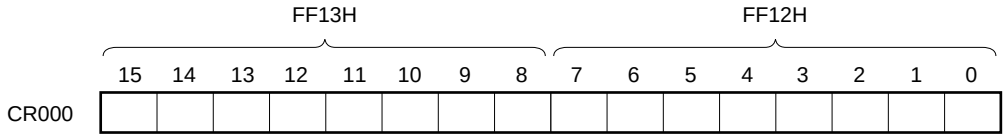
Setting Flag of SFR Register / Status Transition	OSCSELS	Waiting for Oscillation Stabilization	CSS
(A) → (B) → (D)	1	Necessary	1

Remarks 1. (A) to (I) in Table 5-5 correspond to (A) to (I) in Figure 5-15.

2. EXCLK, OSCSEL, OSCSELS: Bits 7, 6, and 4 of the clock operation mode select register (OSCCTL)
MSTOP: Bit 7 of the main OSC control register (MOC)
XSEL, MCM0: Bits 2 and 0 of the main clock mode register (MCM)
CSS: Bit 4 of the processor clock control register (PCC)

Figure 6-3. Format of 16-Bit Timer Capture/Compare Register 000 (CR000)

Address: FF12H, FF13H After reset: 0000H R/W



(i) When CR000 is used as a compare register

The value set in CR000 is constantly compared with the TM00 count value, and an interrupt request signal (INTTM000) is generated if they match. The value is held until CR000 is rewritten.

Caution CR000 does not perform the capture operation when it is set in the comparison mode, even if a capture trigger is input to it.

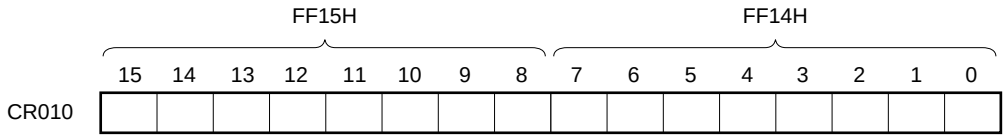
(ii) When CR000 is used as a capture register

The count value of TM00 is captured to CR000 when a capture trigger is input.

As the capture trigger, an edge of a phase reverse to that of the TI000 pin or the valid edge of the TI010 pin can be selected by using CRC00 or PRM00.

Figure 6-4. Format of 16-Bit Timer Capture/Compare Register 010 (CR010)

Address: FF14H, FF15H After reset: 0000H R/W



(i) When CR010 is used as a compare register

The value set in CR010 is constantly compared with the TM00 count value, and an interrupt request signal (INTTM010) is generated if they match.

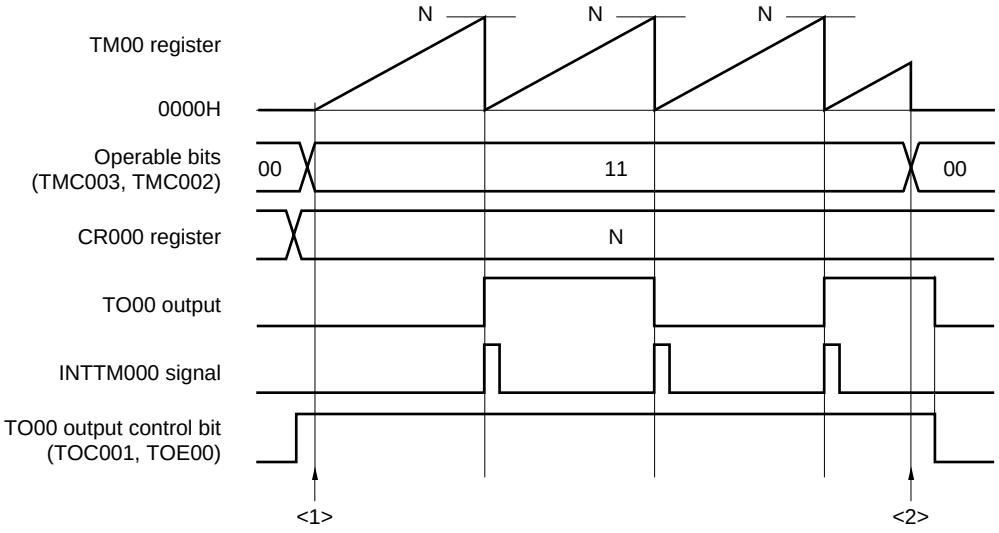
Caution CR010 does not perform the capture operation when it is set in the comparison mode, even if a capture trigger is input to it.

(ii) When CR010 is used as a capture register

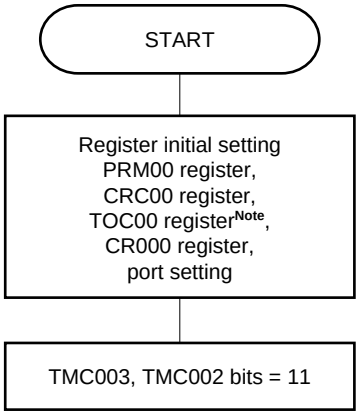
The count value of TM00 is captured to CR010 when a capture trigger is input.

It is possible to select the valid edge of the TI000 pin as the capture trigger. The TI000 pin valid edge is set by PRM00.

Figure 6-19. Example of Software Processing for Square Wave Output Function



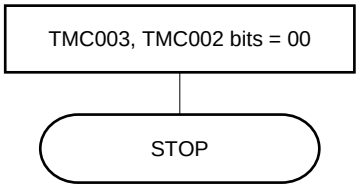
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 11.

Starts count operation

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

Note Care must be exercised when setting TOC00. For details, see **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

8.4.2 Operation as PWM output

In PWM output mode, a pulse with an arbitrary duty and arbitrary cycle can be output.

The 8-bit timer compare register 0n (CMP0n) controls the cycle of timer output (TOHn). Rewriting the CMP0n register during timer operation is prohibited.

The 8-bit timer compare register 1n (CMP1n) controls the duty of timer output (TOHn). Rewriting the CMP1n register during timer operation is possible.

The operation in PWM output mode is as follows.

PWM output (TOHn output) outputs an active level and 8-bit timer counter Hn is cleared to 0 when 8-bit timer counter Hn and the CMP0n register match after the timer count is started. PWM output (TOHn output) outputs an inactive level when 8-bit timer counter Hn and the CMP1n register match.

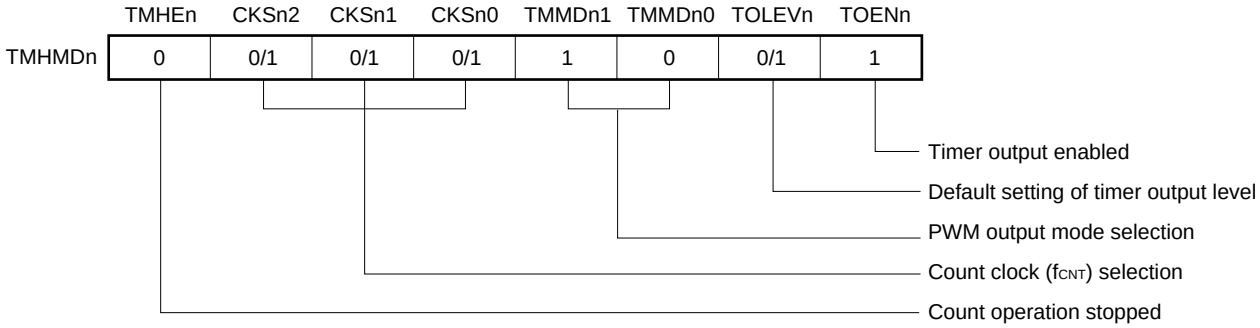
The timer output of TMH2 (PWM output) can only be used as an external event input enable signal of TM52. Note, no pins for external output are available.

Setting

<1> Set each register.

Figure 8-13. Register Setting in PWM Output Mode

(i) Setting timer H mode register n (TMHMDn)



(ii) Setting CMP0n register

- Compare value (N): Cycle setting

(iii) Setting CMP1n register

- Compare value (M): Duty setting

Remarks 1. n = 0 to 2, however, TOH0 and TOH1 only for TOHn

2. 00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH

<2> The count operation starts when TMHEn = 1.

<3> The CMP0n register is the compare register that is to be compared first after counter operation is enabled. When the values of the 8-bit timer counter Hn and the CMP0n register match, the 8-bit timer counter Hn is cleared, an interrupt request signal (INTTMHn) is generated, an active level is output. At the same time, the compare register to be compared with the 8-bit timer counter Hn is changed from the CMP0n register to the CMP1n register.

<4> When the 8-bit timer counter Hn and the CMP1n register match, an inactive level is output and the compare register to be compared with 8-bit timer counter Hn is changed from the CMP1n register to the CMP0n register. At this time, 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

<5> By performing procedures <3> and <4> repeatedly, a pulse with an arbitrary duty can be obtained.

<6> To stop the count operation, set TMHEn = 0.

If the setting value of the CMP0n register is N, the setting value of the CMP1n register is M, and the count clock frequency is f_{CNT}, the PWM pulse output cycle and duty are as follows.

- PWM pulse output cycle = (N + 1)/f_{CNT}
- Duty = (M + 1)/(N + 1)

Cautions 1. The set value of the CMP1n register can be changed while the timer counter is operating. However, this takes a duration of three operating clocks (signal selected by the CKSn2 to CKSn0 bits of the TMHMDn register) from when the value of the CMP1n register is changed until the value is transferred to the register.

2. Be sure to set the CMP1n register when starting the timer count operation (TMHEn = 1) after the timer count operation was stopped (TMHEn = 0) (be sure to set again even if setting the same value to the CMP1n register).

3. Make sure that the CMP1n register setting value (M) and CMP0n register setting value (N) are within the following range.

00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH

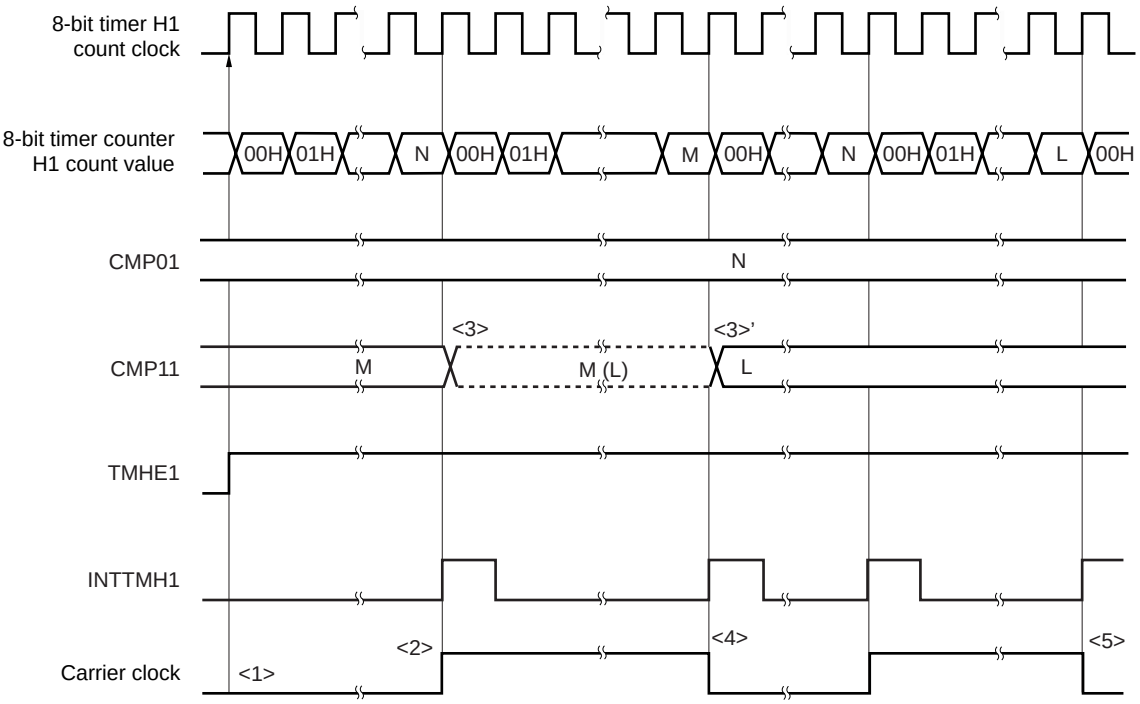
Remarks 1. For the setting of the output pin, see **8.3 (3) Port mode register 3 (PM3)**.

2. For details on how to enable the INTTMHn signal interrupt, see **CHAPTER 17 INTERRUPT FUNCTIONS**.

3. n = 0 to 2, however, TOH0 and TOH1 only for TOHn

Figure 8-17. Carrier Generator Mode Operation Timing (3/3)

(c) Operation when CMP11 is changed



<1> When TMHE1 = 1 is set, the 8-bit timer H1 starts a count operation. At that time, the carrier clock remains default.

<2> When the count value of the 8-bit timer counter H1 matches the value of the CMP01 register, the INTTMH1 signal is output, the carrier signal is inverted, and the timer counter is cleared to 00H. At the same time, the compare register whose value is to be compared with that of the 8-bit timer counter H1 is changed from the CMP01 register to the CMP11 register.

<3> The CMP11 register is asynchronous to the count clock, and its value can be changed while the 8-bit timer H1 is operating. The new value (L) to which the value of the register is to be changed is latched. When the count value of the 8-bit timer counter H1 matches the value (M) of the CMP11 register before the change, the CMP11 register is changed (<3>').

However, it takes three count clocks or more since the value of the CMP11 register has been changed until the value is transferred to the register. Even if a match signal is generated before the duration of three count clocks elapses, the new value is not transferred to the register.

<4> When the count value of 8-bit timer counter H1 matches the value (M) of the CMP1 register before the change, the INTTMH1 signal is output, the carrier signal is inverted, and the timer counter is cleared to 00H. At the same time, the compare register whose value is to be compared with that of the 8-bit timer counter H1 is changed from the CMP11 register to the CMP01 register.

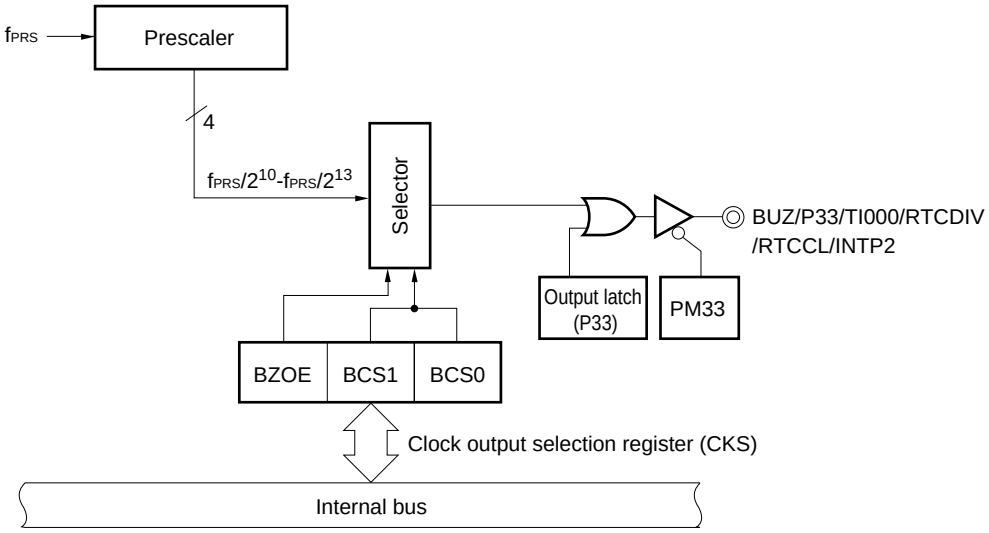
<5> The timing at which the count value of the 8-bit timer counter H1 and the CMP11 register value match again is indicated by the value after the change (L).

CHAPTER 11 BUZZER OUTPUT CONTROLLER

11.1 Functions of Buzzer Output Controller

The buzzer output is intended for square-wave output of buzzer frequency selected with CKS.
Figure 11-1 shows the block diagram of buzzer output controller.

Figure 11-1. Block Diagram of Buzzer Output Controller



11.2 Configuration of Buzzer Output Controller

The buzzer output controller includes the following hardware.

Table 11-1. Configuration of Buzzer Output Controller

Item	Configuration
Control registers	Clock output selection register (CKS) Port mode register 3 (PM3) Port register 3 (P3)

11.3 Registers Controlling Buzzer Output Controller

The following two registers are used to control the buzzer output controller.

- Clock output selection register (CKS)
- Port mode register 3 (PM3)

(1) Clock output selection register (CKS)

This register sets output enable/disable for the buzzer frequency output (BUZ), and sets the output clock.

CKS is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CKS to 00H.

(11) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 12-22. Internal Equivalent Circuit of ANIn Pin

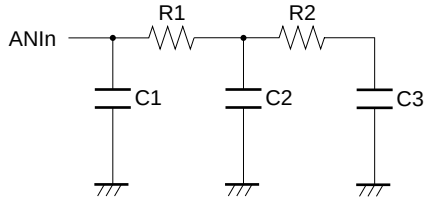


Table 12-4. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

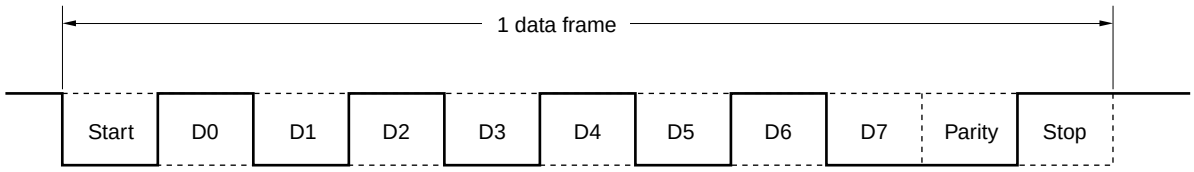
AV_{REF}	R1	R2	C1	C2	C3
2.7 V	TBD	TBD	TBD	TBD	TBD
4.5 V	TBD	TBD	TBD	TBD	TBD

Remarks 1. The resistance and capacitance values shown in Table 12-4 are not guaranteed values.

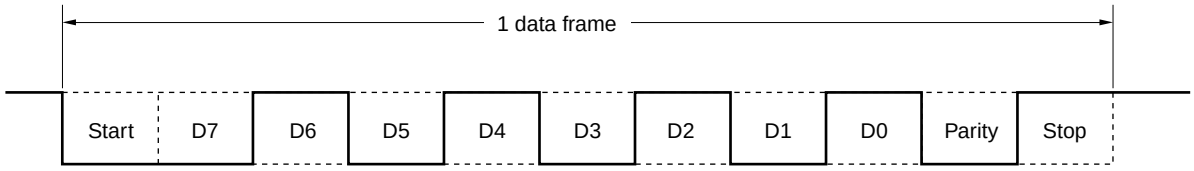
2. n = 0 to 5

Figure 14-16. Example of Normal UART Transmit/Receive Data Waveform

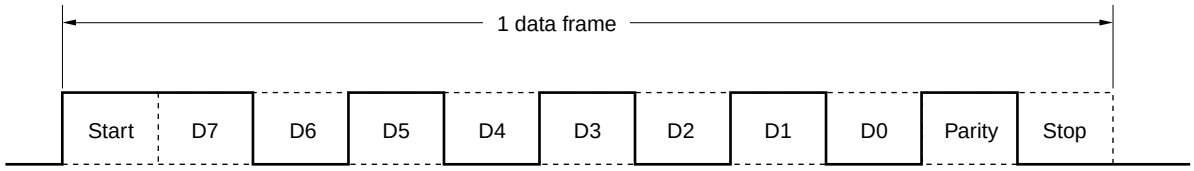
1. Data length: 8 bits, LSB first, Parity: Even parity, Stop bit: 1 bit, Communication data: 55H



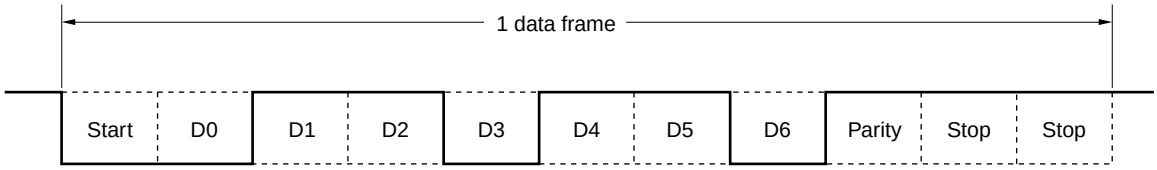
2. Data length: 8 bits, MSB first, Parity: Even parity, Stop bit: 1 bit, Communication data: 55H



3. Data length: 8 bits, MSB first, Parity: Even parity, Stop bit: 1 bit, Communication data: 55H, TxD6 pin inverted output



4. Data length: 7 bits, LSB first, Parity: Odd parity, Stop bit: 2 bits, Communication data: 36H



5. Data length: 8 bits, LSB first, Parity: None, Stop bit: 1 bit, Communication data: 87H

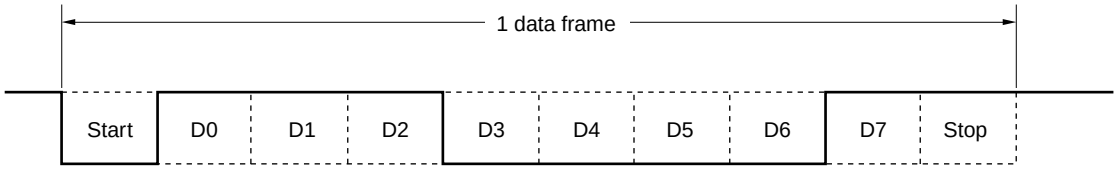
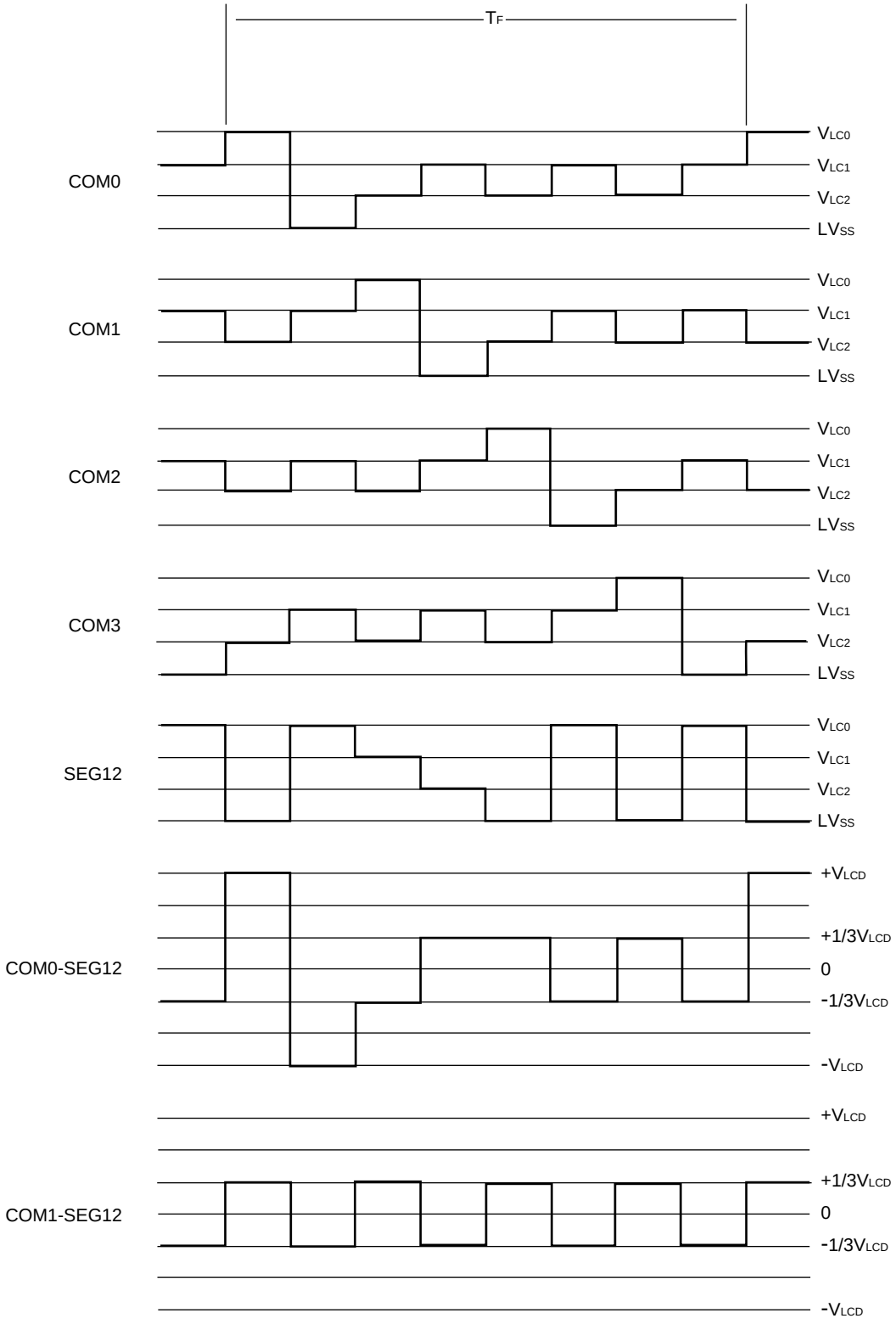


Figure 15-22. Four-Time-Slice LCD Drive Waveform Examples (1/3 Bias Method)



Remark The waveforms for COM2 to SEG12 and COM3 to SEG12 are omitted.

16.4.2 Manchester code generator mode

This mode is used to transmit data in Manchester code format using the MCGO pin.

(1) Register description

MCG control register 0 (MC0CTL0), MCG control register 1 (MC0CTL1), and MCG control register 2 (MC0CTL2) are used to set the Manchester code generator mode.

(a) MCG control register 0 (MC0CTL0)

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Address: FF4CH After reset: 10H R/W

Symbol	<7>	6	5	<4>	3	2	<1>	<0>
MC0CTL0	MC0PWR	0	0	MC0DIR	0	0	MC0OSL	MC0OLV

MC0PWR	Operation control
0	Operation stopped
1	Operation enabled

MC0DIR	First bit specification
0	MSB
1	LSB

MC0OSL	Data format
0	Manchester code
1	Bit sequential data

MC0OLV	Output level when transmission suspended
0	Low level
1	High level

Caution Clear (0) the MC0PWR bit before rewriting the MC0DIR, MC0OSL, and MC0OLV bits (it is possible to rewrite these bits by an 8-bit memory manipulation instruction at the same time when the MC0PWR bit is set (1)).

17.3 Registers Controlling Interrupt Functions

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag register (IF0L, IF0H, IF1L, IF1H)
- Interrupt mask flag register (MK0L, MK0H, MK1L, MK1H)
- Priority specification flag register (PR0L, PR0H, PR1L, PR1H)
- External interrupt rising edge enable register (EGP)
- External interrupt falling edge enable register (EGN)
- Program status word (PSW)

Table 17-2 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 17-2. Flags Corresponding to Interrupt Request Sources

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTLVI	LVIIF	IF0L	LVIMK	MK0L	LVIPR	PR0L
INTP0	PIF0		PMK0		PPR0	
INTP1	PIF1		PMK1		PPR1	
INTP2	PIF2		PMK2		PPR2	
INTP3	PIF3		PMK3		PPR3	
INTSRE6	SREIF6		SREMK6		SREPR6	
INTSR6	SRIF6	IF0H	SRMK6	MK0H	SRPR6	PR0H
INTST6	STIF6		STMK6		STPR6	
INTST0	STIF0		STMK0		STPR0	
INTTMH1	TMIFH1		TMMKH1		TMPRH1	
INTTMH0	TMIFH0		TMMKH0		TMPRH0	
INTTM50	TMIF50		TMMK50		TMPR50	
INTTM000	TMIF000		TMMK000		TMPR000	
INTTM010	TMIF010		TMMK010		TMPR010	
INTAD[Note 1]	ADIF[Note 1]	IF1L	ADMK[Note 1]	MK1L	ADPR[Note 1]	PR1L
INTSR0	SRIF0		SRMK0		SRPR0	
INTRTC	RTCIF		RTCMK		RTCPR	
INTTM51[Note 2]	TMIF51		TMMK51		TMPR51	
INTKR	KRIF		KRMK		KRPR	
INTRTCI	RTCIIF		RTCIMK		RTCIPR	
INTTM52	TMIF52		TMMK52		TMPR52	
INTTMH2	TMHIF2	IF1H	TMHMK2	MK1H	TMHPR2	PR1H
INTMCG	MCGIF		MCGMK		MCGPR	

Notes 1. μPD78F041x only.

2. When 8-bit timer/event counter 51 and 8-bit timer H1 are used in the carrier generator mode, an interrupt is generated upon the timing when the INTTM5H1 signal is generated (see **Figure 8-15 Transfer Timing**).

24.8 Flash Memory Programming by Self-Programming (Under Development)

The 78K0/LC3 supports a self-programming function that can be used to rewrite the flash memory via a user program. Because this function allows a user application to rewrite the flash memory by using the 78K0/LC3 self-programming sample library, it can be used to upgrade the program in the field.

If an interrupt occurs during self-programming, self-programming can be temporarily stopped and interrupt servicing can be executed. To execute interrupt servicing, restore the normal operation mode after self-programming has been stopped, and execute the EI instruction. After the self-programming mode is later restored, self-programming can be resumed.

Cautions 1. The self-programming function cannot be used when the CPU operates with the subsystem clock.

2. Input a high level to the FLMD0 pin during self-programming.

3. Be sure to execute the DI instruction before starting self-programming.
The self-programming function checks the interrupt request flags (IF0L, IF0H, IF1L, and IF1H). If an interrupt request is generated, self-programming is stopped.

4. Self-programming is also stopped by an interrupt request that is not masked even in the DI status. To prevent this, mask the interrupt by using the interrupt mask flag registers (MK0L, MK0H, MK1L, and MK1H).

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P12, P13, P31 to P34, P40, P100, P101, P112, P113, P120, P140 to P143, P150 to P153	−10	mA
		Total of all pins −35 mA	P12, P13, P31 to P34, P40, P120	−25	mA
			P100, P101, P112, P113, P140 to P143, P150 to P153	−10	mA
	I_{OH2}	Per pin	P20 to P25	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL}	Per pin	P12, P13, P31 to P34, P40, P100, P101, P112, P113, P120, P140 to P143, P150 to P153	30	mA
		Total of all pins 80 mA	P12, P13, P31 to P34, P40, P120	40	mA
			P100, P101, P112, P113, P140 to P143, P150 to P153	40	mA
		Per pin	P20 to P25	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.