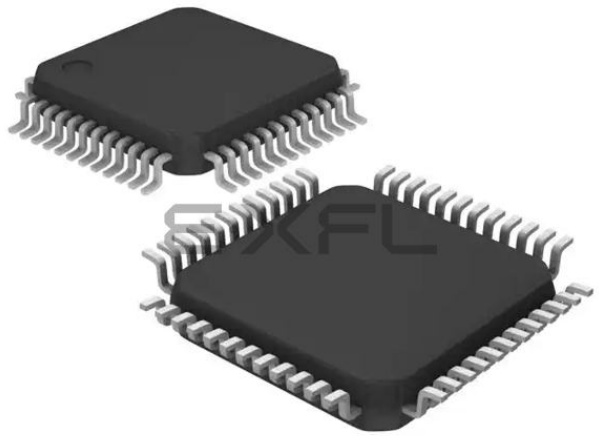

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0412ga-gam-ax

INTRODUCTION

Readers

This manual is intended for user engineers who wish to understand the functions of the 78K0/LC3 and design and develop application systems and programs for these devices. The target products are as follows.

78K0/LC3: μPD78F0400, 78F0401, 78F0402, 78F0403
μPD78F0410, 78F0411, 78F0412, 78F0413

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The 78K0/LC3 manual is separated into two parts: this manual and the instructions edition (common to the 78K0 microcontrollers).

78K0/LC3 User's Manual (This Manual)	**78K/0 Series User's Manual Instructions**
• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**.
- How to interpret the register format:
  → For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.
- To know details of the 78K0 microcontroller instructions:
  → Refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

The list of functions in the 78K0/Lx3 Microcontrollers is shown below. (1/3)

Item \ Part Number			78K0/LC3								78K0/LD3							
			μPD78F040x				μPD78F041x				μPD78F042x				μPD78F043x			
			48 Pins								52 Pins							
Flash memory (KB)			8	16	24	32	8	16	24	32	8	16	24	32	8	16	24	32
RAM (KB)			0.5	0.75	1	1	0.5	0.75	1	1	0.5	0.75	1	1	0.5	0.75	1	1
Power supply voltage			V_{DD} = 1.8 to 5.5 V															
Regulator			Provided															
Minimum instruction execution time			0.2 μs (10 MHz: V_{DD} = 2.7 to 5.5 V)/ 0.4 μs (5 MHz: V_{DD} = 1.8 to 5.5 V)															
Clock	Main	High-speed system clock	10 MHz: V_{DD} = 2.7 to 5.5 V/5 MHz: V_{DD} = 1.8 to 5.5 V															
		Internal high-speed oscillation clock	8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V															
	Subclock		32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V															
	Internal low-speed oscillation clock		240 kHz (TYP.): V_{DD} = 1.8 to 5.5 V															
Port	Total		30								34							
Timer	16 bits (TM0)		1 ch															
	8 bits (TM5)		3 ch															
	8 bits (TMH)		3 ch															
	RTC		1 ch															
	WDT		1 ch															
Serial interface	3-wire CSI		–								1 ch[Note 1]							
	UART		1 ch								1 ch[Note 1]							
	UART supporting LIN-bus		1 ch[Note 2]								1 ch[Note 3]							
LCD	Type		External resistance division and internal resistance division are switchable.															
	Segment signal		22 (18)[Note 4]								24 (20)[Note 4]							
	Common signal		4 (8)[Note 4]															
10-bit successive approximation type A/D			–				6 ch				–				6 ch			
16-bit ΔΣ type A/D			–															
Interrupt	External		5															
	Internal		17				18				19				20			
Key interrupt			3 ch								5 ch							
Reset	$\overline{\text{RESET}}$ pin		Provided															
	POC		1.59 V ±0.15 V (Time for rising up to 1.8 V : 3.6 ms (MAX.))															
	LVI		The detection level of the supply voltage is selectable in 16 steps.															
	WDT		Provided															
Clock output			–															
Buzzer output			Provided															
Remote controller receiver			–								Provided							
MCG			Provided															
On-chip debug function			Provided															
Operating ambient temperature			T_A = –40 to +85°C															

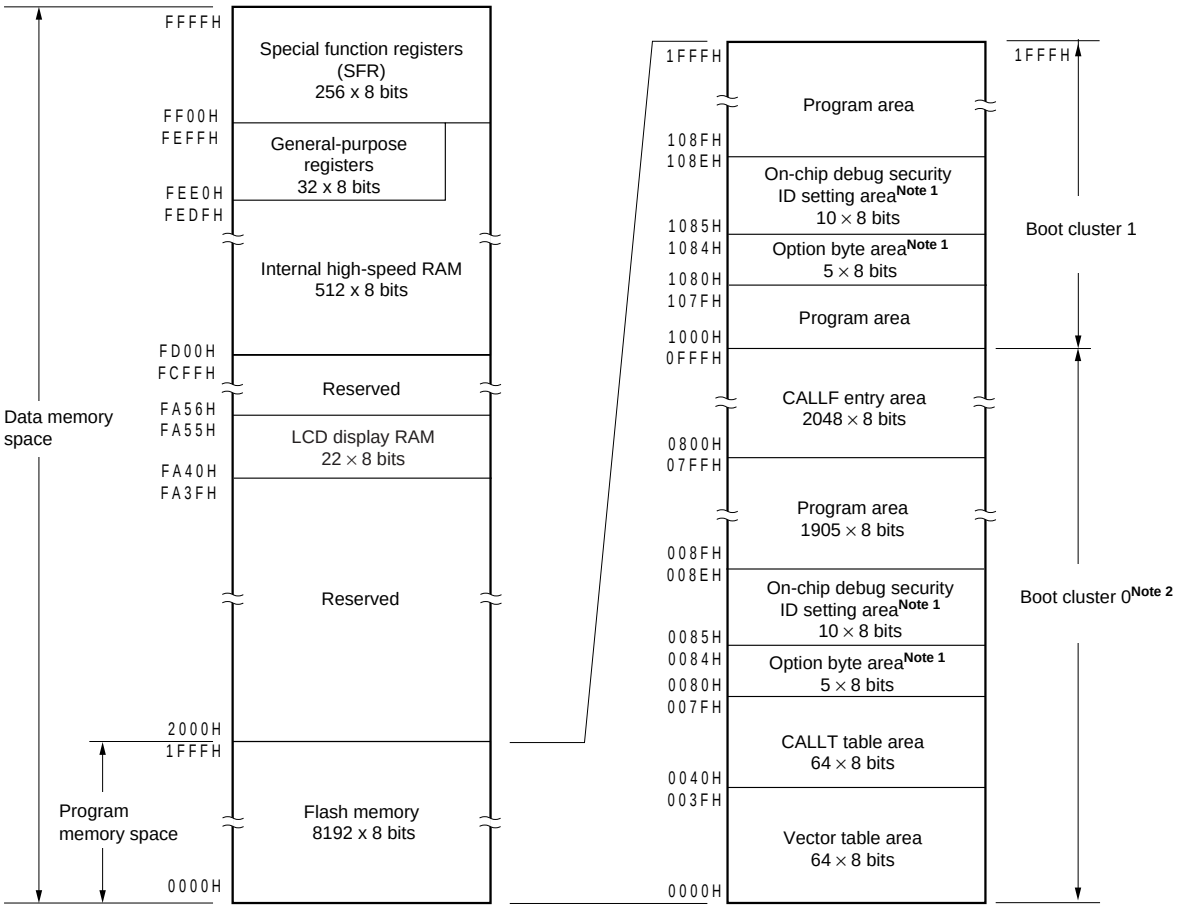
Notes 1. Since 3-wire CSI and UART are used as alternate-function pins, they must be assigned to either of the functions for use.

2. The LIN-bus supporting UART pins can be changed to the UART pins (pin numbers 47 and 48).

3. The LIN-bus supporting UART pins can be changed to the 3-wire CSI/UART pins (pin numbers 50 and 51).

4. The values in parentheses are the number of signal outputs when 8com is used.

Figure 3-1. Memory Map (μPD78F0400, 78F0410)



Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (see **24.7 Security Setting**).

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-2 Correspondence Between Address Values and Block Numbers in Flash Memory**.

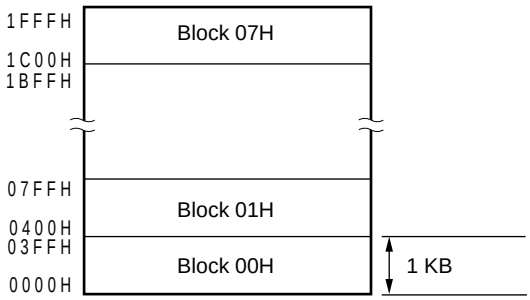


Table 4-2. Port Functions

Function Name	I/O	Function	After Reset	Alternate Function
P12	I/O	Port 1. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	RxD0/KR3/<RxD6>
P13				TxD0/KR4/<TxD6>
P20	I/O	Port 2. 6-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	SEG21/ANI0Note
P21				SEG20/ANI1Note
P22				SEG19/ANI2Note
P23				SEG18/ANI3Note
P24				SEG17/ANI4Note
P25				SEG16/ANI5Note
P31	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOH1/INTP3
P32				TOH0/MCGO
P33				TI000/RTCDIV/ RTCCL/BUZ/INTP2
P34				TI52/TI010/TO00/ RTC1HZ/INTP1
P40	I/O	Port 4. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	V_{LC3}/KR0
P100, P101	I/O	Port 10. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG4, SEG5
P112	I/O	Port 11. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG6/TxD6
P113				SEG7/RxD6
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. Only for P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1/OCD0A
P122				X2/EXCLK/OCD0B
P123				XT1
P124				XT2
P140 to P143	I/O	Port 14. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG8 to SEG11
P150 to P153	I/O	Port 15. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG12 to SEG15

Note μPD78F041x only.

Remark The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

(9) Internal high-speed oscillation trimming register (HIOTRM)

This register corrects the accuracy of the internal high-speed oscillator. The accuracy can be corrected by self-measuring the frequency of the internal high-speed oscillator, using a subsystem clock using a crystal resonator or using a timer with high-accuracy external clock input, such as a real-time counter.

HIOTRM can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets HIOTRM to 10H.

Caution If the temperature or V_{DD} pin voltage is changed after accuracy correction, the frequency will fluctuate. Also, if a value other than the initial value (10H) is set to the HIOTRM register, the oscillation accuracy of the internal high-speed oscillation clock may exceed the MIN. and MAX. values described in CHAPTER 27 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) due to the subsequent fluctuation in the temperature or V_{DD} voltage, or HIOTRM register setting value. If the temperature or V_{DD} voltage fluctuates, accuracy correction must be executed either before frequency accuracy will be required or regularly.

Table 5-8. Maximum Time Required for Main System Clock Switchover

Set Value Before Switchover	Set Value After Switchover	
MCM0	MCM0	
	0	1
0		1 + $2f_{RH}/f_{XH}$ clock
1	1 + $2f_{XH}/f_{RH}$ clock	

Caution When switching the internal high-speed oscillation clock to the high-speed system clock, bit 2 (XSEL) of MCM must be set to 1 in advance. The value of XSEL can be changed only once after a reset release.

Remarks 1. The number of clocks listed in Table 5-8 is the number of main system clocks before switchover.

2. Calculate the number of clocks in Table 5-8 by removing the decimal portion.

Example When switching the main system clock from the internal high-speed oscillation clock to the high-speed system clock (@ oscillation with f_{RH} = 8 MHz, f_{XH} = 10 MHz)

$1 + 2f_{RH}/f_{XH} = 1 + 2 \times 8/10 = 1 + 2 \times 0.8 = 1 + 1.6 = 2.6 \rightarrow 2$ clocks

5.6.9 Conditions before clock oscillation is stopped

The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped.

Table 5-9. Conditions Before the Clock Oscillation Is Stopped and Flag Settings

Clock	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
Internal high-speed oscillation clock	MCS = 1 or CLS = 1 (The CPU is operating on a clock other than the internal high-speed oscillation clock)	RSTOP = 1
X1 clock	MCS = 0 or CLS = 1 (The CPU is operating on a clock other than the high-speed system clock)	MSTOP = 1
External main system clock		
XT1 clock	CLS = 0 (The CPU is operating on a clock other than the subsystem clock)	OSCSELS = 0

Cautions 1. When TMHE0 = 1, setting the other bits of TMHMD0 is prohibited. However, TMHMD0 can be refreshed (the same value is written).

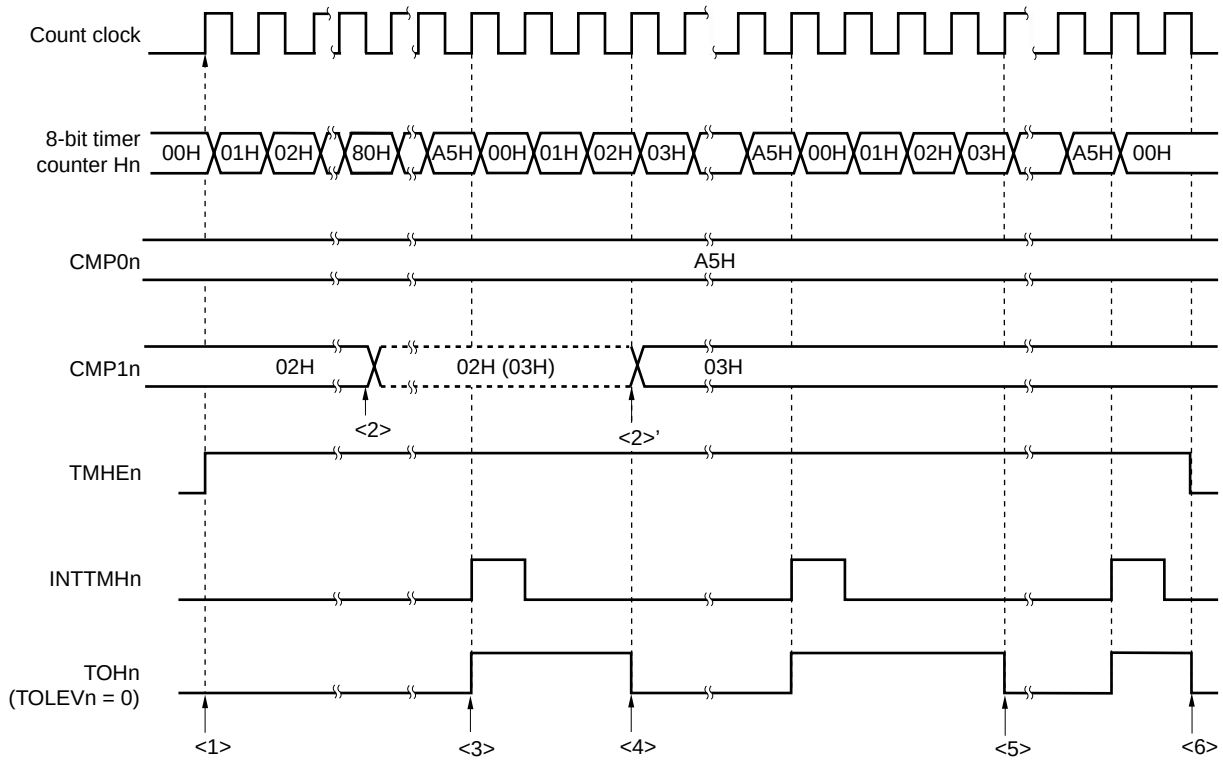
2. In the PWM output mode, be sure to set the 8-bit timer H compare register 10 (CMP10) when starting the timer count operation (TMHE0 = 1) after the timer count operation was stopped (TMHE0 = 0) (be sure to set again even if setting the same value to CMP10).

3. The actual TOH0/P32/MCGO pin output is determined depending on PM32 and P32, besides TOH0 output.

Remark f_{PRS}: Peripheral hardware clock frequency

Figure 8-14. Operation Timing in PWM Output Mode (4/4)

(e) Operation by changing CMP1n (CMP1n = 02H → 03H, CMP0n = A5H)



<1> The count operation is enabled by setting TMHEn = 1. Start 8-bit timer counter Hn by masking one count clock to count up. At this time, PWM output outputs an inactive level.

<2> The CMP1n register value can be changed during timer counter operation. This operation is asynchronous to the count clock.

<3> When the values of 8-bit timer counter Hn and the CMP0n register match, the value of 8-bit timer counter Hn is cleared, an active level is output, and the INTTMHn signal is output.

<4> If the CMP1n register value is changed, the value is latched and not transferred to the register. When the values of the 8-bit timer counter Hn and the CMP1n register before the change match, the value is transferred to the CMP1n register and the CMP1n register value is changed (<2>').

However, three count clocks or more are required from when the CMP1n register value is changed to when the value is transferred to the register. If a match signal is generated within three count clocks, the changed value cannot be transferred to the register.

<5> When the values of 8-bit timer counter Hn and the CMP1n register after the change match, an inactive level is output. 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

<6> Clearing the TMHEn bit to 0 during timer Hn operation sets the INTTMHn signal to the default and PWM output to an inactive level.

Remark n = 0 to 2, however, TOH0 and TOH1 only for TOHn

11.2 Configuration of Buzzer Output Controller

The buzzer output controller includes the following hardware.

Table 11-1. Configuration of Buzzer Output Controller

Item	Configuration
Control registers	Clock output selection register (CKS) Port mode register 3 (PM3) Port register 3 (P3)

11.3 Registers Controlling Buzzer Output Controller

The following two registers are used to control the buzzer output controller.

- Clock output selection register (CKS)
- Port mode register 3 (PM3)

(1) Clock output selection register (CKS)

This register sets output enable/disable for the buzzer frequency output (BUZ), and sets the output clock.

CKS is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CKS to 00H.

(5) Port mode register 1 (PM1)

This register sets port 1 input/output in 1-bit units.

When using the P13/TxD0/KR4/<TxD6> pin for serial interface data output, clear PM13 to 0. The output latch of P13 at this time may be 0 or 1.

When using the P12/RxD0/KR3/<RxD6> pin for serial interface data input, set PM12 to 1. The output latch of P12 at this time may be 0 or 1.

PM1 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Remark The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

Figure 13-6. Format of Port Mode Register 1 (PM1)

Address: FF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	1	1	1	1	PM13	PM12	1	1

PM1n	P1n pin I/O mode selection (n = 2, 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

(6) Asynchronous serial interface control register 6 (ASICL6)

This register controls the serial communication operations of serial interface UART6.

ASICL6 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 16H.

Caution ASICL6 can be refreshed (the same value is written) by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of ASIM6 = 1 or bits 7 and 5 (POWER6, RXE6) of ASIM6 = 1). However, do not set both SBRT6 and SBTT6 to 1 by a refresh operation during SBF reception (SBRT6 = 1) or SBF transmission (until INTST6 occurs since SBTT6 has been set (1)), because it may re-trigger SBF reception or SBF transmission.

Figure 14-10. Format of Asynchronous Serial Interface Control Register 6 (ASICL6) (1/2)

Address: FF58H After reset: 16H R/W[Note]

Symbol	<7>	<6>	5	4	3	2	1	0
ASICL6	SBRF6	SBRT6	SBTT6	SBL62	SBL61	SBL60	DIR6	TXDLV6

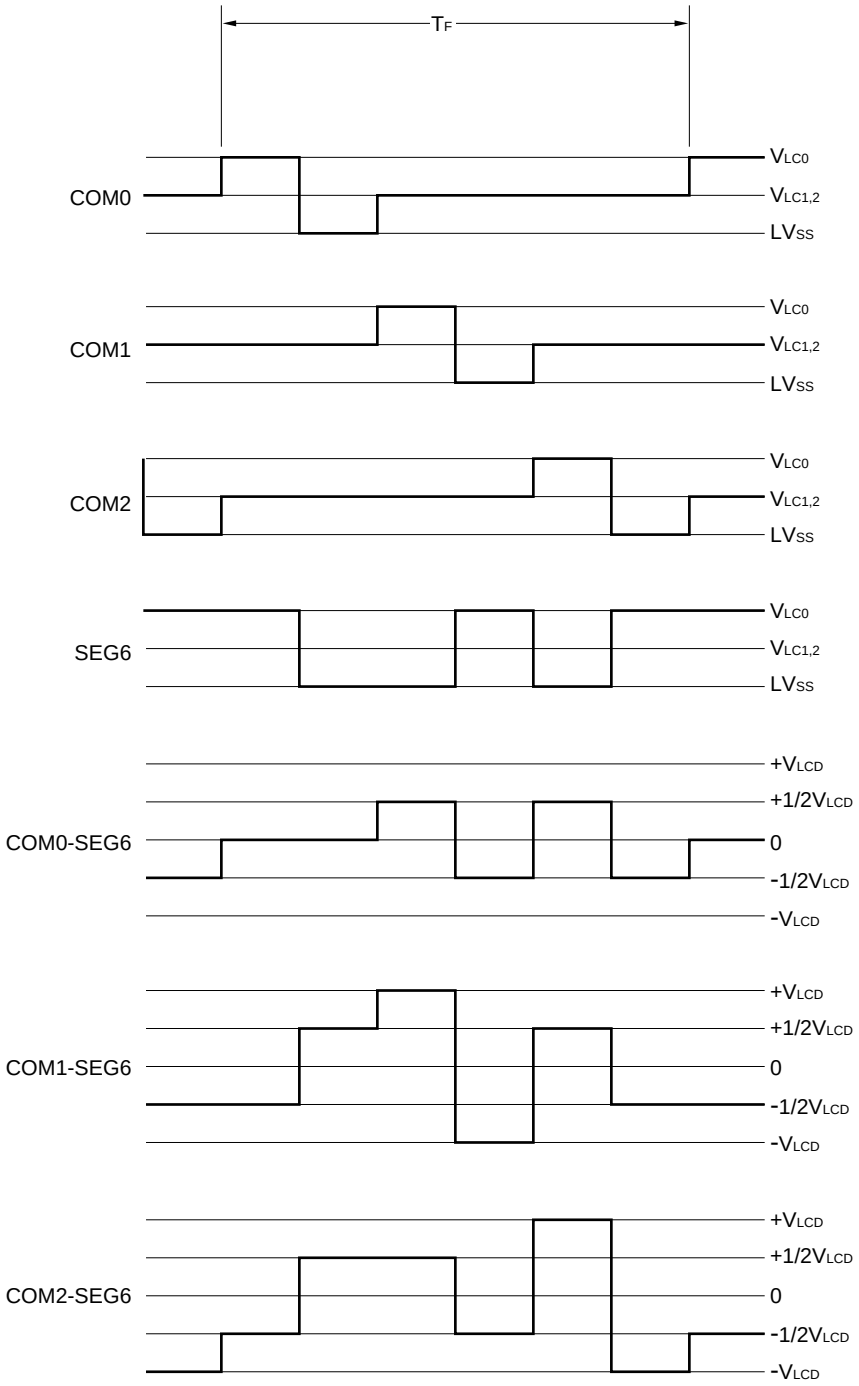
SBRF6	SBF reception status flag
0	If POWER6 = 0 and RXE6 = 0 or if SBF reception has been completed correctly
1	SBF reception in progress

SBRT6	SBF reception trigger
0	–
1	SBF reception trigger

SBTT6	SBF transmission trigger
0	–
1	SBF transmission trigger

Note Bit 7 is read-only.

Figure 15-18. Three-Time-Slice LCD Drive Waveform Examples (1/2 Bias Method)



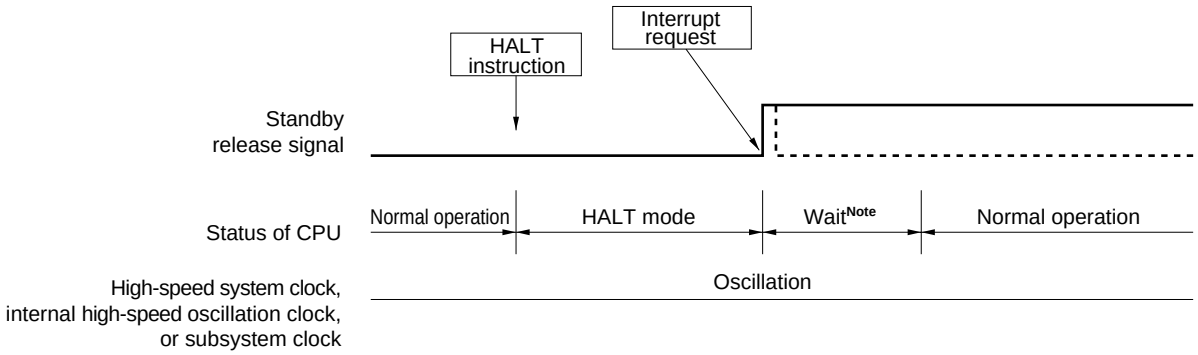
(2) HALT mode release

The HALT mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 19-3. HALT Mode Release by Interrupt Request Generation



Note The wait time is as follows:

- When vectored interrupt servicing is carried out: 8 or 9 clocks
- When vectored interrupt servicing is not carried out: 2 or 3 clocks

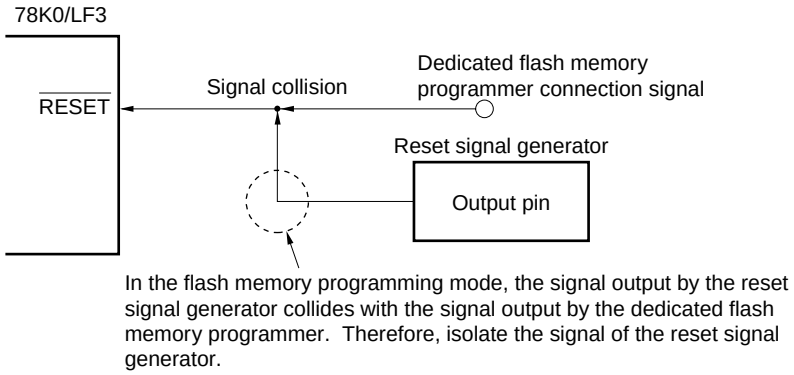
Remark The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

24.5.3 $\overline{\text{RESET}}$ pin

If the reset signal of the dedicated flash memory programmer is connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board, signal collision takes place. To prevent this collision, isolate the connection with the reset signal generator.

If the reset signal is input from the user system while the flash memory programming mode is set, the flash memory will not be correctly programmed. Do not input any signal other than the reset signal of the dedicated flash memory programmer.

Figure 24-8. Signal Collision ($\overline{\text{RESET}}$ Pin)



24.5.4 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to V_{DD} or V_{SS} via a resistor.

24.5.5 REGC pin

Connect the REGC pin to GND via a capacitor (0.47 to 1 μF: recommended) in the same manner as during normal operation.

24.6.3 Selecting communication mode

In the 78K0/LC3, a communication mode is selected by inputting pulses to the FLMD0 pin after the dedicated flash memory programming mode is entered. These FLMD0 pulses are generated by the flash memory programmer.

The following table shows the relationship between the number of pulses and communication modes.

Table 24-6. Communication Modes

Communication Mode	Standard Setting[Note 1]				Pins Used	Peripheral Clock	Number of FLMD0 Pulses
	Port	Speed	Frequency	Multiply Rate			
UART (UART6)	UART-Ext-Osc	115,200 bps[Note 3]	2 to 10 MHz[Note 2]	1.0	TxD6, RxD6	f_X	0
	UART-Ext-FP4CK					f_{EXCLK}	3

Notes 1. Selection items for Standard settings on GUI of the flash memory programmer.

2. The possible setting range differs depending on the voltage. For details, see **CHAPTER 27 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS)**.

3. Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.

Caution When UART6 is selected, the receive clock is calculated based on the reset command sent from the dedicated flash memory programmer after the FLMD0 pulse has been received.

Remark f_X: X1 clock

f_{EXCLK}: External main system clock

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P12, P13, P31 to P34, P40, P100, P101, P112, P113, P120, P140 to P143, P150 to P153	−10	mA
		Total of all pins −35 mA	P12, P13, P31 to P34, P40, P120	−25	mA
			P100, P101, P112, P113, P140 to P143, P150 to P153	−10	mA
	I_{OH2}	Per pin	P20 to P25	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL}	Per pin	P12, P13, P31 to P34, P40, P100, P101, P112, P113, P120, P140 to P143, P150 to P153	30	mA
		Total of all pins 80 mA	P12, P13, P31 to P34, P40, P120	40	mA
			P100, P101, P112, P113, P140 to P143, P150 to P153	40	mA
		Per pin	P20 to P25	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (1/5)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note1]	I_{OH1}	Per pin for P12, P13, P31 to P34, P40, P120	4.0 V ≤ V_{DD} ≤ 5.5 V			–3.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–2.5	mA
			1.8 V ≤ V_{DD} < 2.7 V			–1.0	mA
		Per pin for P100, P101, P112, P113, P140 to P143, P150 to P153	4.0 V ≤ V_{DD} ≤ 5.5 V			–0.1	mA
			2.7 V ≤ V_{DD} < 4.0 V			–0.1	mA
			1.8 V ≤ V_{DD} < 2.7 V			–0.1	mA
		Total[Note3] of P12, P13, P31 to P34, P40, P120	4.0 V ≤ V_{DD} ≤ 5.5 V			–20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
		Total[Note3] of P100, P101, P112, P113, P140 to P143, P150 to P153	4.0 V ≤ V_{DD} ≤ 5.5 V			–2.8	mA
			2.7 V ≤ V_{DD} < 4.0 V			–2.8	mA
			1.8 V ≤ V_{DD} < 2.7 V			–2.8	mA
		Total[Note3] of all pins	4.0 V ≤ V_{DD} ≤ 5.5 V			–22.8	mA
			2.7 V ≤ V_{DD} < 4.0 V			–12.8	mA
			1.8 V ≤ V_{DD} < 2.7 V			–7.8	mA
	I_{OH2}	Per pin for P20 to P25	AV_{REF} = V_{DD}			–0.1	mA
Output current, low[Note2]	I_{OL1}	Per pin for P12, P13, P31 to P34, P40, P120	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			5.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.0	mA
		Per pin for P100, P101, P112, P113, P140 to P143, P150 to P153	4.0 V ≤ V_{DD} ≤ 5.5 V			0.4	mA
			2.7 V ≤ V_{DD} < 4.0 V			0.4	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.4	mA
		Total[Note3] of P12, P13, P31 to P34, P40, P120	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total[Note3] of P100, P101, P112, P113, P140 to P143, P150 to P153	4.0 V ≤ V_{DD} ≤ 5.5 V			11.2	mA
			2.7 V ≤ V_{DD} < 4.0 V			11.2	mA
			1.8 V ≤ V_{DD} < 2.7 V			11.2	mA
		Total[Note3] of all pins	4.0 V ≤ V_{DD} ≤ 5.5 V			31.2	mA
			2.7 V ≤ V_{DD} < 4.0 V			26.2	mA
			1.8 V ≤ V_{DD} < 2.7 V			20.2	mA
	I_{OL2}	Per pin for P20 to P25	AV_{REF} = V_{DD}			0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from V_{DD} to an output pin.

2. Value of current at which the device operation is guaranteed even if the current flows from an output pin to GND.

3. Specification under conditions where the duty factor is 70% (time for which current is output is 0.7 × t and time for which current is not output is 0.3 × t, where t is a specific time). The total output current of the pins at a duty factor of other than 70% can be calculated by the following expression.

- Where the duty factor of I_{OH} is n%: Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where the duty factor is 50%, I_{OH} = 20.0 mA

Total output current of pins = (20.0 × 0.7)/(50 × 0.01) = 28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (2/5)

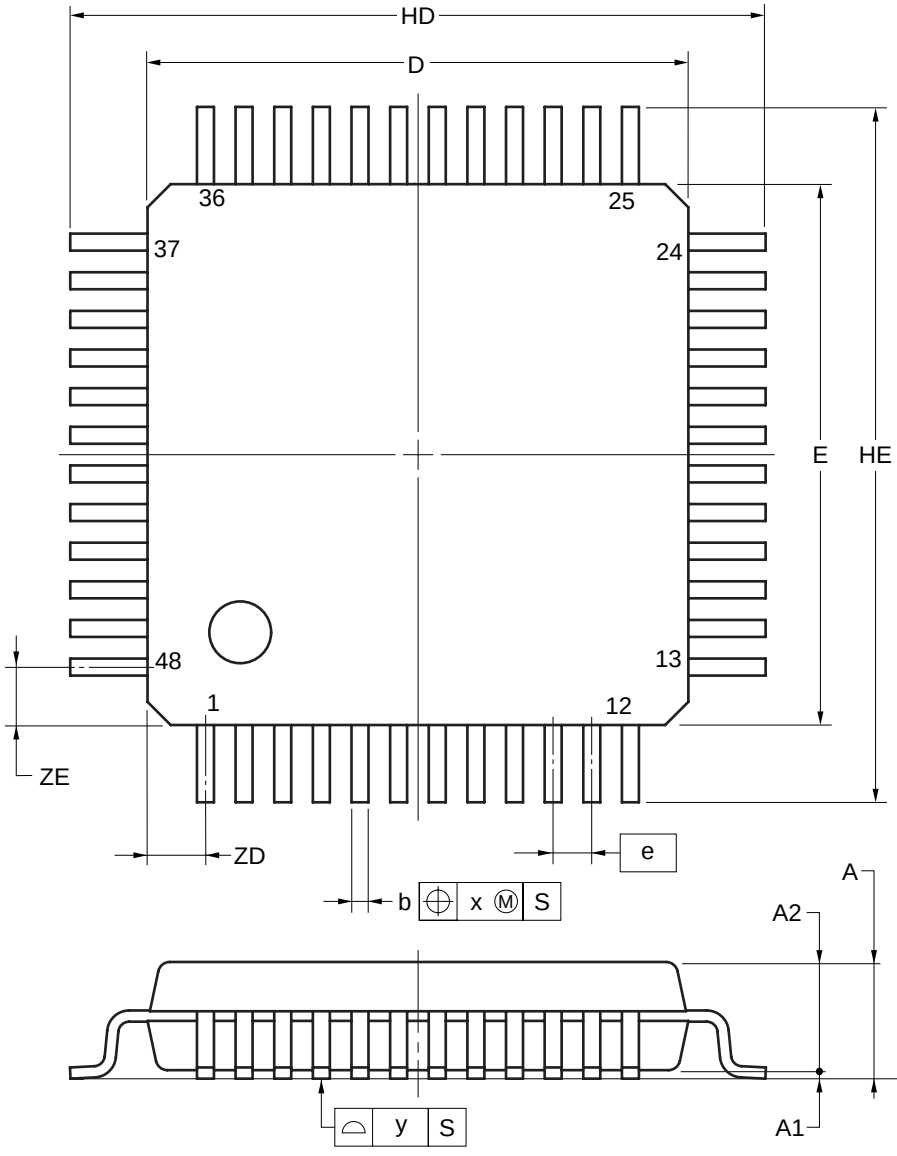
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P32, P100, P101, P112, P121 to P124, P140 to P143, P150 to P153		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P12, P13, P31, P33, P34, P40, P113, P120, $\overline{\text{RESET}}$, EXCLK		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P20 to P25	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
Input voltage, low	V_{IL1}	P32, P100, P101, P112, P121 to P124, P140 to P143, P150 to P153		0		0.3V_{DD}	V
	V_{IL2}	P12, P13, P31, P33, P34, P40, P113, P120, $\overline{\text{RESET}}$, EXCLK		0		0.2V_{DD}	V
	V_{IL3}	P20 to P25	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
Output voltage, high	V_{OH1}	P12, P13, P31 to P34, P40, P120	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	V_{DD} – 0.7			V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OH1} = –2.5 mA	V_{DD} – 0.5			V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OH1} = –1.0 mA	V_{DD} – 0.5			V
		P100, P101, P112, P113, P140 to P143, P150 to P153	I_{OH1} = –0.1 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P25	AV_{REF} = V_{DD}, I_{OH2} = –0.1 mA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P12, P13, P31 to P34, P40, P120	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 5.0 mA			0.7	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 2.0 mA			0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 1.0 mA			0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 0.5 mA			0.4	V
		P100, P101, P112, P113, P140 to P143, P150 to P153	I_{OL1} = 0.4 mA			0.4	V
	V_{OL2}	P20 to P25	AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA			0.4	V

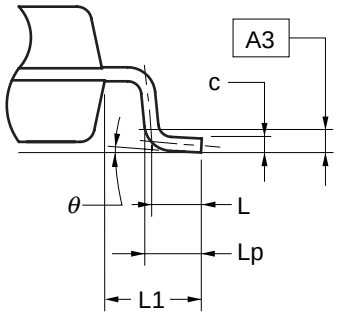
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The high-level and low-level input voltages of P122/EXCLK vary between the input port mode and external clock mode.

48-PIN PLASTIC LQFP (FINE PITCH) (7x7)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

P48GA-50-GAM

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.