



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 18x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk12dx256vlf5

Table of Contents

1 Ordering parts.....	3	5.3.2 General switching specifications.....	20
1.1 Determining valid orderable parts.....	3	5.4 Thermal specifications.....	20
2 Part identification.....	3	5.4.1 Thermal operating requirements.....	21
2.1 Description.....	3	5.4.2 Thermal attributes.....	21
2.2 Format.....	3	6 Peripheral operating requirements and behaviors.....	22
2.3 Fields.....	3	6.1 Core modules.....	22
2.4 Example.....	4	6.1.1 JTAG electricals.....	22
2.5 Small package marking.....	4	6.2 System modules.....	25
3 Terminology and guidelines.....	5	6.3 Clock modules.....	25
3.1 Definition: Operating requirement.....	5	6.3.1 MCG specifications.....	25
3.2 Definition: Operating behavior.....	5	6.3.2 Oscillator electrical specifications.....	27
3.3 Definition: Attribute.....	6	6.3.3 32 kHz oscillator electrical characteristics.....	29
3.4 Definition: Rating.....	6	6.4 Memories and memory interfaces.....	30
3.5 Result of exceeding a rating.....	7	6.4.1 Flash electrical specifications.....	30
3.6 Relationship between ratings and operating requirements.....	7	6.4.2 EzPort switching specifications.....	33
3.7 Guidelines for ratings and operating requirements.....	8	6.5 Security and integrity modules.....	34
3.8 Definition: Typical value.....	8	6.6 Analog.....	34
3.9 Typical value conditions.....	9	6.6.1 ADC electrical specifications.....	34
4 Ratings.....	9	6.6.2 CMP and 6-bit DAC electrical specifications.....	38
4.1 Thermal handling ratings.....	9	6.6.3 Voltage reference electrical specifications.....	41
4.2 Moisture handling ratings.....	10	6.7 Timers.....	42
4.3 ESD handling ratings.....	10	6.8 Communication interfaces.....	42
4.4 Voltage and current operating ratings.....	10	6.8.1 DSPI switching specifications (limited voltage range).....	42
5 General.....	10	6.8.2 DSPI switching specifications (full voltage range).....	44
5.1 AC electrical characteristics.....	11	6.8.3 I2C switching specifications.....	46
5.2 Nonswitching electrical specifications.....	11	6.8.4 UART switching specifications.....	46
5.2.1 Voltage and current operating requirements.....	11	6.8.5 Normal Run, Wait and Stop mode performance over the full operating voltage range.....	46
5.2.2 LVD and POR operating requirements.....	12	6.8.6 VLPR, VLPW, and VLPS mode performance over the full operating voltage range.....	48
5.2.3 Voltage and current operating behaviors.....	13	7 Dimensions.....	50
5.2.4 Power mode transition operating behaviors.....	13	7.1 Obtaining package dimensions.....	50
5.2.5 Power consumption operating behaviors.....	14	8 Pinout.....	50
5.2.6 EMC radiated emissions operating behaviors.....	18	8.1 K12 Signal Multiplexing and Pin Assignments.....	50
5.2.7 Designing with radiated emissions in mind.....	19	8.2 K12 Pinouts.....	53
5.2.8 Capacitance attributes.....	19	9 Revision History.....	54
5.3 Switching specifications.....	19		
5.3.1 Device clock specifications.....	19		

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

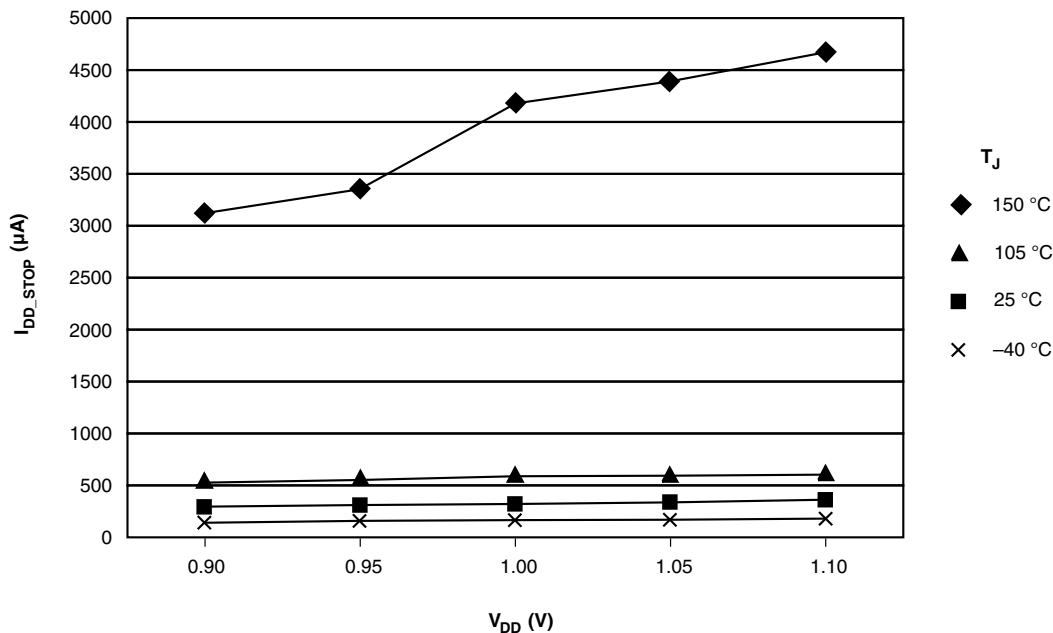
This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	°C
V _{DD}	3.3 V supply voltage	3.3	V

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	155	mA
V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3		V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
VREGIN	USB regulator input	-0.3	6.0	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{OH}	Output high voltage — high drive strength <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -9\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -3\text{ mA}$ 	$V_{DD} - 0.5$	—	V	
		$V_{DD} - 0.5$	—	V	
	Output high voltage — low drive strength <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -2\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -0.6\text{ mA}$ 	$V_{DD} - 0.5$	—	V	
		$V_{DD} - 0.5$	—	V	
I _{OHT}	Output high current total for all ports	—	100	mA	
V _{OL}	Output low voltage — high drive strength <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 9\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 3\text{ mA}$ 	—	0.5	V	
		—	0.5	V	
	Output low voltage — low drive strength <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 2\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 0.6\text{ mA}$ 	—	0.5	V	
		—	0.5	V	
I _{OLT}	Output low current total for all ports	—	100	mA	
I _{IN}	Input leakage current (per pin) <ul style="list-style-type: none"> • @ full temperature range • @ 25 °C 	—	1.0	μA	1
		—	0.1	μA	
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
I _{OZ}	Total Hi-Z (off-state) leakage current (all input pins)	—	4	μA	
R _{PU}	Internal pullup resistors	22	50	kΩ	2
R _{PD}	Internal pulldown resistors	22	50	kΩ	3

1. Tested by ganged leakage method
2. Measured at V_{input} = V_{SS}
3. Measured at V_{input} = V_{DD}

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and $VLLSx \rightarrow RUN$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. <ul style="list-style-type: none"> • $1.71 \text{ V} / (V_{DD} \text{ slew rate}) \leq 300 \mu\text{s}$ • $1.71 \text{ V} / (V_{DD} \text{ slew rate}) > 300 \mu\text{s}$ 	— —	300 $1.7 \text{ V} / (V_{DD} \text{ slew rate})$	μs	1
	• $VLLS0 \rightarrow RUN$	—	135	μs	
	• $VLLS1 \rightarrow RUN$	—	135	μs	
	• $VLLS2 \rightarrow RUN$	—	85	μs	
	• $VLLS3 \rightarrow RUN$	—	85	μs	
	• $LLS \rightarrow RUN$	—	6	μs	
	• $VLPS \rightarrow RUN$	—	5.2	μs	
	• $STOP \rightarrow RUN$	—	5.2	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash <ul style="list-style-type: none"> • @ 1.8 V • @ 3.0 V 	—	12.98	14	mA	2
		—	12.93	13.8	mA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V <ul style="list-style-type: none"> • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C 	—	1.03 1.92 4.03 17.43	1.8 7.5 15.9 28.7	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled <ul style="list-style-type: none"> • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C 	—	0.543 1.36 3.39 16.52	1.1 7.58 14.3 24.1	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled <ul style="list-style-type: none"> • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C 	—	0.359 1.03 2.87 15.20	0.95 6.8 15.4 25.3	μA	
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers at 3.0 V <ul style="list-style-type: none"> • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C 	—	0.91 1.1 1.5 4.3	1.1 1.35 1.85 5.7	μA	9

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
4. Max values are measured with CPU executing DSP instructions
5. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Includes 32 kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

3. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{OSC} = 12\text{ MHz}$ (crystal), $f_{SYS} = 48\text{ MHz}$, $f_{BUS} = 48\text{ MHz}$
4. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	50	MHz	
f_{BUS}	Bus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode ¹					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

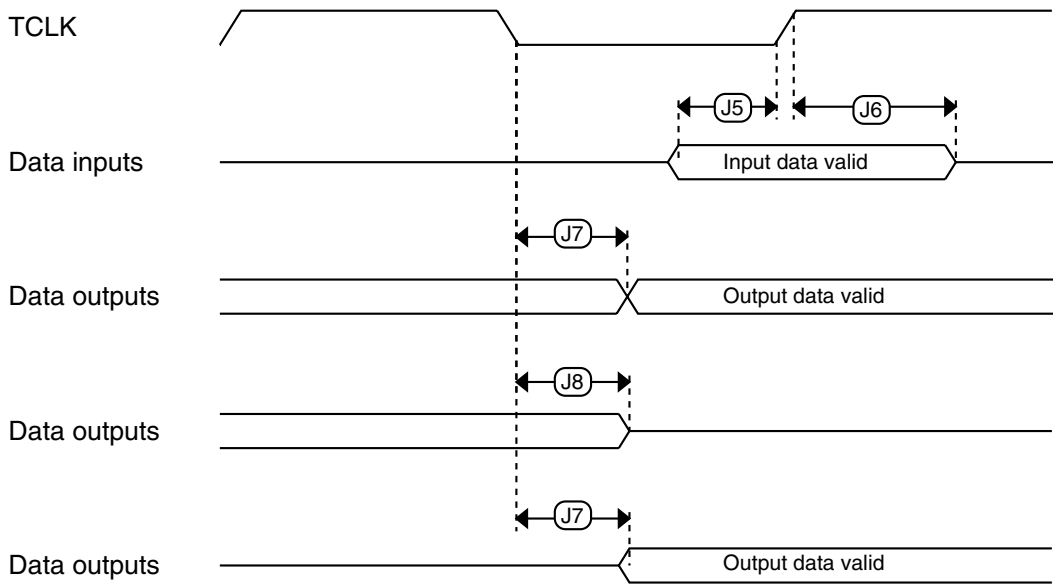


Figure 5. Boundary scan (JTAG) timing

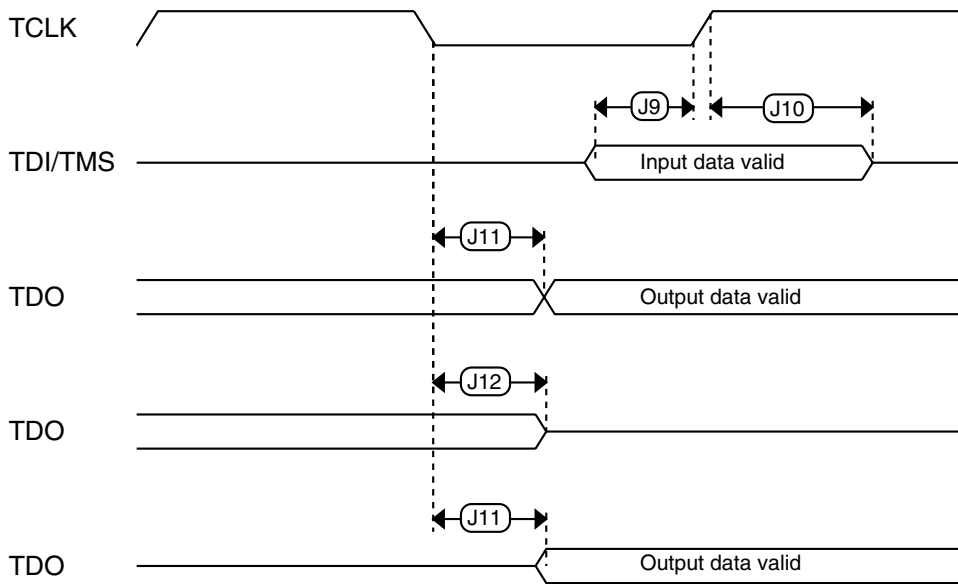


Figure 6. Test Access Port timing

Table 14. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll_ref})$	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. $2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

6.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	

Table continues on the next page...

6.4.1.2 Flash timing specifications — commands

Table 20. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk64k}$	Read 1s Block execution time	—	—	0.9	ms	
$t_{rd1blk256k}$	<ul style="list-style-type: none"> 64 KB data flash 256 KB program flash 	—	—	1.7	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
t_{rdsrc}	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	
$t_{ersblk64k}$	Erase Flash Block execution time	—	58	580	ms	2
$t_{ersblk256k}$	<ul style="list-style-type: none"> 64 KB data flash 256 KB program flash 	—	122	985	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
$t_{pgmsec512}$	Program Section execution time	—	2.4	—	ms	
$t_{pgmsec1k}$	<ul style="list-style-type: none"> 512 bytes flash 1 KB flash 	—	4.7	—	ms	
$t_{pgmsec2k}$	<ul style="list-style-type: none"> 2 KB flash 	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	μs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μs	
t_{ersall}	Erase All Blocks execution time	—	250	2000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
$t_{swapx01}$	Swap Control execution time	—	200	—	μs	
$t_{swapx02}$	<ul style="list-style-type: none"> control code 0x01 control code 0x02 	—	70	150	μs	
$t_{swapx04}$	<ul style="list-style-type: none"> control code 0x04 	—	70	150	μs	
$t_{swapx08}$	<ul style="list-style-type: none"> control code 0x08 	—	—	30	μs	
$t_{pgmpart64k}$	Program Partition for EEPROM execution time	—	138	—	ms	
$t_{setramff}$	Set FlexRAM Function execution time:	—	70	—	μs	
$t_{setram32k}$	<ul style="list-style-type: none"> Control Code 0xFF 32 KB EEPROM backup 	—	0.8	1.2	ms	
$t_{setram64k}$	<ul style="list-style-type: none"> 64 KB EEPROM backup 	—	1.3	1.9	ms	
Byte-write to FlexRAM for EEPROM operation						
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3

Table continues on the next page...

Table 20. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{\text{eewr8b32k}}$	Byte-write to FlexRAM execution time: • 32 KB EEPROM backup	—	385	1800	μs	
$t_{\text{eewr8b64k}}$	• 64 KB EEPROM backup		475	2000	μs	
Word-write to FlexRAM for EEPROM operation						
$t_{\text{eewr16bers}}$	Word-write to erased FlexRAM location execution time	—	175	260	μs	
$t_{\text{eewr16b32k}}$	Word-write to FlexRAM execution time: • 32 KB EEPROM backup	—	385	1800	μs	
$t_{\text{eewr16b64k}}$	• 64 KB EEPROM backup	—	475	2000	μs	
Longword-write to FlexRAM for EEPROM operation						
$t_{\text{eewr32bers}}$	Longword-write to erased FlexRAM location execution time	—	360	540	μs	
$t_{\text{eewr32b32k}}$	Longword-write to FlexRAM execution time: • 32 KB EEPROM backup	—	630	2050	μs	
$t_{\text{eewr32b64k}}$	• 64 KB EEPROM backup	—	810	2250	μs	

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash high voltage current behaviors

Table 21. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{\text{DD_PGM}}$	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
$I_{\text{DD_ERS}}$	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.4.1.4 Reliability specifications

Table 22. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
$t_{\text{nvrmretp10k}}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{\text{nvrmretp1k}}$	Data retention after up to 1 K cycles	20	100	—	years	
n_{nvmcycp}	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{\text{nvrmretd10k}}$	Data retention after up to 10 K cycles	5	50	—	years	

Table continues on the next page...

Table 22. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
$t_{\text{nvmretd1k}}$	Data retention after up to 1 K cycles	20	100	—	years	
n_{nvmcyed}	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{\text{nvmretee100}}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{\text{nvmretee10}}$	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
$n_{\text{nvmwree16}}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{\text{nvmwree128}}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{\text{nvmwree512}}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{\text{nvmwree4k}}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq \text{°C}$.
3. Write endurance represents the number of writes to each FlexRAM location at $-40\text{ °C} \leq T_j \leq \text{°C}$ influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.2 EzPort switching specifications

Table 23. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{\text{SYS}}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{\text{SYS}}/8$	MHz
EP2	$\overline{\text{EZP_CS}}$ negation to next $\overline{\text{EZP_CS}}$ assertion	$2 \times t_{\text{EZP_CK}}$	—	ns
EP3	$\overline{\text{EZP_CS}}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{\text{EZP_CS}}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	—	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{\text{EZP_CS}}$ negation to EZP_Q tri-state	—	12	ns

Table 24. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	ADC reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage	<ul style="list-style-type: none"> 16-bit differential mode All other modes 	V _{REFL} V _{REFL}	— —	31/32 * V _{REFH} V _{REFH}	V	
C _{ADIN}	Input capacitance	<ul style="list-style-type: none"> 16-bit mode 8-bit / 10-bit / 12-bit modes 	— —	8 4	10 5	pF	
R _{ADIN}	Input resistance		—	2	5	kΩ	
R _{AS}	Analog source resistance	13-bit / 12-bit modes f _{ADCK} < 4 MHz	—	—	5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C _{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C _{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

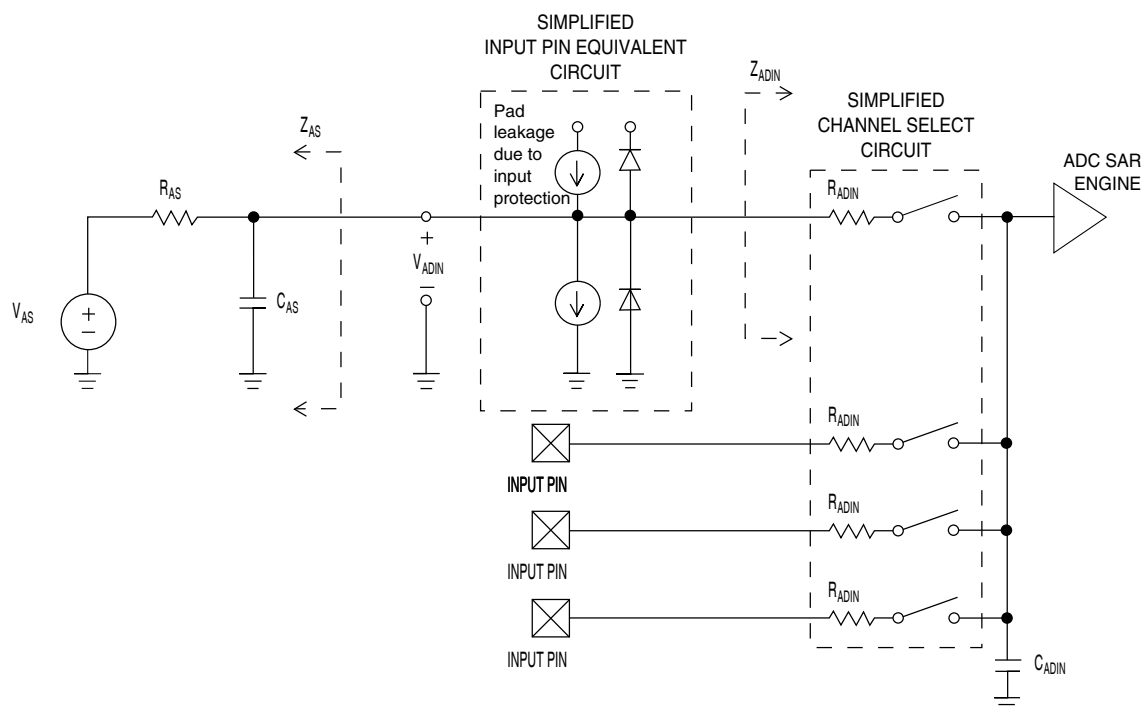


Figure 9. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics

Table 25. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	<ul style="list-style-type: none"> ADLPC = 1, ADHSC = 0 ADLPC = 1, ADHSC = 1 ADLPC = 0, ADHSC = 0 ADLPC = 0, ADHSC = 1 	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	<ul style="list-style-type: none"> 12-bit modes <12-bit modes 	— —	±4 ±1.4	±6.8 ±2.1	LSB ⁴	5
DNL	Differential non-linearity	<ul style="list-style-type: none"> 12-bit modes <12-bit modes 	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	<ul style="list-style-type: none"> 12-bit modes <12-bit modes 	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	<ul style="list-style-type: none"> 12-bit modes <12-bit modes 	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ 5

Table continues on the next page...

Peripheral operating requirements and behaviors

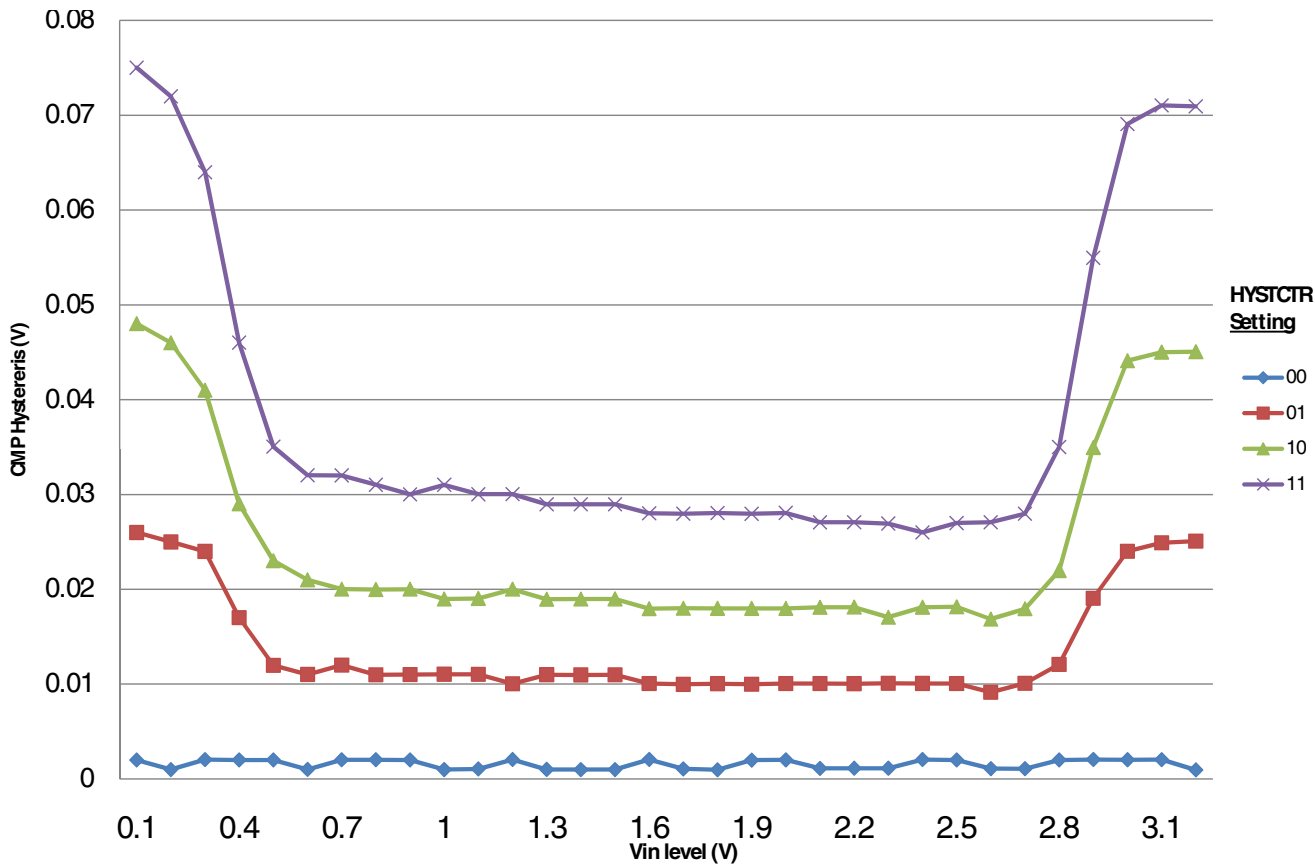
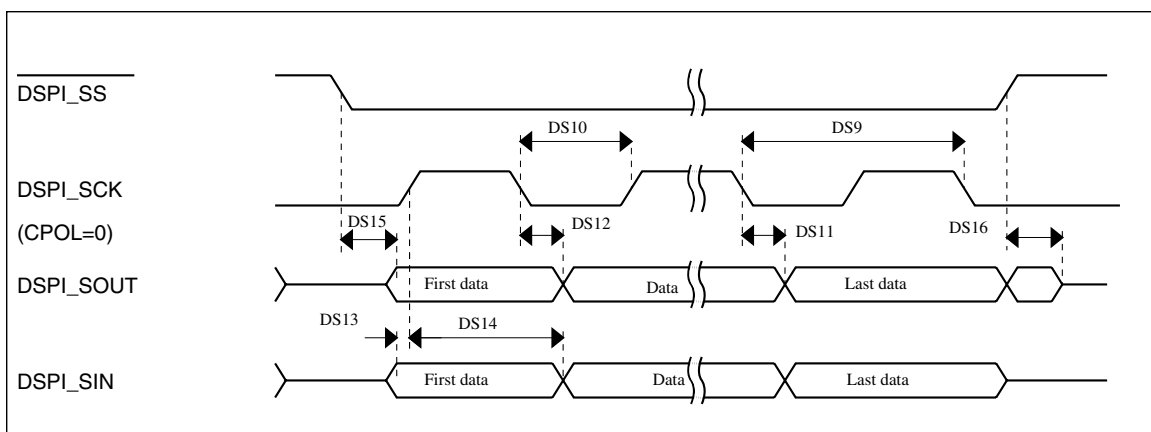


Figure 12. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

Table 32. Slave mode DSPI timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns </td
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	14	ns


Figure 15. DSPI classic SPI timing — slave mode

6.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 33. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	2

Table continues on the next page...

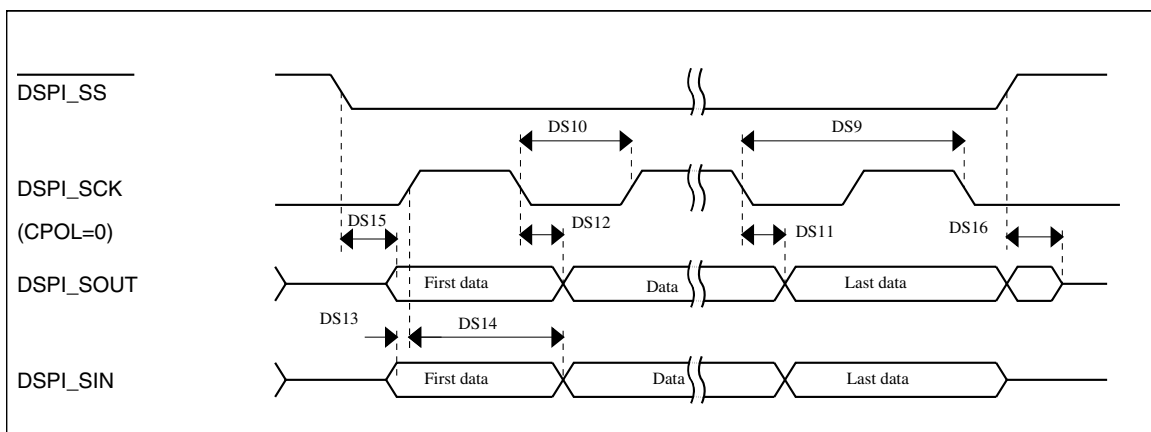


Figure 17. DSPI classic SPI timing — slave mode

6.8.3 I²C switching specifications

See [General switching specifications](#).

6.8.4 UART switching specifications

See [General switching specifications](#).

6.8.5 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 35. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns

Table continues on the next page...

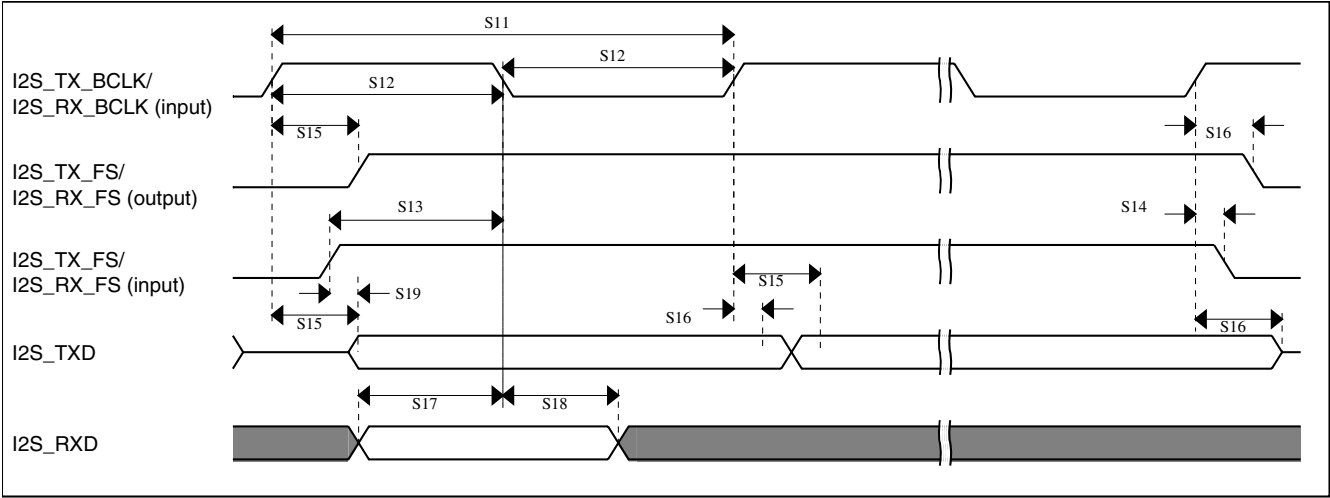


Figure 21. I2S/SAI timing — slave modes

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
48-pin LQFP	98ASH00962A

8 Pinout

8.1 K12 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

- The analog input signals ADC0_SE10, ADC0_SE11, ADC0_DP1, and ADC0_DM1 are available only for K11,

How to Reach Us:**Home Page:**

freescale.com

Web Support:

freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale, the Freescale logo, Energy Efficient Solutions logo, and Kinetis are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners. ARM and Cortex are the registered trademarks of ARM Limited.

© 2012-2013 Freescale Semiconductor, Inc.