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Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	4
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qd2vsc

Revision History

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<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	15 Sep 06	Initial public release
2	09 Jan 07	Added MC9S08QD2 information; added "M" temperature range (–40 °C to 125 °C); updated temperature sensor equation in the ADC chapter.
3	19 Nov. 07	Added S9S08QD4 and S9S08QD2 information for automotive applications. Revised "Accessing (read or write) any flash control register..." to "Writing any flash control register..." in Section 4.5.5 , "Access Errors."
4	9 Sep 08	Changed the SPMSC3 in Section 5.6 , "Low-Voltage Detect (LVD) System," and Section 5.6.4 , "Low-Voltage Warning (LVW)," to SPMSC2. Added V_{POR} to Table A-5 . Updated "How to Reach Us" information.
5	24 Nov 08	Revised dc injection current in Table A-5 .
6	14 Oct 10	Added T_{JMax} in the Table A-2 .

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MC9S08QD4 Series MCU Data Sheet, Rev. 6

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Chapter 1

Device Overview

1.1 Introduction

MC9S08QD4 series MCUs are members of the low-cost, high-performance HCS08 family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

1.2 Devices in the MC9S08QD4 Series

This data sheet covers:

- MC9S08QD4
- MC9S08QD2
- S9S08QD4
- S9S08QD2

NOTE

- The MC9S08QD4 and MC9S08QD2 devices are qualified for, and are intended to be used in, *consumer and industrial* applications.
- The S9S08QD4 and S9S08QD2 devices are qualified for, and are intended to be used in, *automotive* applications.

[Table 1-1](#) summarizes the features available in the MCUs.

Table 4-2. Direct-Page Register Summary (continued)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0x0017	APCTL1	—	—	—	—	ADPC3	ADPC2	ADPC1	ADPC0
0x0018	Reserved	—	—	—	—	—	—	—	—
0x0019	Reserved	—	—	—	—	—	—	—	—
0x001A– 0x001F	Reserved	—	—	—	—	—	—	—	—
0x0020	TPM2SC	TOF	TOIE	CPWMS	CLKSB	CLKSA	PS2	PS1	PS0
0x0021	TPM2CNTH	Bit 15	14	13	12	11	10	9	Bit 8
0x0022	TPM2CNTL	Bit 7	6	5	4	3	2	1	Bit 0
0x0023	TPM2MODH	Bit 15	14	13	12	11	10	9	Bit 8
0x0024	TPM2MODL	Bit 7	6	5	4	3	2	1	Bit 0
0x0025	TPM2C0SC	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	0	0
0x0026	TPM2C0VH	Bit 15	14	13	12	11	10	9	Bit 8
0x0027	TPM2C0VL	Bit 7	6	5	4	3	2	1	Bit 0
0x0028– 0x0037	Reserved	—	—	—	—	—	—	—	—
0x0038	ICSC1	0	CLKS	0	0	0	1	1	IREFSTEN
0x0039	ICSC2	BDIV		0	0	LP	0	0	0
0x003A	ICSTRM	TRIM							
0x003B	ICSSC	0	0	0	0	0	CLKST	0	FTRIM
0x003C	Reserved	—	—	—	—	—	—	—	—
0x0040	TPMSC	TOF	TOIE	CPWMS	CLKSB	CLKSA	PS2	PS1	PS0
0x0041	TPMCNTH	Bit 15	14	13	12	11	10	9	Bit 8
0x0042	TPMCNTL	Bit 7	6	5	4	3	2	1	Bit 0
0x0043	TPMMODH	Bit 15	14	13	12	11	10	9	Bit 8
0x0044	TPMMODL	Bit 7	6	5	4	3	2	1	Bit 0
0x0045	TPMC0SC	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	0	0
0x0046	TPMC0VH	Bit 15	14	13	12	11	10	9	Bit 8
0x0047	TPMC0VL	Bit 7	6	5	4	3	2	1	Bit 0
0x0048	TPMC1SC	CH1F	CH1IE	MS1B	MS1A	ELS1B	ELS1A	0	0
0x0049	TPMC1VH	Bit 15	14	13	12	11	10	9	Bit 8
0x004A	TPMC1VL	Bit 7	6	5	4	3	2	1	Bit 0
0x004B– 0x005F	Reserved	—	—	—	—	—	—	—	—

High-page registers, shown in [Table 4-3](#), are accessed much less often than other I/O and control registers so they have been located outside the direct addressable memory space, starting at 0x1800.

program and erase pulses. An integer number of these timing pulses is used by the command processor to complete a program or erase command.

Table 4-5 shows program and erase times. The bus clock frequency and FCDIV determine the frequency of FCLK (f_{FCLK}). The time for one cycle of FCLK is $t_{FCLK} = 1/f_{FCLK}$. The times are shown as a number of cycles of FCLK and as an absolute time for the case where $t_{FCLK} = 5 \mu s$. Program and erase times shown include overhead for the command state machine and enabling and disabling of program and erase voltages.

Table 4-5. Program and Erase Times

Parameter	Cycles of FCLK	Time if FCLK = 200 kHz
Byte program	9	45 μs
Byte program (burst)	4	20 μs ¹
Page erase	4000	20 ms
Mass erase	20,000	100 ms

¹ Excluding start/end overhead

4.5.3 Program and Erase Command Execution

The steps for executing any of the commands are listed below. The FCDIV register must be initialized and any error flags cleared before beginning command execution. The command execution steps are:

1. Write a data value to an address in the flash array. The address and data information from this write is latched into the flash interface. This write is a required first step in any command sequence. For erase and blank check commands, the value of the data is not important. For page erase commands, the address can be any address in the 512-byte page of flash to be erased. For mass erase and blank check commands, the address can be any address in the flash memory. Whole pages of 512 bytes are the smallest block of flash that can be erased.

NOTE

- A mass or page erase of the last page in flash will erase the factory programmed internal reference clock trim value.
 - Do not program any byte in the flash more than once after a successful erase operation. Reprogramming bits in a byte which is already programmed is not allowed without first erasing the page in which the byte resides or mass erasing the entire flash memory. Programming without first erasing may disturb data stored in the flash.
2. Write the command code for the desired command to FCMD. The five valid commands are blank check (0x05), byte program (0x20), burst program (0x25), page erase (0x40), and mass erase (0x41). The command code is latched into the command buffer.
 3. Write a 1 to the FCBEF bit in FSTAT to clear FCBEF and launch the command (including its address and data information).

A partial command sequence can be aborted manually by writing a 0 to FCBEF any time after the write to the memory array and before writing the 1 that clears FCBEF and launches the complete command.

Table 5-2. Vector Summary

Vector Priority	Vector Number	Address (High:Low)	Vector Name	Module	Source	Enable	Description	
Lower Higher	31 through 24	0xFFC0:FFC1 through 0xFFCE:FFCF	Unused Vector Space (available for user program)					
	23	0xFFD0:FFD1	Vrti	System control	RTIF	RTIE	Real-time interrupt	
	22	0xFFD2:FFD3	—	—	—	—	—	
	21	0xFFD4:FFD5	—	—	—	—	—	
	20	0xFFD6:FFD7	—	—	—	—	—	
	19	0xFFD8:FFD9	Vadc1	ADC1	COCO	AIEN	ADC1	
	18	0xFFDA:FFDB	Vkeyboard1	KBI1	KBF	KBIE	Keyboard pins	
	17	0xFFDC:FFDD	—	—	—	—	—	
	16	0xFFDE:FFDF	—	—	—	—	—	
	15	0xFFE0:FFE1	—	—	—	—	—	
	14	0xFFE2:FFE3	—	—	—	—	—	
	13	0xFFE4:FFE5	—	—	—	—	—	
	12	0xFFE6:FFE7	—	—	—	—	—	
	11	0xFFE8:FFE9	—	—	—	—	—	
	10	0xFFEA:FFEB	Vtpm2ovf	TPM2	TOF	TOIE	TPM2 overflow	
	9	0xFFEC:FFED	—	—	—	—	—	
	8	0xFFEE:FFEF	Vtpm2ch0	TPM2	CH0F	CH0IE	TPM2 channel 0	
	7	0xFFF0:FFF1	Vtpm1ovf	TPM1	TOF	TOIE	TPM1 overflow	
	6	0xFFF2:FFF3	Vtpm1ch1	TPM1	CH1F	CH1IE	TPM1 channel 1	
	5	0xFFF4:FFF5	Vtpm1ch0	TPM1	CH0F	CH0IE	TPM1 channel 0	
	4	0xFFF6:FFF7	—	—	—	—	—	
	3	0xFFF8:FFF9	Virq	IRQ	IRRQF	IRQIE	IRQ pin	
	2	0xFFFA:FFFB	Vlvd	System control	LVDF	LVDIE	Low voltage detect	
	1	0xFFFC:FFFD	Vswi	CPU	SWI Instruction	—	Software interrupt	
	0	0xFFFE:FFFF	Vreset	System control	COP LVD RESET pin Illegal opcode Illegal address POR	COPE LVDRE RSTPE — — —	Watchdog timer Low-voltage detect External pin Illegal opcode Illegal address power-on-reset	

5.6 Low-Voltage Detect (LVD) System

The MC9S08QD4 series includes a system to protect against low voltage conditions in order to protect memory contents and control MCU system states during supply voltage variations. The system is comprised of a power-on reset (POR) circuit and an LVD circuit with a user selectable trip voltage, either high (V_{LVDH}) or low (V_{LVDL}). The LVD circuit is enabled when LVDE in SPMSC1 is high and the trip voltage is selected by LVDV in SPMSC2. The LVD is disabled upon entering any of the stop modes unless LVDSE is set in SPMSC1. If LVDSE and LVDE are both set, then the MCU cannot enter stop1 or stop2, and the current consumption in stop3 with the LVD enabled will be greater.

- In stop1 mode, all internal registers including parallel I/O control and data registers are powered off. Each of the pins assumes its default reset state (output buffer and internal pullup disabled). Upon exit from stop1, all pins must be re-configured the same as if the MCU had been reset.
- Stop2 mode is a partial power-down mode, whereby latches maintain the pin state as before the STOP instruction was executed. CPU register status and the state of I/O registers must be saved in RAM before the STOP instruction is executed to place the MCU in stop2 mode. Upon recovery from stop2 mode, before accessing any I/O, the user must examine the state of the PPDF bit in the SPMSC2 register. If the PPDF bit is 0, I/O must be initialized as if a power on reset had occurred. If the PPDF bit is 1, I/O data previously stored in RAM, before the STOP instruction was executed, peripherals previously enabled will require being initialized and restored to their pre-stop condition. The user must then write a 1 to the PPDACK bit in the SPMSC2 register. Access of pins is now permitted again in the user’s application program.
- In stop3 mode, all pin states are maintained because internal logic stays powered up. Upon recovery, all pin functions are the same as before entering stop3.

6.4 Parallel I/O Registers

6.4.1 Port A Registers

This section provides information about the registers associated with the parallel I/O ports.

Refer to tables in [Chapter 4, “Memory Map and Register Definition,”](#) for the absolute address assignments for all parallel I/O. This section refers to registers and control bits only by their names. A Freescale Semiconductor-provided equate or header file normally is used to translate these names into the appropriate absolute addresses.

6.4.1.1 Port A Data (PTAD)

	7	6	5	4	3	2	1	0
R	0	0	PTAD5 ¹	PTAD4 ²	PTAD3	PTAD2	PTAD1	PTAD0
W								
Reset:	0	0	0	0	0	0	0	0

¹ Reads of bit PTAD5 always return the pin value of PTA5, regardless of the value stored in bit PTADD5.

² Reads of bit PTAD4 always return the contents of PTAD4, regardless of the value stored in bit PTADD4.

Figure 6-2. Port A Data Register (PTAD)

Table 7-2. Instruction Set Summary (Sheet 2 of 9)

Source Form	Operation	Address Mode	Object Code	Cycles	Cyc-by-Cyc Details	Affect on CCR				
						VH	I	N	Z	C
BCLR <i>n,opr8a</i>	Clear Bit <i>n</i> in Memory ($M_n \leftarrow 0$)	DIR (b0)	11 dd	5	rfwpp	--	-	-	-	-
		DIR (b1)	13 dd	5	rfwpp					
		DIR (b2)	15 dd	5	rfwpp					
		DIR (b3)	17 dd	5	rfwpp					
		DIR (b4)	19 dd	5	rfwpp					
		DIR (b5)	1B dd	5	rfwpp					
		DIR (b6)	1D dd	5	rfwpp					
		DIR (b7)	1F dd	5	rfwpp					
BCS <i>rel</i>	Branch if Carry Bit Set (if C = 1) (Same as BLO)	REL	25 rr	3	ppp	--	-	-	-	-
BEQ <i>rel</i>	Branch if Equal (if Z = 1)	REL	27 rr	3	ppp	--	-	-	-	-
BGE <i>rel</i>	Branch if Greater Than or Equal To (if $N \oplus V = 0$) (Signed)	REL	90 rr	3	ppp	--	-	-	-	-
BGND	Enter active background if ENBDM=1 Waits for and processes BDM commands until GO, TRACE1, or TAGGO	INH	82	5+	fp...ppp	--	-	-	-	-
BGT <i>rel</i>	Branch if Greater Than (if $Z \mid (N \oplus V) = 0$) (Signed)	REL	92 rr	3	ppp	--	-	-	-	-
BHCC <i>rel</i>	Branch if Half Carry Bit Clear (if H = 0)	REL	28 rr	3	ppp	--	-	-	-	-
BHCS <i>rel</i>	Branch if Half Carry Bit Set (if H = 1)	REL	29 rr	3	ppp	--	-	-	-	-
BHI <i>rel</i>	Branch if Higher (if $C \mid Z = 0$)	REL	22 rr	3	ppp	--	-	-	-	-
BHS <i>rel</i>	Branch if Higher or Same (if C = 0) (Same as BCC)	REL	24 rr	3	ppp	--	-	-	-	-
BIH <i>rel</i>	Branch if IRQ Pin High (if IRQ pin = 1)	REL	2F rr	3	ppp	--	-	-	-	-
BIL <i>rel</i>	Branch if IRQ Pin Low (if IRQ pin = 0)	REL	2E rr	3	ppp	--	-	-	-	-
BIT # <i>opr8i</i> BIT <i>opr8a</i> BIT <i>opr16a</i> BIT <i>opr16,X</i> BIT <i>opr8,X</i> BIT <i>,X</i> BIT <i>opr16,SP</i> BIT <i>opr8,SP</i>	Bit Test (A) & (M) (CCR Updated but Operands Not Changed)	IMM DIR EXT IX2 IX1 IX SP2 SP1	A5 ii B5 dd C5 hh ll D5 ee ff E5 ff F5 9E D5 ee ff 9E E5 ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	0-	-	↑	↓	-
BLE <i>rel</i>	Branch if Less Than or Equal To (if $Z \mid (N \oplus V) = 1$) (Signed)	REL	93 rr	3	ppp	--	-	-	-	-
BLO <i>rel</i>	Branch if Lower (if C = 1) (Same as BCS)	REL	25 rr	3	ppp	--	-	-	-	-
BLS <i>rel</i>	Branch if Lower or Same (if $C \mid Z = 1$)	REL	23 rr	3	ppp	--	-	-	-	-
BLT <i>rel</i>	Branch if Less Than (if $N \oplus V = 1$) (Signed)	REL	91 rr	3	ppp	--	-	-	-	-
BMC <i>rel</i>	Branch if Interrupt Mask Clear (if I = 0)	REL	2C rr	3	ppp	--	-	-	-	-
BMI <i>rel</i>	Branch if Minus (if N = 1)	REL	2B rr	3	ppp	--	-	-	-	-
BMS <i>rel</i>	Branch if Interrupt Mask Set (if I = 1)	REL	2D rr	3	ppp	--	-	-	-	-
BNE <i>rel</i>	Branch if Not Equal (if Z = 0)	REL	26 rr	3	ppp	--	-	-	-	-
BPL <i>rel</i>	Branch if Plus (if N = 0)	REL	2A rr	3	ppp	--	-	-	-	-

Table 7-2. Instruction Set Summary (Sheet 4 of 9)

Source Form	Operation	Address Mode	Object Code	Cycles	Cyc-by-Cyc Details	Affect on CCR				
						VH	I	N	Z	C
CMP #opr8i CMP opr8a CMP opr16a CMP oprx16,X CMP oprx8,X CMP ,X CMP oprx16,SP CMP oprx8,SP	Compare Accumulator with Memory $A - M$ (CCR Updated But Operands Not Changed)	IMM DIR EXT IX2 IX1 IX SP2 SP1	A1 ii B1 dd C1 hh ll D1 ee ff E1 ff F1 9E D1 ee ff 9E E1 ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	↓- ↓- ↓- ↓- ↓- ↓- ↓- ↓-	- - - - - - - -	↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑	↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓
COM opr8a COMA COMX COM oprx8,X COM ,X COM oprx8,SP	Complement (One's Complement) $M \leftarrow (\overline{M}) = \$FF - (M)$ $A \leftarrow (\overline{A}) = \$FF - (A)$ $X \leftarrow (\overline{X}) = \$FF - (X)$ $M \leftarrow (\overline{M}) = \$FF - (M)$ $M \leftarrow (\overline{M}) = \$FF - (M)$ $M \leftarrow (\overline{M}) = \$FF - (M)$	DIR INH INH IX1 IX SP1	33 dd 43 53 63 ff 73 9E 63 ff	5 1 1 5 4 6	rfwpp p p rfwpp rfwpp prfwpp	0- 0- 0- 0- 0- 0- 0- 0-	- - - - - - - -	↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑	↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	1 1 1 1 1 1
CPHX opr16a CPHX #opr16i CPHX opr8a CPHX oprx8,SP	Compare Index Register (H:X) with Memory $(H:X) - (M:M + \$0001)$ (CCR Updated But Operands Not Changed)	EXT IMM DIR SP1	3E hh ll 65 jj kk 75 dd 9E F3 ff	6 3 5 6	prrfpp ppp rrfpp prrfpp	↓- ↓- ↓- ↓-	- - - -	↑ ↑ ↑ ↑	↓ ↓ ↓ ↓	
CPX #opr8i CPX opr8a CPX opr16a CPX oprx16,X CPX oprx8,X CPX ,X CPX oprx16,SP CPX oprx8,SP	Compare X (Index Register Low) with Memory $X - M$ (CCR Updated But Operands Not Changed)	IMM DIR EXT IX2 IX1 IX SP2 SP1	A3 ii B3 dd C3 hh ll D3 ee ff E3 ff F3 9E D3 ee ff 9E E3 ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	↓- ↓- ↓- ↓- ↓- ↓- ↓- ↓-	- - - - - - - -	↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑	↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	
DAA	Decimal Adjust Accumulator After ADD or ADC of BCD Values	INH	72	1	p	U-	-	↑	↓	↑
DBNZ opr8a,rel DBNZA rel DBNZX rel DBNZ oprx8,X,rel DBNZ ,X,rel DBNZ oprx8,SP,rel	Decrement A, X, or M and Branch if Not Zero (if (result) ≠ 0) DBNZX Affects X Not H	DIR INH INH IX1 IX SP1	3B dd rr 4B rr 5B rr 6B ff rr 7B rr 9E 6B ff rr	7 4 4 7 6 8	rfwpppp fppp fppp rfwpppp rfwppp prfwpppp	-- -- -- -- -- --	- - - - - -	↑ ↑ ↑ ↑ ↑ ↑	↓ ↓ ↓ ↓ ↓ ↓	
DEC opr8a DECA DECX DEC oprx8,X DEC ,X DEC oprx8,SP	Decrement $M \leftarrow (M) - \$01$ $A \leftarrow (A) - \$01$ $X \leftarrow (X) - \$01$ $M \leftarrow (M) - \$01$ $M \leftarrow (M) - \$01$ $M \leftarrow (M) - \$01$	DIR INH INH IX1 IX SP1	3A dd 4A 5A 6A ff 7A 9E 6A ff	5 1 1 5 4 6	rfwpp p p rfwpp rfwpp prfwpp	↓- ↓- ↓- ↓- ↓- ↓-	- - - - - -	↑ ↑ ↑ ↑ ↑ ↑	↓ ↓ ↓ ↓ ↓ ↓	
DIV	Divide $A \leftarrow (H:A) \div (X)$; $H \leftarrow \text{Remainder}$	INH	52	6	fffffp	--	-	↑	↓	↑
EOR #opr8i EOR opr8a EOR opr16a EOR oprx16,X EOR oprx8,X EOR ,X EOR oprx16,SP EOR oprx8,SP	Exclusive OR Memory with Accumulator $A \leftarrow (A \oplus M)$	IMM DIR EXT IX2 IX1 IX SP2 SP1	A8 ii B8 dd C8 hh ll D8 ee ff E8 ff F8 9E D8 ee ff 9E E8 ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	0- 0- 0- 0- 0- 0- 0- 0-	- - - - - - - -	↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑	↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	

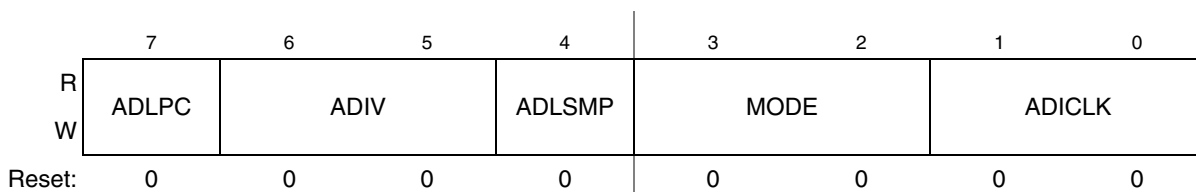


Figure 8-10. Configuration Register (ADCCFG)

Table 8-5. ADCCFG Register Field Descriptions

Field	Description
7 ADLPC	Low Power Configuration — ADLPC controls the speed and power configuration of the successive approximation converter. This is used to optimize power consumption when higher sample rates are not required. 0 High speed configuration 1 Low power configuration: {FC31}The power is reduced at the expense of maximum clock speed.
6:5 ADIV	Clock Divide Select — ADIV select the divide ratio used by the ADC to generate the internal clock ADCK. Table 8-6 shows the available clock configurations.
4 ADLSMP	Long Sample Time Configuration — ADLSMP selects between long and short sample time. This adjusts the sample period to allow higher impedance inputs to be accurately sampled or to maximize conversion speed for lower impedance inputs. Longer sample times can also be used to lower overall power consumption when continuous conversions are enabled if high conversion rates are not required. 0 Short sample time 1 Long sample time
3:2 MODE	Conversion Mode Selection — MODE bits are used to select between 10- or 8-bit operation. See Table 8-7 .
1:0 ADICLK	Input Clock Select — ADICLK bits select the input clock source to generate the internal clock ADCK. See Table 8-8 .

Table 8-6. Clock Divide Select

ADIV	Divide Ratio	Clock Rate
00	1	Input clock
01	2	Input clock ÷ 2
10	4	Input clock ÷ 4
11	8	Input clock ÷ 8

Table 8-7. Conversion Modes

MODE	Mode Description
00	8-bit conversion (N=8)
01	Reserved
10	10-bit conversion (N=10)
11	Reserved

result of the conversion is transferred to ADCRH and ADCRL upon completion of the conversion algorithm.

If the bus frequency is less than the f_{ADCK} frequency, precise sample time for continuous conversions cannot be guaranteed when short sample is enabled (ADLSMP=0). If the bus frequency is less than 1/11th of the f_{ADCK} frequency, precise sample time for continuous conversions cannot be guaranteed when long sample is enabled (ADLSMP=1).

The maximum total conversion time for different conditions is summarized in [Table 8-12](#).

Table 8-12. Total Conversion Time vs. Control Conditions

Conversion Type	ADICLK	ADLSMP	Max Total Conversion Time
Single or first continuous 8-bit	0x, 10	0	20 ADCK cycles + 5 bus clock cycles
Single or first continuous 10-bit	0x, 10	0	23 ADCK cycles + 5 bus clock cycles
Single or first continuous 8-bit	0x, 10	1	40 ADCK cycles + 5 bus clock cycles
Single or first continuous 10-bit	0x, 10	1	43 ADCK cycles + 5 bus clock cycles
Single or first continuous 8-bit	11	0	5 μ s + 20 ADCK + 5 bus clock cycles
Single or first continuous 10-bit	11	0	5 μ s + 23 ADCK + 5 bus clock cycles
Single or first continuous 8-bit	11	1	5 μ s + 40 ADCK + 5 bus clock cycles
Single or first continuous 10-bit	11	1	5 μ s + 43 ADCK + 5 bus clock cycles
Subsequent continuous 8-bit; $f_{BUS} \geq f_{ADCK}$	xx	0	17 ADCK cycles
Subsequent continuous 10-bit; $f_{BUS} \geq f_{ADCK}$	xx	0	20 ADCK cycles
Subsequent continuous 8-bit; $f_{BUS} \geq f_{ADCK}/11$	xx	1	37 ADCK cycles
Subsequent continuous 10-bit; $f_{BUS} \geq f_{ADCK}/11$	xx	1	40 ADCK cycles

The maximum total conversion time is determined by the clock source chosen and the divide ratio selected. The clock source is selectable by the ADICLK bits, and the divide ratio is specified by the ADIV bits. For example, in 10-bit mode, with the bus clock selected as the input clock source, the input clock divide-by-1 ratio selected, and a bus frequency of 8 MHz, then the conversion time for a single conversion is:

$$\text{Conversion time} = \frac{23 \text{ ADCK cyc}}{8 \text{ MHz}/1} + \frac{5 \text{ bus cyc}}{8 \text{ MHz}} = 3.5 \mu\text{s}$$

$$\text{Number of bus cycles} = 3.5 \mu\text{s} \times 8 \text{ MHz} = 28 \text{ cycles}$$

NOTE

The ADCK frequency must be between f_{ADCK} minimum and f_{ADCK} maximum to meet ADC specifications.



Figure 8-14. Initialization Flowchart for Example

8.6 Application Information

This section contains information for using the ADC module in applications. The ADC has been designed to be integrated into a microcontroller for use in embedded control applications requiring an A/D converter.

8.6.1 External Pins and Routing

The following sections discuss the external pins associated with the ADC module and how they must be used for best results.

8.6.1.1 Analog Supply Pins

The ADC module has analog power and ground supplies (V_{DDAD} and V_{SSAD}) which are available as separate pins on some devices. On other devices, V_{SSAD} is shared on the same pin as the MCU digital V_{SS} , and on others, both V_{SSAD} and V_{DDAD} are shared with the MCU digital supply pins. In these cases, there are separate pads for the analog supplies which are bonded to the same pin as the corresponding digital supply so that some degree of isolation between the supplies is maintained.

When available on a separate pin, both V_{DDAD} and V_{SSAD} must be connected to the same voltage potential as their corresponding MCU digital supply (V_{DD} and V_{SS}) and must be routed carefully for maximum noise immunity and bypass capacitors placed as near as possible to the package.

9.1.2 Features

Key features of the ICS module are:

- Frequency-locked loop (FLL) is trimmable for accuracy
 - 0.2% resolution using internal 32 kHz reference
 - 2% deviation over voltage and temperature using internal 32 kHz reference
- Internal or external reference clocks up to 5 MHz can be used to control the FLL
 - 3 bit select for reference divider is provided
- Internal reference clock has 9 trim bits available
- Internal or external reference clocks can be selected as the clock source for the MCU
- Whichever clock is selected as the source can be divided down
 - 2 bit select for clock divider is provided
 - Allowable dividers are: 1, 2, 4, 8
 - BDC clock is provided as a constant divide by 2 of the DCO output
- Control signals for a low power oscillator as the external reference clock are provided
 - HGO, RANGE, EREFS, ERCLKEN, EREFSTEN
- FLL engaged internal mode is automatically selected out of reset

9.1.3 Modes of Operation

There are seven modes of operation for the ICS: FEI, FEE, FBI, FBILP, FBE, FBELP, and stop.

9.1.3.1 FLL Engaged Internal (FEI)

In FLL engaged internal mode, which is the default mode, the ICS supplies a clock derived from the FLL which is controlled by the internal reference clock. The BDC clock is supplied from the FLL.

9.1.3.2 FLL Engaged External (FEE)

In FLL engaged external mode, the ICS supplies a clock derived from the FLL which is controlled by an external reference clock. The BDC clock is supplied from the FLL.

9.1.3.3 FLL Bypassed Internal (FBI)

In FLL bypassed internal mode, the FLL is enabled and controlled by the internal reference clock, but is bypassed. The ICS supplies a clock derived from the internal reference clock. The BDC clock is supplied from the FLL.

9.1.3.4 FLL Bypassed Internal Low Power (FBILP)

In FLL bypassed internal low power mode, the FLL is disabled and bypassed, and the ICS supplies a clock derived from the internal reference clock. The BDC clock is not available.

9.3.2 ICS Control Register 2 (ICSC2)

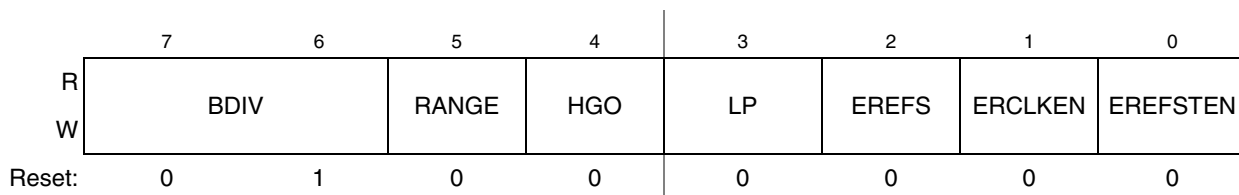


Figure 9-4. ICS Control Register 2 (ICSC2)

Table 9-2. ICS Control Register 2 Field Descriptions

Field	Description
7:6 BDIV	Bus Frequency Divider — Selects the amount to divide down the clock source selected by the CLKS bits. This controls the bus frequency. 00 Encoding 0 — Divides selected clock by 1 01 Encoding 1 — Divides selected clock by 2 (reset default) 10 Encoding 2 — Divides selected clock by 4 11 Encoding 3 — Divides selected clock by 8
5 RANGE	Frequency Range Select — Selects the frequency range for the external oscillator. 1 High frequency range selected for the external oscillator 0 Low frequency range selected for the external oscillator
4 HGO	High Gain Oscillator Select — The HGO bit controls the external oscillator mode of operation. 1 Configure external oscillator for high gain operation 0 Configure external oscillator for low power operation
3 LP	Low Power Select — The LP bit controls whether the FLL is disabled in FLL bypassed modes. 1 FLL is disabled in bypass modes unless BDM is active 0 FLL is not disabled in bypass mode
2 EREFs	External Reference Select — The EREFs bit selects the source for the external reference clock. 1 Oscillator requested 0 External Clock Source requested
1 ERCLKEN	External Reference Enable — The ERCLKEN bit enables the external reference clock for use as ICsERCLK. 1 ICsERCLK active 0 ICsERCLK inactive
0 EREFSTEN	External Reference Stop Enable — The EREFSTEN bit controls whether or not the external reference clock remains enabled when the ICS enters stop mode. 1 External reference clock stays enabled in stop if ERCLKEN is set or if ICS is in FEE, FBE, or FBELP mode before entering stop 0 External reference clock is disabled in stop

9.4.7 Fixed Frequency Clock

The ICS presents the divided FLL reference clock as ICSFFCLK for use as an additional clock source for peripheral modules. The ICS provides an output signal (ICSFFE) which indicates when the ICS is providing ICSOUT frequencies four times or greater than the divided FLL reference clock (ICSFFCLK). In FLL engaged mode (FEI and FEE) this is always true and ICSFFE is always high. In ICS bypass modes, ICSFFE will get asserted for the following combinations of BDIV and RDIV values:

- BDIV=00 (divide by 1), RDIV ≥ 010
- BDIV=01 (divide by 2), RDIV ≥ 011
- BDIV=10 (divide by 4), RDIV ≥ 100
- BDIV=11 (divide by 8), RDIV ≥ 101

9.5 Module Initialization

This section describes how to initialize and configure the ICS module. The following sections contain two initialization examples.

9.5.1 ICS Module Initialization Sequence

The ICS comes out of POR configured for FEI mode with the BDIV set for divide-by 2. The internal reference will stabilize in t_{IRST} microseconds before the FLL can acquire lock. As soon as the internal reference is stable, the FLL will acquire lock in $t_{Acquire}$ milliseconds.

Upon POR, the internal reference will require trimming to guarantee an accurate clock. Freescale recommends using FLASH location 0xFFAE for storing the fine trim bit, FTRIM in the ICSSC register, and 0xFFAF for storing the 8-bit trim value for the ICSTRM register. The MCU will not automatically copy the values in these FLASH locations to the respective registers. Therefore, user code must copy these values from FLASH to the registers.

NOTE

The BDIV value must not be changed to divide-by 1 without first trimming the internal reference. Failure to do so could result in the MCU running out of specification.

9.5.1.1 Initialization Sequence, Internal Clock Mode to External Clock Mode

To change from FEI or FBI clock modes to FEE or FBE clock modes, follow this procedure:

1. Enable the external clock source by setting the appropriate bits in ICSC2.
 - If FBE will be the selected mode, also set the LP bit at this time to minimize power consumption.
2. If necessary, wait for the external clock source to stabilize. Typical crystal startup times are given in Electrical Characteristics appendix. If EREFS is set in step 1, then the OSCINIT bit will set as soon as the oscillator has completed the initialization cycles.
3. Write to ICSC1 to select the clock mode.

All TPM channels are programmable independently as input capture, output compare, or buffered edge-aligned PWM channels.

11.2 External Signal Description

When any pin associated with the timer is configured as a timer input, a passive pullup can be enabled. After reset, the TPM modules are disabled and all pins default to general-purpose inputs with the passive pullups disabled.

11.2.1 External TPM Clock Sources

When control bits CLKSB:CLKSA in the timer status and control register are set to 1:1, the prescaler and consequently the 16-bit counter for TPMx are driven by an external clock source, TPMxCLK, connected to an I/O pin. A synchronizer is needed between the external clock and the rest of the TPM. This synchronizer is clocked by the bus clock so the frequency of the external source must be less than one-half the frequency of the bus rate clock. The upper frequency limit for this external clock source is specified to be one-fourth the bus frequency to conservatively accommodate duty cycle and phase-locked loop (PLL) or frequency-locked loop (FLL) frequency jitter effects.

On some devices the external clock input is shared with one of the TPM channels. When a TPM channel is shared as the external clock input, the associated TPM channel cannot use the pin. (The channel can still be used in output compare mode as a software timer.) Also, if one of the TPM channels is used as the external clock input, the corresponding ELSnB:ELSnA control bits must be set to 0:0 so the channel is not trying to use the same pin.

11.2.2 TPMxCHn — TPMx Channel n I/O Pins

Each TPM channel is associated with an I/O pin on the MCU. The function of this pin depends on the configuration of the channel. In some cases, no pin function is needed so the pin reverts to being controlled by general-purpose I/O controls. When a timer has control of a port pin, the port data and data direction registers do not affect the related pin(s). See the [Pins and Connections](#) chapter for additional information about shared pin functions.

11.3 Register Definition

The TPM includes:

- An 8-bit status and control register (TPMxSC)
- A 16-bit counter (TPMxCNTH:TPMxCNTL)
- A 16-bit modulo register (TPMxMODH:TPMxMODL)

Each timer channel has:

- An 8-bit status and control register (TPMxCnSC)
- A 16-bit channel value register (TPMxCnVH:TPMxCnVL)

Refer to the direct-page register summary in the [Memory](#) chapter of this data sheet for the absolute address assignments for all TPM registers. This section refers to registers and control bits only by their names. A

When center-aligned PWM operation is specified, the counter counts upward from 0x0000 through its terminal count and then counts downward to 0x0000 where it returns to up-counting. Both 0x0000 and the terminal count value (value in TPMxMODH:TPMxMODL) are normal length counts (one timer clock period long).

An interrupt flag and enable are associated with the main 16-bit counter. The timer overflow flag (TOF) is a software-accessible indication that the timer counter has overflowed. The enable signal selects between software polling (TOIE = 0) where no hardware interrupt is generated, or interrupt-driven operation (TOIE = 1) where a static hardware interrupt is automatically generated whenever the TOF flag is 1.

The conditions that cause TOF to become set depend on the counting mode (up or up/down). In up-counting mode, the main 16-bit counter counts from 0x0000 through 0xFFFF and overflows to 0x0000 on the next counting clock. TOF becomes set at the transition from 0xFFFF to 0x0000. When a modulus limit is set, TOF becomes set at the transition from the value set in the modulus register to 0x0000. When the main 16-bit counter is operating in up-/down-counting mode, the TOF flag gets set as the counter changes direction at the transition from the value set in the modulus register and the next lower count value. This corresponds to the end of a PWM period. (The 0x0000 count value corresponds to the center of a period.)

Because the HCS08 MCU is an 8-bit architecture, a coherency mechanism is built into the timer counter for read operations. Whenever either byte of the counter is read (TPMxCNTH or TPMxCNTL), both bytes are captured into a buffer so when the other byte is read, the value will represent the other byte of the count at the time the first byte was read. The counter continues to count normally, but no new value can be read from either byte until both bytes of the old count have been read.

The main timer counter can be reset manually at any time by writing any value to either byte of the timer count TPMxCNTH or TPMxCNTL. Resetting the counter in this manner also resets the coherency mechanism in case only one byte of the counter was read before resetting the count.

11.4.2 Channel Mode Selection

Provided CPWMS = 0 (center-aligned PWM operation is not specified), the MSnB and MSnA control bits in the channel n status and control registers determine the basic mode of operation for the corresponding channel. Choices include input capture, output compare, and buffered edge-aligned PWM.

11.4.2.1 Input Capture Mode

With the input capture function, the TPM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TPM latches the contents of the TPM counter into the channel value registers (TPMxCnVH:TPMxCnVL). Rising edges, falling edges, or any edge may be chosen as the active edge that triggers an input capture.

When either byte of the 16-bit capture register is read, both bytes are latched into a buffer to support coherent 16-bit accesses regardless of order. The coherency sequence can be manually reset by writing to the channel status/control register (TPMxCnSC).

An input capture event sets a flag bit (CHnF) that can optionally generate a CPU interrupt request.

A.8 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

A.8.1 Control Timing

Table A-8. Control Timing

Parameter	Symbol	Min	Typical ¹	Max	Unit
Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	1	—	8	MHz
Real-time interrupt internal oscillator period	t_{RTI}	700	—	1300	μ s
External reset pulse width ²	t_{extrst}	100	—	—	ns
IRQ pulse width Asynchronous path ² Synchronous path ³	t_{LILH}, t_{IHIL}	100 $1.5 t_{cyc}$	—	—	ns
KBIPx pulse width Asynchronous path ² Synchronous path ³	t_{LILH}, t_{IHIL}	100 $1.5 t_{cyc}$	—	—	ns
Port rise and fall time (load = 50 pF) ⁴ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	3 30	— —	ns
BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes ⁵	t_{MSH}	100	—	—	μ s

¹ Data in Typical column was characterized at 3.0 V, 25°C.

² This is the shortest pulse that is guaranteed to be recognized.

³ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

⁴ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40°C to 125°C.

⁵ To enter BDM mode following a POR, BKGD/MS must be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD} .

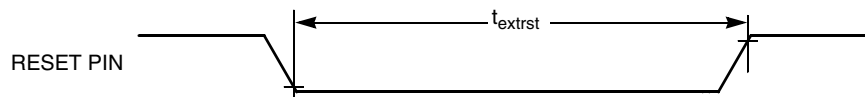


Figure A-12. Reset Timing



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
2. ALL DIMENSIONS ARE IN INCHES.
3. 626-03 TO 626-06 OBSOLETE. NEW STANDARD 626-07.
4. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.
5. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CONERS).

STYLE 1:

PIN	1.	AC IN	5.	GROUND
	2.	DC + IN	6.	OUTPUT
	3.	DC - IN	7.	AUXILIARY
	4.	AC IN	8.	VCC

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TITLE: 8 LD PDIP		DOCUMENT NO: 98ASB42420B		REV: N	
		CASE NUMBER: 626-06		19 MAY 2005	
		STANDARD: NON-JEDEC			