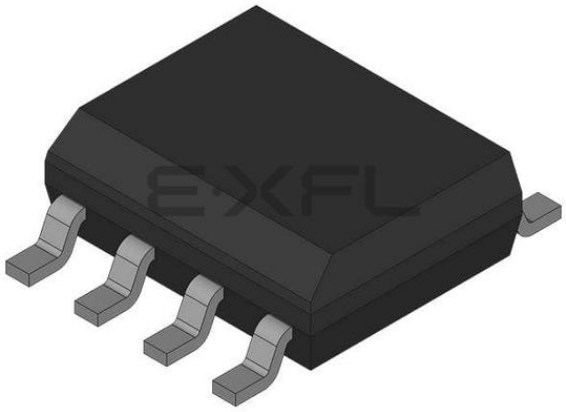


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	4
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s08qd2j1msc

Table 4-2. Direct-Page Register Summary (continued)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0x0017	**APCTL1**	—	—	—	—	ADPC3	ADPC2	ADPC1	ADPC0
0x0018	Reserved	—	—	—	—	—	—	—	—
0x0019	Reserved	—	—	—	—	—	—	—	—
0x001A– 0x001F	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
0x0020	**TPM2SC**	TOF	TOIE	CPWMS	CLKSB	CLKSA	PS2	PS1	PS0
0x0021	**TPM2CNTH**	Bit 15	14	13	12	11	10	9	Bit 8
0x0022	**TPM2CNTL**	Bit 7	6	5	4	3	2	1	Bit 0
0x0023	**TPM2MODH**	Bit 15	14	13	12	11	10	9	Bit 8
0x0024	**TPM2MODL**	Bit 7	6	5	4	3	2	1	Bit 0
0x0025	**TPM2C0SC**	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	0	0
0x0026	**TPM2C0VH**	Bit 15	14	13	12	11	10	9	Bit 8
0x0027	**TPM2C0VL**	Bit 7	6	5	4	3	2	1	Bit 0
0x0028– 0x0037	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
0x0038	**ICSC1**	0	CLKS	0	0	0	1	1	IREFSTEN
0x0039	**ICSC2**	BDIV		0	0	LP	0	0	0
0x003A	**ICSTRM**	TRIM							
0x003B	**ICSSC**	0	0	0	0	0	CLKST	0	FTRIM
0x003C	Reserved	—	—	—	—	—	—	—	—
0x0040	**TPMSC**	TOF	TOIE	CPWMS	CLKSB	CLKSA	PS2	PS1	PS0
0x0041	**TPMCNTH**	Bit 15	14	13	12	11	10	9	Bit 8
0x0042	**TPMCNTL**	Bit 7	6	5	4	3	2	1	Bit 0
0x0043	**TPMMODH**	Bit 15	14	13	12	11	10	9	Bit 8
0x0044	**TPMMODL**	Bit 7	6	5	4	3	2	1	Bit 0
0x0045	**TPMC0SC**	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	0	0
0x0046	**TPMC0VH**	Bit 15	14	13	12	11	10	9	Bit 8
0x0047	**TPMC0VL**	Bit 7	6	5	4	3	2	1	Bit 0
0x0048	**TPMC1SC**	CH1F	CH1IE	MS1B	MS1A	ELS1B	ELS1A	0	0
0x0049	**TPMC1VH**	Bit 15	14	13	12	11	10	9	Bit 8
0x004A	**TPMC1VL**	Bit 7	6	5	4	3	2	1	Bit 0
0x004B– 0x005F	Reserved	— —	— —	— —	— —	— —	— —	— —	— —

High-page registers, shown in Table 4-3, are accessed much less often than other I/O and control registers so they have been located outside the direct addressable memory space, starting at 0x1800.

Table 4-4. Nonvolatile Register Summary

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0xFFAA – 0xFFAC	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
0xFFAD	Reserved for ADCRL of AD26 value during ICS trim	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
0xFFAE	Reserved for ADCRH of AD26 value during ICS trim and ICS Trim value “FTRIM”	ADR9	ADR8	—	—	—	—	—	FTRIM
0xFFAF	Reserved for ICS Trim value “TRIM”	TRIM							
0xFFB0 – 0xFFB7	**NVBACKKEY**	8-Byte Comparison Key							
0xFFB8 – 0xFFBC	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
0xFFBD	**NVPROT**	FPS							FPDIS
0xFFBE	Unused	—	—	—	—	—	—	—	—
0xFFBF	**NVOPT**	KEYEN	FNORED	0	0	0	0	SEC01	SEC00

Provided the key enable (KEYEN) bit is 1, the 8-byte comparison key can be used to temporarily disengage memory security. This key mechanism can be accessed only through user code running in secure memory. (A security key cannot be entered directly through background debug commands.) This security key can be disabled completely by programming the KEYEN bit to 0. If the security key is disabled, the only way to disengage security is by mass erasing the flash if needed (normally through the background debug interface) and verifying that flash is blank. To avoid returning to secure mode after the next reset, program the security bits (SEC01:SEC00) to the unsecured state (1:0).

The ICS factory-trimmed value will be stored in 0xFFAE (bit-0) and 0xFFAF. Development tools, such as programmers can trim the ICS and the internal temperature sensor (via the ADC) and store the values in 0xFFAD–0xFFAF.

4.4 RAM

The MC9S08QD4 series includes static RAM. The locations in RAM below 0x0100 can be accessed using the more efficient direct addressing mode, and any single bit in this area can be accessed with the bit manipulation instructions (BCLR, BSET, BRCLR, and BRSET). Locating the most frequently accessed program variables in this area of RAM is preferred.

The RAM retains data when the MCU is in low-power wait, stop2, or stop3 mode. At power-on or after wakeup from stop1, the contents of RAM are uninitialized. RAM data is unaffected by any reset provided that the supply voltage does not drop below the minimum value for RAM retention (V_{RAM}).

One use for block protection is to block protect an area of flash memory for a bootloader program. This bootloader program then can be used to erase the rest of the flash memory and reprogram it. Because the bootloader is protected, it remains intact even if MCU power is lost in the middle of an erase and reprogram operation.

4.5.7 Vector Redirection

Whenever any block protection is enabled, the reset and interrupt vectors will be protected. Vector redirection allows users to modify interrupt vector information without unprotecting bootloader and reset vector space. Vector redirection is enabled by programming the FNORED bit in the NVOPT register located at address 0xFFBF to 0. For redirection to occur, at least some portion but not all of the flash memory must be block protected by programming the NVPROT register located at address 0xFFBD. All of the interrupt vectors (memory locations 0xFFC0–0xFFFD) are redirected, though the reset vector (0xFFFE:FFFF) is not.

For example, if 512 bytes of flash are protected, the protected address region is from 0xFE00 through 0xFFFF. The interrupt vectors (0xFFC0–0xFFFD) are redirected to the locations 0xFDC0–0xFDFD. For example, vector redirection is enabled and an interrupt occurs, the values in the locations 0xFDE0:FDE1 are used for the vector instead of the values in the locations 0xFFE0:FFE1. This allows the user to reprogram the unprotected portion of the flash with new program code including new interrupt vector values while leaving the protected area, which includes the default vector locations, unchanged.

4.6 Security

The MC9S08QD4 series includes circuitry to prevent unauthorized access to the contents of flash and RAM memory. When security is engaged, flash and RAM are considered secure resources. Direct-page registers, high-page registers, and the background debug controller are considered unsecured resources. Programs executing within secure memory have normal access to any MCU memory locations and resources. Attempts to access a secure memory location with a program executing from an unsecured memory space or through the background debug interface are blocked (writes are ignored and reads return all 0s).

Security is engaged or disengaged based on the state of two register bits (SEC01:SEC00) in the FOPT register. During reset, the contents of the nonvolatile location NVOPT are copied from flash into the working FOPT register in high-page register space. A user engages security by programming the NVOPT location, which can be performed at the same time the flash memory is programmed. The 1:0 state disengages security and the other three combinations engage security. Notice the erased state (1:1) makes the MCU secure. During development, whenever the flash is erased, it is good practice to immediately program the SEC00 bit to 0 in NVOPT so SEC01:SEC00 = 1:0. This would allow the MCU to remain unsecured after a subsequent reset.

The on-chip debug module cannot be enabled while the MCU is secure. The separate background debug controller can be used for background memory access commands, but the MCU cannot enter active background mode except by holding BKGD/MS low at the rising edge of reset.

A user can choose to allow or disallow a security unlocking mechanism through an 8-byte backdoor security key. If the nonvolatile KEYEN bit in NVOPT/FOPT is 0, the backdoor key is disabled and there

Table 5-2. Vector Summary

Vector Priority	Vector Number	Address (High:Low)	Vector Name	Module	Source	Enable	Description
Lower	31 through 24	0xFFC0:FFC1 through 0xFFCE:FFCF	Unused Vector Space (available for user program)				
	23	0xFFD0:FFD1	Vrti	System control	RTIF	RTIE	Real-time interrupt
	22	0xFFD2:FFD3	—	—	—	—	—
	21	0xFFD4:FFD5	—	—	—	—	—
	20	0xFFD6:FFD7	—	—	—	—	—
	19	0xFFD8:FFD9	Vadc1	ADC1	COCO	AIEN	ADC1
	18	0xFFDA:FFDB	Vkeyboard1	KBI1	KBF	KBIE	Keyboard pins
	17	0xFFDC:FFDD	—	—	—	—	—
	16	0xFFDE:FFDF	—	—	—	—	—
	15	0xFFE0:FFE1	—	—	—	—	—
	14	0xFFE2:FFE3	—	—	—	—	—
	13	0xFFE4:FFE5	—	—	—	—	—
	12	0xFFE6:FFE7	—	—	—	—	—
	11	0xFFE8:FFE9	—	—	—	—	—
	10	0xFFEA:FFEB	Vtpm2ovf	TPM2	TOF	TOIE	TPM2 overflow
	9	0xFFEC:FFED	—	—	—	—	—
	8	0xFFEE:FFEF	Vtpm2ch0	TPM2	CH0F	CH0IE	TPM2 channel 0
	7	0xFFF0:FFF1	Vtpm1ovf	TPM1	TOF	TOIE	TPM1 overflow
	6	0xFFF2:FFF3	Vtpm1ch1	TPM1	CH1F	CH1IE	TPM1 channel 1
	5	0xFFF4:FFF5	Vtpm1ch0	TPM1	CH0F	CH0IE	TPM1 channel 0
	4	0xFFF6:FFF7	—	—	—	—	—
	3	0xFFF8:FFF9	Virq	IRQ	IRRQF	IRQIE	IRQ pin
	2	0xFFFA:FFFB	Vlvd	System control	LVDF	LVDIE	Low voltage detect
	1	0xFFFC:FFFD	Vswi	CPU	SWI Instruction	—	Software interrupt
Higher	0	0xFFFE:FFFF	Vreset	System control	COP LVD $\overline{\text{RESET}}$ pin Illegal opcode Illegal address POR	COPE LVDRE RSTPE — — —	Watchdog timer Low-voltage detect External pin Illegal opcode Illegal address power-on-reset

5.6 Low-Voltage Detect (LVD) System

The MC9S08QD4 series includes a system to protect against low voltage conditions in order to protect memory contents and control MCU system states during supply voltage variations. The system is comprised of a power-on reset (POR) circuit and an LVD circuit with a user selectable trip voltage, either high (V_{LVDH}) or low (V_{LVDL}). The LVD circuit is enabled when LVDE in SPMSC1 is high and the trip voltage is selected by LVDV in SPMSC2. The LVD is disabled upon entering any of the stop modes unless LVDSE is set in SPMSC1. If LVDSE and LVDE are both set, then the MCU cannot enter stop1 or stop2, and the current consumption in stop3 with the LVD enabled will be greater.

Table 5-11. Real-Time Interrupt Period

RTIS2:RTIS1:RTIS0	Using Internal 1 kHz Clock Source[1] [2]	Using 32 kHz ICS Clock Source Period = t_{ext}[3]
0:0:0	Disable RTI	Disable RTI
0:0:1	8 ms	$t_{ext} \times 256$
0:1:0	32 ms	$t_{ext} \times 1024$
0:1:1	64 ms	$t_{ext} \times 2048$
1:0:0	128 ms	$t_{ext} \times 4096$
1:0:1	256 ms	$t_{ext} \times 8192$
1:1:0	512 ms	$t_{ext} \times 16384$
1:1:1	1.024 s	$t_{ext} \times 32768$

1 Values are shown in this column based on t_{RTI} = 1 ms. See t_{RTI} in the Section A.8.1, "Control Timing," for the tolerance of this value.

2 The initial RTI timeout period will be up to one 1 kHz clock period less than the time specified.

3 t_{ext} is the period of the 32 kHz ICS frequency.

5.8.8 System Power Management Status and Control 1 Register (SPMSC1)

This high-page register contains status and control bits to support the low voltage detect function, and to enable the bandgap voltage reference for use by the ADC module. To configure the low voltage detect trip voltage, see Table 5-13 for the LVDV bit description in SPMSC2.

	7	6	5	4	3	2	1[1]	0
R	LVDF	0	LVDIE	LVDRE[2]	LVDSE	LVDE[2]	0	BGBE
W		LVDACK						
Reset:	0	0	0	1	1	1	0	0

= Unimplemented or Reserved

1 Bit 1 is a reserved bit that must always be written to 0.

2 This bit can be written only one time after reset. Additional writes are ignored.

Figure 5-10. System Power Management Status and Control 1 Register (SPMSC1)

Table 5-12. SPMSC1 Register Field Descriptions

Field	Description
7 LVDF	**Low-Voltage Detect Flag** — Provided LVDE = 1, this read-only status bit indicates a low-voltage detect event.
6 LVDACK	**Low-Voltage Detect Acknowledge** — This write-only bit is used to acknowledge low voltage detection errors (write 1 to clear LVDF). Reads always return 0.

Table 5-13. SPMSC2 Register Field Descriptions

Field	Description
7 LVWF	**Low-Voltage Warning Flag** — The LVWF bit indicates the low voltage warning status. 0 Low voltage warning **not** preset. 1 Low voltage warning is present or was present.
6 LVWACK	**Low-Voltage Warning Acknowledge** — The LVWACK bit is the low-voltage warning acknowledge. Writing a 1 to LVWACK clears LVWF to a 0 if a low voltage warning is not present.
5 LVDV	**Low-Voltage Detect Voltage Select** — The LVDV bit selects the LVD trip point voltage (V_{LVD}). 0 Low trip point selected ($V_{LVD} = V_{LVDL}$). 1 High trip point selected ($V_{LVD} = V_{LVDH}$).
4 LVWV	**Low-Voltage Warning Voltage Select** — The LVWV bit selects the LVW trip point voltage (V_{LVW}). 0 Low trip point selected ($V_{LVW} = V_{LVWL}$). 1 High trip point selected ($V_{LVW} = V_{LVWH}$).
3 PPDF	**Partial Power Down Flag** — The PPDF bit indicates that the MCU has exited the stop2 mode. 0 Not stop2 mode recovery. 1 Stop2 mode recovery.
2 PPDACK	**Partial Power Down Acknowledge** — Writing a 1 to PPDACK clears the PPDF bit.
0 PPDC	**Partial Power Down Control** — The write-once PPDC bit controls whether stop2 or stop3 mode is selected. 0 Stop3 mode enabled. 1 Stop2, partial power down, mode enabled.

7.2.3 Stack Pointer (SP)

This 16-bit address pointer register points at the next available location on the automatic last-in-first-out (LIFO) stack. The stack may be located anywhere in the 64-Kbyte address space that has RAM and can be any size up to the amount of available RAM. The stack is used to automatically save the return address for subroutine calls, the return address and CPU registers during interrupts, and for local variables. The AIS (add immediate to stack pointer) instruction adds an 8-bit signed immediate value to SP. This is most often used to allocate or deallocate space for local variables on the stack.

SP is forced to 0x00FF at reset for compatibility with the earlier M68HC05 Family. HCS08 programs normally change the value in SP to the address of the last location (highest address) in on-chip RAM during reset initialization to free up direct page RAM (from the end of the on-chip registers to 0x00FF).

The RSP (reset stack pointer) instruction was included for compatibility with the M68HC05 Family and is seldom used in new HCS08 programs because it only affects the low-order half of the stack pointer.

7.2.4 Program Counter (PC)

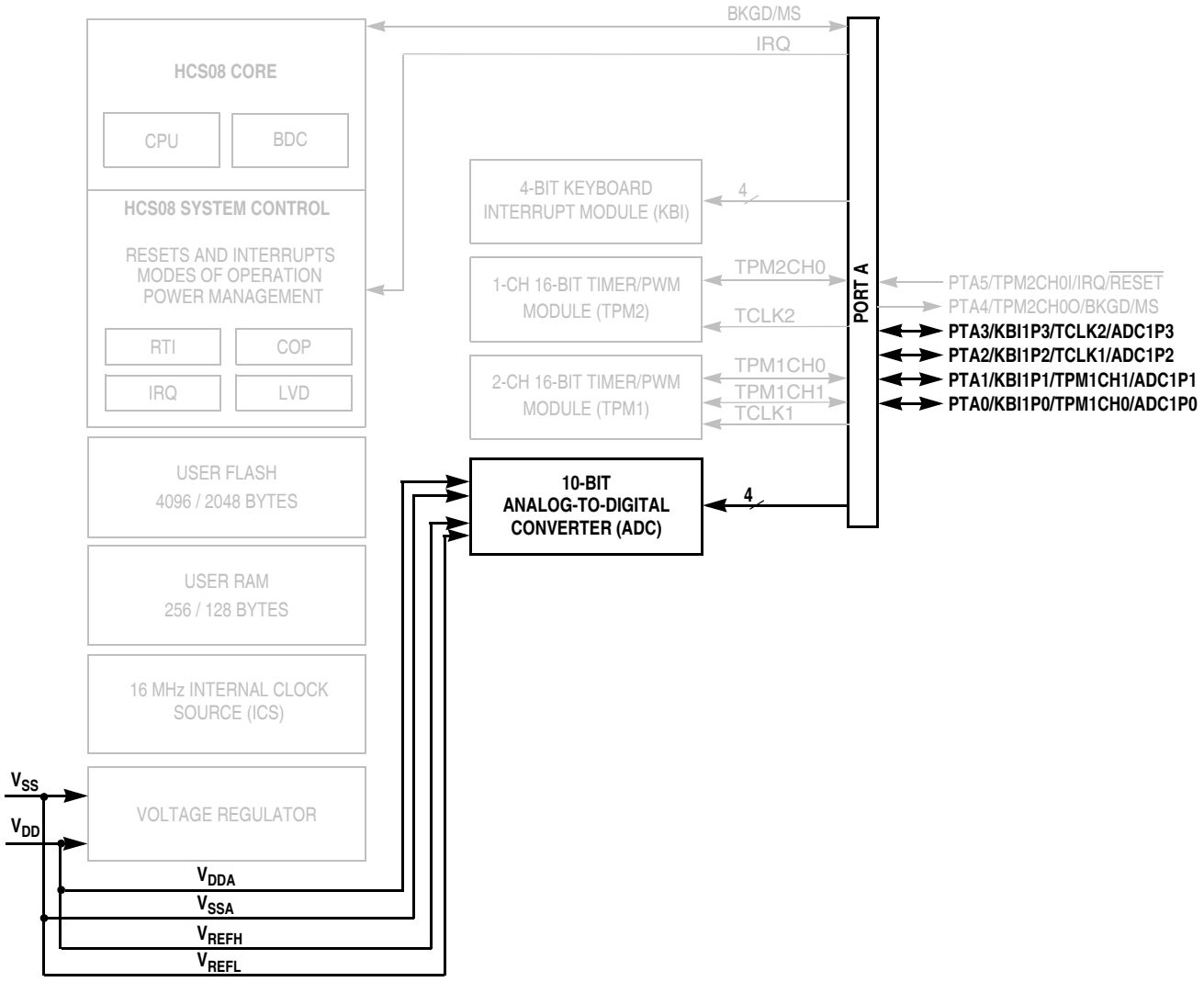
The program counter is a 16-bit register that contains the address of the next instruction or operand to be fetched.

During normal program execution, the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, interrupt, and return operations load the program counter with an address other than that of the next sequential location. This is called a change-of-flow.

During reset, the program counter is loaded with the reset vector that is located at 0xFFFE and 0xFFFF. The vector stored there is the address of the first instruction that will be executed after exiting the reset state.

7.2.5 Condition Code Register (CCR)

The 8-bit condition code register contains the interrupt mask (I) and five flags that indicate the results of the instruction just executed. Bits 6 and 5 are set permanently to 1. The following paragraphs describe the functions of the condition code bits in general terms. For a more detailed explanation of how each instruction sets the CCR bits, refer to the *HCS08 Family Reference Manual, volume 1,* Freescale Semiconductor document order number HCS08RMv1.



NOTES:
1. Port pins are software configurable with pullup device if input port.
2. Port pins are software configurable for output drive strength.
3. Port pins are software configurable for output slew rate control.
4. IRQ contains a software configurable (IRQPDD) pullup/pulldown device if PTA5 enabled as IRQ pin function (IRQPE = 1).
5. $\overline{\text{RESET}}$ contains integrated pullup device if PTA5 enabled as reset pin function (RSTPE = 1).
6. PTA5 does not contain a clamp diode to V_{DD} and must not be driven above V_{DD}. The voltage measured on this pin when internal pullup is enabled may be as low as $V_{DD} - 0.7$ V. The internal gates connected to this pin are pulled to V_{DD}.
7. PTA4 contains integrated pullup device if BKGD enabled (BKGDPE = 1).
8. When pin functions as KBI (KBIPEn = 1) and associated pin is configured to enable the pullup device, KBEDGn can be used to reconfigure the pullup as a pulldown device.

Figure 8-1. MC9S08QD4 Series Block Diagram Highlighting ADC Block and Pins

8.1.1 Module Configurations

This section provides device-specific information for configuring the ADC on MC9S08QD4 series.

8.1.1.1 Channel Assignments

The ADC channel assignments for the MC9S08QD4 series devices are shown in Table 8-1. Reserved channels convert to an unknown value.

Table 8-1. ADC Channel Assignment

ADCH	Channel	Input	Pin Control
00000	AD0	PTA0/ADC1P0	ADPC0
00001	AD1	PTA1/ADC1P1	ADPC1
00010	AD2	PTA2/ADC1P2	ADPC2
00011	AD3	PTA3/ADC1P3	ADPC3
00100	AD4	Vss	N/A
00101	AD5	Vss	N/A
00110	AD6	Vss	N/A
00111	AD7	Vss	N/A
01000	AD8	V_{SS}	N/A
01001	AD9	V_{SS}	N/A
01010	AD10	V_{SS}	N/A
01011	AD11	V_{SS}	N/A
01100	AD12	V_{SS}	N/A
01101	AD13	V_{SS}	N/A
01110	AD14	V_{SS}	N/A
01111	AD15	V_{SS}	N/A
10000	AD16	V_{SS}	N/A
10001	AD17	V_{SS}	N/A
10010	AD18	V_{SS}	N/A
10011	AD19	V_{SS}	N/A
10100	AD20	V_{SS}	N/A
10101	AD21	V_{SS}	N/A
10110	AD22	Reserved	N/A
10111	AD23	Reserved	N/A
11000	AD24	Reserved	N/A
11001	AD25	Reserved	N/A
11010	AD26	Temperature Sensor[1]	N/A
11011	AD27	Internal Bandgap[2]	N/A
11100	V_{REFH}	V_{DD}	N/A
11101	V_{REFH}	V_{DD}	N/A
11110	V_{REFL}	V_{SS}	N/A
11111	Module Disabled	None	N/A

1 For information, see Section 8.1.1.5, “Temperature Sensor.”

2 Requires BGBE =1 in SPMSC1 see Section 5.8.8, “System Power Management Status and Control 1 Register (SPMSC1).” For value of bandgap voltage reference see Appendix A.5, “DC Characteristics.”

8.1.1.2 Alternate Clock

The ADC is capable of performing conversions using the MCU bus clock, the bus clock divided by two, or the local asynchronous clock (ADACK) within the module. The alternate clock, ALTCLK, input for the MC9S08QD4 series MCU devices is not implemented.

8.1.1.3 Hardware Trigger

The ADC hardware trigger, ADHWT, is output from the real-time interrupt (RTI) counter. The RTI counter can be clocked by either ICSERCLK or a nominal 32 kHz clock source within the RTI block.

The period of the RTI is determined by the input clock frequency and the RTIS bits. The RTI counter is a free running counter that generates an overflow at the RTI rate determined by the RTIS bits. When the ADC hardware trigger is enabled, a conversion is initiated upon a RTI counter overflow.

converter yields the lower code (and vice-versa). However, even very small amounts of system noise can cause the converter to be indeterminate (between two codes) for a range of input voltages around the transition voltage. This range is normally around ±1/2 LSB and will increase with noise. This error may be reduced by repeatedly sampling the input and averaging the result. Additionally the techniques discussed in Section 8.6.2.3, "Noise-Induced Errors," will reduce this error.

Non-monotonicity is defined as when, except for code jitter, the converter converts to a lower code for a higher input voltage. Missing codes are those values which are never converted for any input value.

In 8-bit or 10-bit mode, the ADC is guaranteed to be monotonic and to have no missing codes.

9.4 Functional Description

9.4.1 Operational Modes

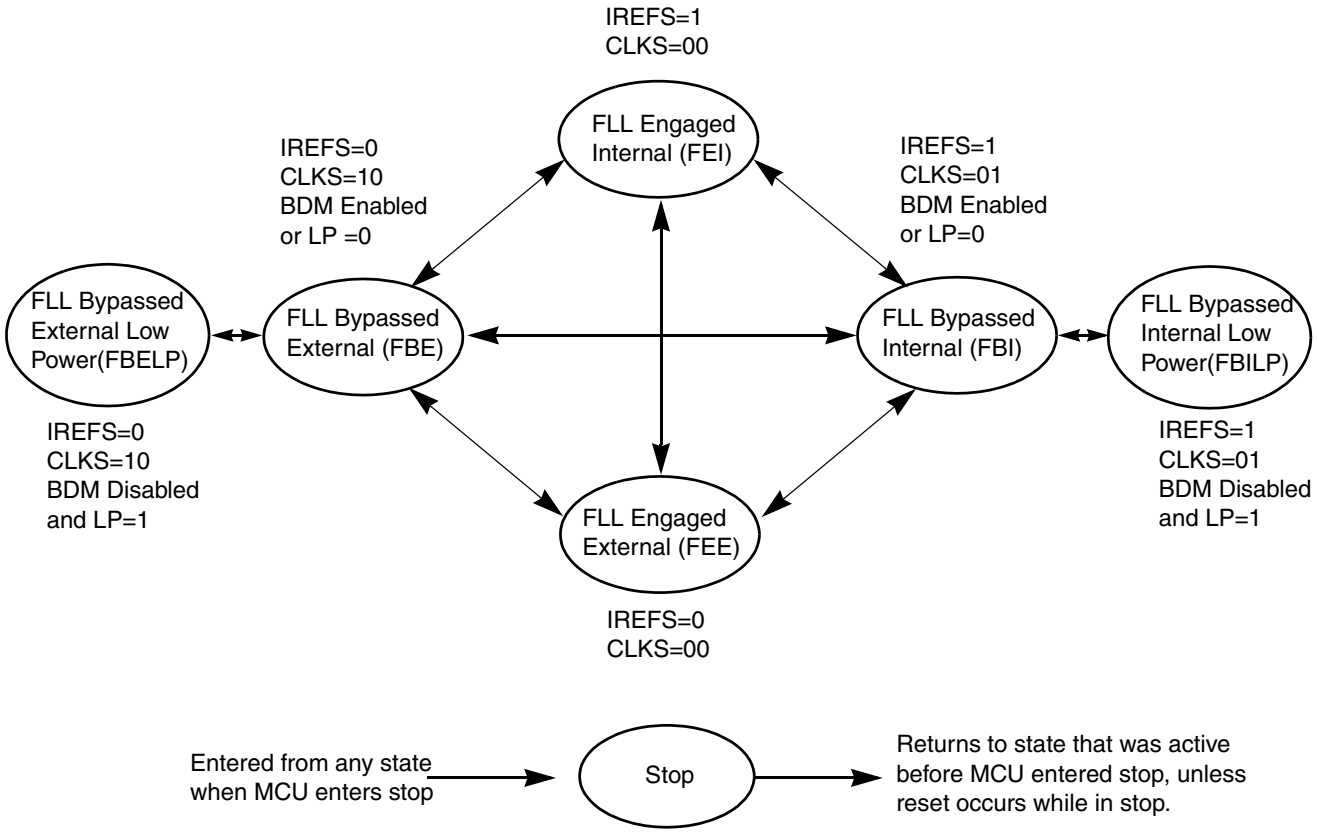


Figure 9-7. Clock Switching Modes

The seven states of the ICS are shown as a state diagram and are described below. The arrows indicate the allowed movements between the states.

9.4.1.1 FLL Engaged Internal (FEI)

FLL engaged internal (FEI) is the default mode of operation and is entered when all the following conditions occur:

- CLKS bits are written to 00
- IREFS bit is written to 1
- RDIV bits are written to divide trimmed reference clock to be within the range of 31.25 kHz to 39.0625 kHz.

In FLL engaged internal mode, the ICSOUT clock is derived from the FLL clock, which is controlled by the internal reference clock. The FLL loop will lock the frequency to 512 times the filter frequency, as selected by the RDIV bits. The ICSLCLK is available for BDC communications, and the internal reference clock is enabled.

times the filter frequency, as selected by the RDIV bits, so that the ICSLCLK will be available for BDC communications, and the external reference clock is enabled.

9.4.1.6 FLL Bypassed External Low Power (FBELP)

The FLL bypassed external low power (FBELP) mode is entered when all the following conditions occur:

- CLKS bits are written to 10.
- IREFS bit is written to 0.
- BDM mode is not active and LP bit is written to 1.

In FLL bypassed external low power mode, the ICSOUT clock is derived from the external reference clock and the FLL is disabled. The ICSLCLK will be not be available for BDC communications. The external reference clock is enabled.

9.4.1.7 Stop

Stop mode is entered whenever the MCU enters a STOP state. In this mode, all ICS clock signals are static except in the following cases:

ICSIRCLK will be active in stop mode when all the following conditions occur:

- IRCLKEN bit is written to 1
- IREFSTEN bit is written to 1

ICSERCLK will be active in stop mode when all the following conditions occur:

- ERCLKEN bit is written to 1
- EREFSTEN bit is written to 1

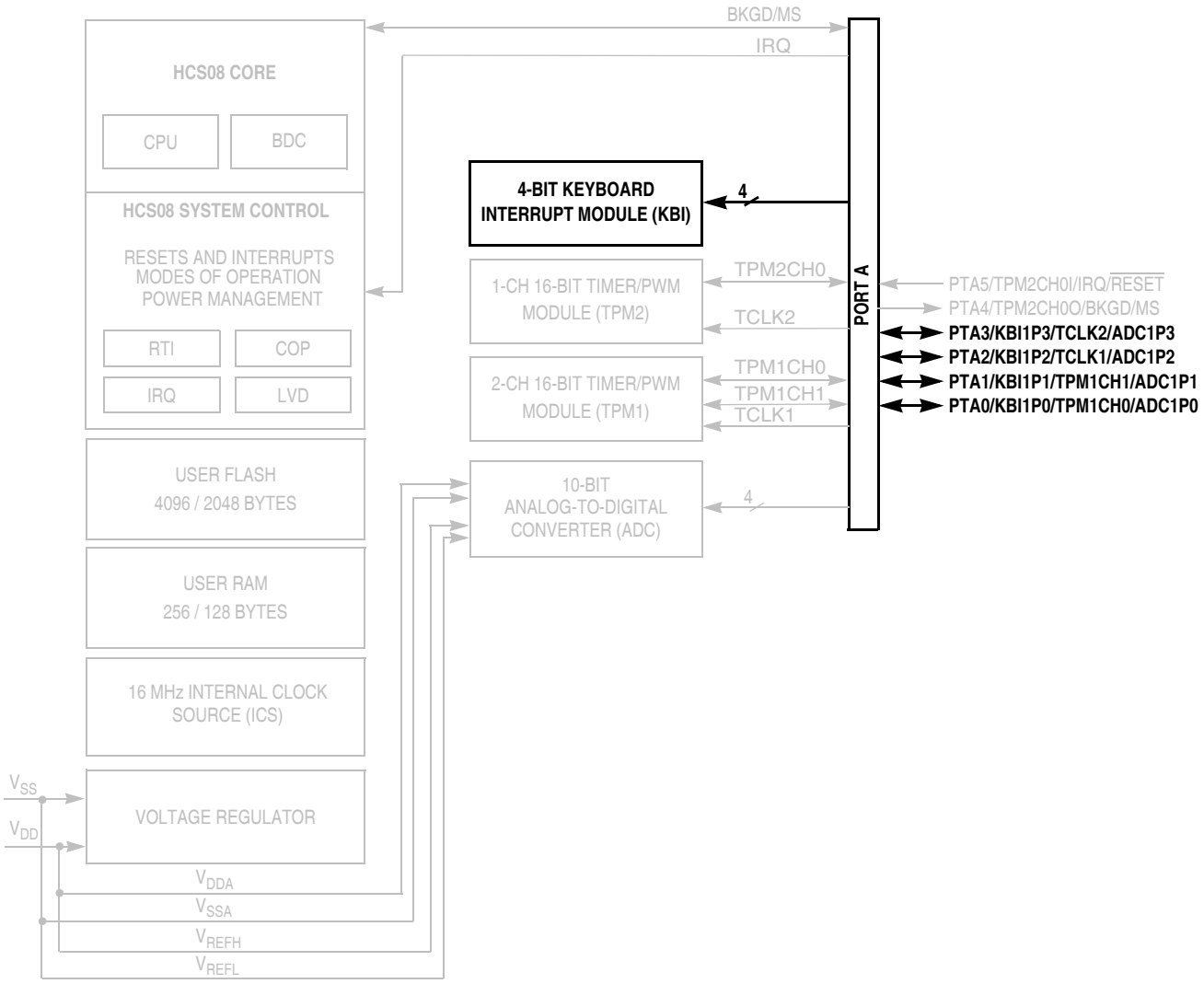
9.4.2 Mode Switching

When switching between FLL engaged internal (FEI) and FLL engaged external (FEE) modes the IREFS bit can be changed at anytime, but the RDIV bits must be changed simultaneously so that the resulting frequency stays in the range of 31.25 kHz to 39.0625 kHz. After a change in the IREFS value the FLL will begin locking again after a few full cycles of the resulting divided reference frequency.

The CLKS bits can also be changed at anytime, but the RDIV bits must be changed simultaneously so that the resulting frequency stays in the range of 31.25 kHz to 39.0625 kHz. The actual switch to the newly selected clock will not occur until after a few full cycles of the new clock. If the newly selected clock is not available, the previous clock will remain selected.

9.4.3 Bus Frequency Divider

The BDIV bits can be changed at anytime and the actual switch to the new frequency will occur immediately.



NOTES:
1. Port pins are software configurable with pullup device if input port.
2. Port pins are software configurable for output drive strength.
3. Port pins are software configurable for output slew rate control.
4. IRQ contains a software configurable (IRQPDD) pullup/pulldown device if PTA5 enabled as IRQ pin function (IRQPE = 1).
5. $\overline{\text{RESET}}$ contains integrated pullup device if PTA5 enabled as reset pin function (RSTPE = 1).
6. PTA5 does not contain a clamp diode to V_{DD} and must not be driven above V_{DD}. The voltage measured on this pin when internal pullup is enabled may be as low as $V_{DD} - 0.7$ V. The internal gates connected to this pin are pulled to V_{DD}.
7. PTA4 contains integrated pullup device if BKGD enabled (BKGDPE = 1).
8. When pin functions as KBI (KBIPEn = 1) and associated pin is configured to enable the pullup device, KBEDGn can be used to reconfigure the pullup as a pulldown device.

Figure 10-1. MC9S08QD4 Series Block Diagram Highlighting KBI Block and Pins

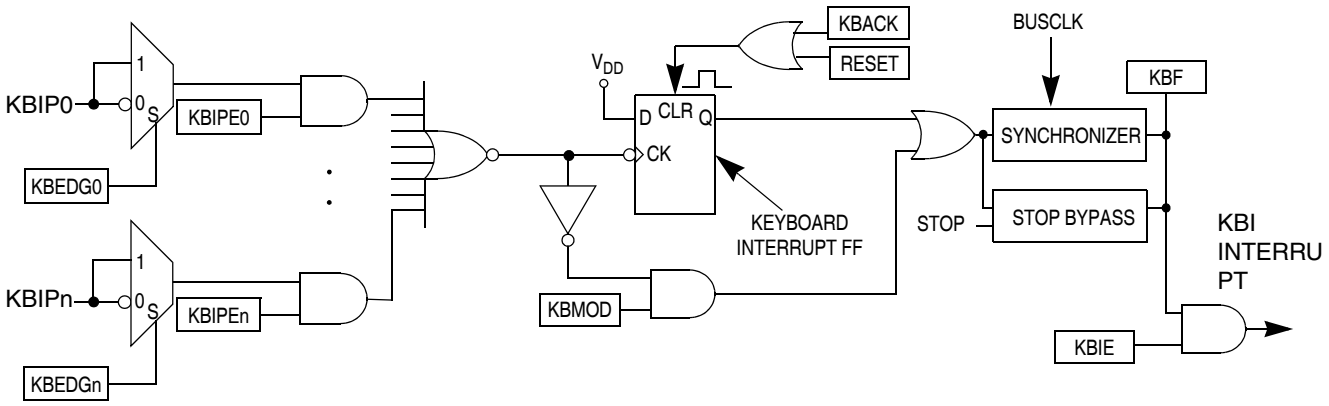


Figure 10-2. KBI Block Diagram

10.2 External Signal Description

The KBI input pins can be used to detect either falling edges, or both falling edge and low level interrupt requests. The KBI input pins can also be used to detect either rising edges, or both rising edge and high level interrupt requests.

The signal properties of KBI are shown in Table 10-1.

Table 10-1. Signal Properties

Signal	Function	I/O
KBIPn	Keyboard interrupt pins	I

10.3 Register Definition

The KBI includes three registers:

- An 8-bit pin status and control register.
- An 8-bit pin enable register.
- An 8-bit edge select register.

Refer to the direct-page register summary in the Memory chapter for the absolute address assignments for all KBI registers. This section refers to registers and control bits only by their names.

Some MCUs may have more than one KBI, so register names include placeholder characters to identify which KBI is being referenced.

10.3.1 KBI Status and Control Register (KBISC)

KBISC contains the status flag and control bits, which are used to configure the KBI.

Chapter 12
Development Support

12.1 Introduction

Development support systems in the HCS08 include the background debug controller (BDC). The BDC provides a single-wire debug interface to the target MCU that provides a convenient interface for programming the on-chip flash and other nonvolatile memories. The BDC is also the primary debug interface for development and allows non-intrusive access to memory data and traditional debug features such as CPU register modify, breakpoints, and single instruction trace commands.

In the HCS08 Family, address and data bus signals are not available on external pins (not even in test modes). Debug is done through commands fed into the target MCU via the single-wire background debug interface. The debug module provides a means to selectively trigger and capture bus information so an external development system can reconstruct what happened inside the MCU on a cycle-by-cycle basis without having external access to the address and data signals.

12.1.1 Forcing Active Background

The method for forcing active background mode depends on the specific HCS08 derivative. For the MC9S08QD4 series, you can force active background mode by holding the BKGD pin low as the MCU exits the reset condition independent of what caused the reset. If no debug pod is connected to the BKGD pin, the MCU will always reset into normal operating mode.

12.1.2 Module Configuration

The alternative BDC clock source for MC9S08QD4 series is the ICGCLK. See Chapter 9, “Internal Clock Source (S08ICSV1),” for more information about ICGCLK and how to select clock sources.

Appendix A
Electrical Characteristics

A.1 Introduction

This chapter contains electrical and timing specifications.

A.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table A-1 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table A-1. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

Table A-5. DC Characteristics (continued)(Temperature Range = –40 to 125°C Ambient)

Parameter	Symbol	Min	Typical	Max	Unit
High impedance (off-state) leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input/output	$\|I_{OZ}\|$	—	0.025	1.0	μA
Internal pullup resistors[4]	R_{PU}	17.5		52.5	kΩ
Internal pulldown resistor (IRQ)	R_{PD}	17.5		52.5	kΩ
Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.6 mA 5 V, I_{Load} = –0.4 mA 3 V, I_{Load} = –0.24 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = –10 mA 3 V, I_{Load} = –3 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	
Maximum total I_{OH} for all port pins 5V 3V	$\|I_{OHT}\|$	 — —	 — —	 100 60	mA
Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.6 mA 5 V, I_{Load} = 0.4 mA 3 V, I_{Load} = 0.24 mA	V_{OL}	 — — — —	 — — — —	 1.5 1.5 0.8 0.8	V
Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 3 V, I_{Load} = 3 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.4 mA		 — — — —	 — — — —	 1.5 1.5 0.8 0.8	
Maximum total I_{OL} for all port pins 5V 3V	I_{OLT}	 — —	 — —	 100 60	mA
DC injection current[2, 5, 6, 7] Single pin limit V_{IN} > V_{DD} V_{IN} < V_{SS} Total MCU limit, includes sum of all stressed pins V_{IN} > V_{DD} V_{IN} < V_{SS}	I_{IC}	 0 0 0 0	 — 	 2 –0.2 12 –1.2	mA
Input capacitance (all non-supply pins)	C_{In}	—		7	pF

1 Maximum is highest voltage that POR is guaranteed.

2 RAM will retain data down to POR voltage. RAM data not guaranteed to be valid following a POR.

3 This parameter is characterized and not tested on each device.

4 Measurement condition for pull resistors: V_{In} = V_{SS} for pullup and V_{In} = V_{DD} for pulldown.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

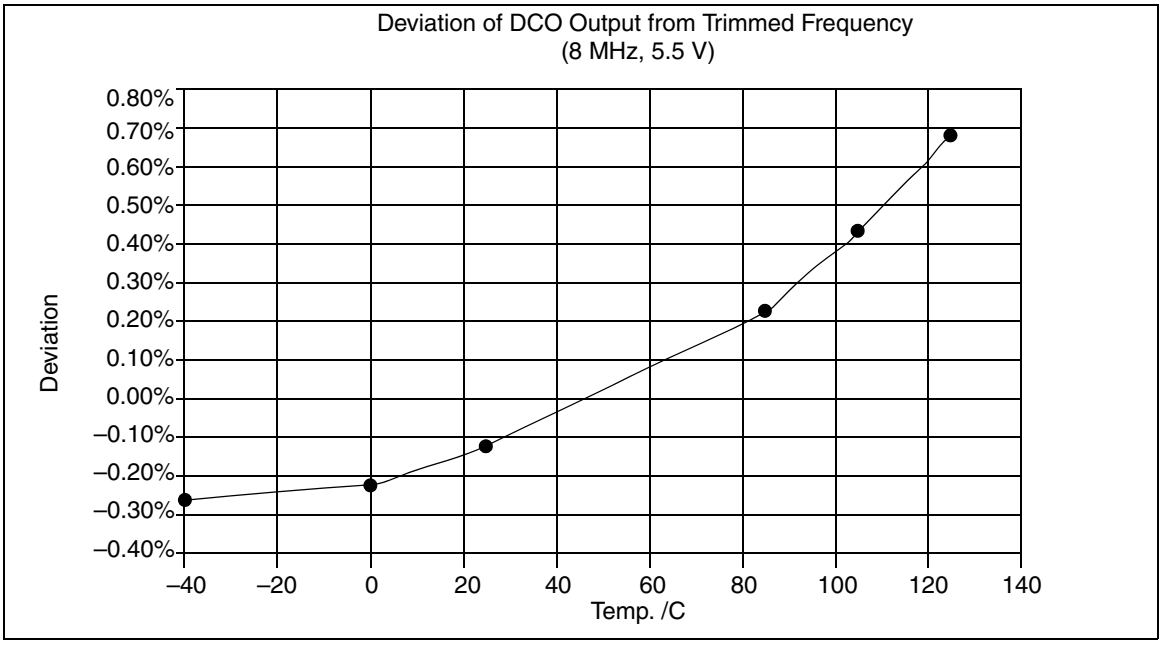


Figure A-10. Typical Deviation of DCO Output vs. Temperature

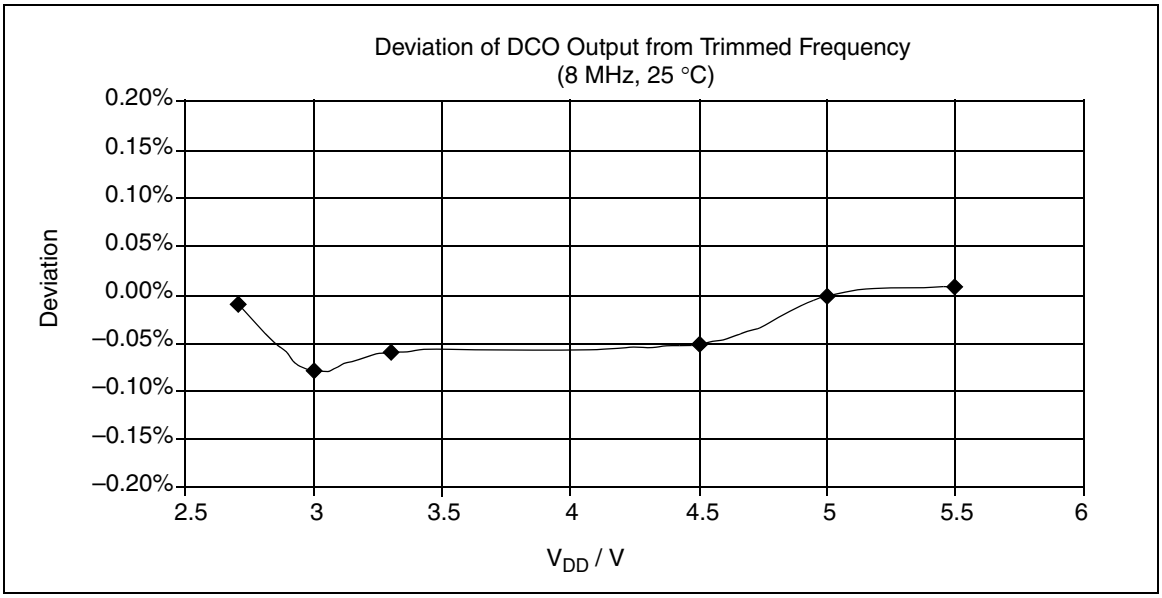


Figure A-11. Typical Deviation of DCO Output vs. Operating Voltage

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42564B	REV: U
8LD SOIC NARROW BODY	CASE NUMBER: 751–07	07 APR 2005
	STANDARD: JEDEC MS–012AA	