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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l041c6t6tr

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2 Description

The access line ultra-low-power STM32L041x4/6 family incorporates the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, high-speed embedded memories (up to 32 Kbytes of Flash program memory, 1 Kbytes of data EEPROM and 8 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L041x4/6 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L041x4/6 devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, AES, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L041x4/6 devices embed standard and advanced communication interfaces: one I2C, one SPI, one USART, and a low-power UART (LPUART).

The STM32L041x4/6 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L041x4/6 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.4.4 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA5, PA6, PA7), USART2 (PA2, PA3) or USART2 (PA9, PA10). See STM32™ microcontroller system memory boot mode AN2606 for details.

3.12 Ultra-low-power comparators and reference voltage

The STM32L041x4/6 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
  - External I/O pins
  - Internal reference voltage (V_{REFINT})
  - submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.13 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM21, TIM22 and LPTIM timer input captures. It also controls the routing of internal analog signals to the ADC, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

3.14 AES

The AES Hardware Accelerator can be used to encrypt and decrypt data using the AES algorithm (compatible with FIPS PUB 197, 2001 Nov 26):

- Key scheduler
- Key derivation for decryption
- 128-bit data block processed
- 128-bit key length
- 213 clock cycles to encrypt/decrypt one 128-bit block
- Electronic codebook (ECB), cypher block chaining (CBC), and counter mode (CTR) supported by hardware.

The AES can be served by the DMA controller.

3.15 Timers and watchdogs

The ultra-low-power STM32L041x4/6 devices include three general-purpose timers, one low- power timer (LPTM), two watchdog timers and the SysTick timer.

Table 9 compares the features of the general-purpose and basic timers.

Table 9. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No

3.15.1 General-purpose timers (TIM2, TIM21 and TIM22)

There are three synchronizable general-purpose timers embedded in the STM32L041x4/6 devices (see *Table 9* for differences).

TIM2

TIM2 is based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2 general-purpose timers can work together or with the TIM21 and TIM22 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2 has independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together and be synchronized with the TIM2, full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.15.2 Low-power Timer (LPTIM)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one shot mode
- Selectable software / hardware input trigger
- Selectable clock source
  - Internal clock source: LSE, LSI, HSI or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.15.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches ‘0’.

3.15.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.15.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

The USART interface (USART2) is able to communicate at speeds of up to 4 Mbit/s.

it provides hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART2 also supports Smartcard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock that allows to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

USART2 interface can be served by the DMA controller.

Table 12 for the supported modes and features of USART interface.

Table 12. USART implementation

USART modes/features(1)	USART2
Hardware flow control for modem	X
Continuous communication using DMA	X
Multiprocessor communication	X
Synchronous mode(2)	X
Smartcard mode	X
Single-wire half-duplex communication	X
IrDA SIR ENDEC block	X
LIN mode	X
Dual clock domain and wakeup from Stop mode	X
Receiver timeout interrupt	X
Modbus communication	X
Auto baud rate detection (4 modes)	X
Driver Enable	X

1. X = supported.
2. This mode allows using the USART as an SPI master.

3.16.3 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Or any received data frame
- Or a specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while

having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.16.4 Serial peripheral interface (SPI)

The SPI is able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The USARTs with synchronous capability can also be used as SPI master.

The SPI can be served by the DMA controller.

Refer to *Table 13* for the supported modes and features of SPI interface.

Table 13. SPI implementation

SPI features(1)	SPI1
Hardware CRC calculation	X
I2S mode	-
TI mode	X

1. X = supported.

3.17 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.18 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 15. Pin definitions (continued)

Pin number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25	UFQFPN28	UFQFPN28 (STM32L041GxUxS only)	LQFP32	UFQFPN32[1]	LQFP48						
7	B4	7	7	7	7	11	PA1	I/O	FT	-	EVENTOUT, LPTIM1_IN2, TIM2_CH2, I2C1_SMBA, USART2_RTS, TIM21_ETR	COMP1_INP, ADC_IN1
8	D4	8	8	8	8	12	PA2	I/O	TC	-	TIM21_CH1, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT	COMP2_INM6, ADC_IN2, RTC_TAMP3/RTC_TS/RTC_OUT/WKUP3
9	E4	9	9	9	9	13	PA3	I/O	FT	-	TIM21_CH2, TIM2_CH4, USART2_RX, LPUART1_RX	COMP2_INP, ADC_IN3
10	B3	10	10	10	10	14	PA4	I/O	TC	-	SPI1_NSS, LPTIM1_IN1, USART2_CK, TIM22_ETR	COMP1_INM4, COMP2_INM4, ADC_IN4
11	D3	11	11	11	11	15	PA5	I/O	TC	-	SPI1_SCK, LPTIM1_IN2, TIM2_ETR, TIM2_CH1	COMP1_INM5, COMP2_INM5, ADC_IN5
12	E3	12	12	12	12	16	PA6	I/O	FT	-	SPI1_MISO, LPTIM1_ETR, LPUART1_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6

Table 16. Alternate functions

Ports		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/USART2 /LPTIM/TIM21 /EVENTOUT/ SYS_AF	SPI1/I2C1/ LPTIM	LPTIM/TIM2/ EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART2/ LPUART1/ TIM22/ EVENTOUT	TIM2/21/22	LPUART1/ EVENTOUT	COMP1/2
Port A	PA0	-	LPTIM1_IN1	TIM2_CH1	-	USART2_CTS	TIM2_ETR	-	COMP1_OUT
	PA1	EVENTOUT	LPTIM1_IN2	TIM2_CH2	I2C1_SMBA	USART2_RTS	TIM21_ETR	-	-
	PA2	TIM21_CH1	-	TIM2_CH3	-	USART2_TX	-	LPUART1_TX	COMP2_OUT
	PA3	TIM21_CH2	-	TIM2_CH4	-	USART2_RX	-	LPUART1_RX	
	PA4	SPI1_NSS	LPTIM1_IN1	-	-	USART2_CK	TIM22_ETR	-	-
	PA5	SPI1_SCK	LPTIM1_IN2	TIM2_ETR	-	-	TIM2_CH1	-	-
	PA6	SPI1_MISO	LPTIM1_ETR	-	-	LPUART1_CTS	TIM22_CH1	EVENTOUT	COMP1_OUT
	PA7	SPI1_MOSI	LPTIM1_OUT	-	-	USART2_CTS	TIM22_CH2	EVENTOUT	COMP2_OUT
	PA8	MCO	-	LPTIM1_IN1	EVENTOUT	USART2_CK	TIM2_CH1	-	-
	PA9	MCO	I2C1_SCL	-	-	USART2_TX	TIM22_CH1	-	-
	PA10	-	I2C1_SDA	-	-	USART2_RX	TIM22_CH2	-	-
	PA11	SPI1_MISO	-	EVENTOUT	-	USART2_CTS	TIM21_CH2	-	COMP1_OUT
	PA12	SPI1_MOSI	-	EVENTOUT	-	USART2_RTS	-	-	COMP2_OUT
	PA13	SWDIO	LPTIM1_ETR	-	-	-	-	LPUART1_RX	-
	PA14	SWCLK	LPTIM1_OUT	-	I2C1_SMBA	USART2_TX	-	LPUART1_TX	-
	PA15	SPI1_NSS	-	TIM2_ETR	EVENTOUT	USART2_RX	TIM2_CH1	-	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 11. Pin loading conditions

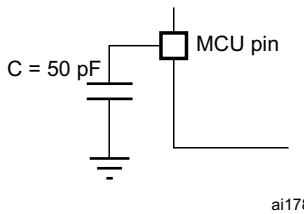


Figure 12. Pin input voltage

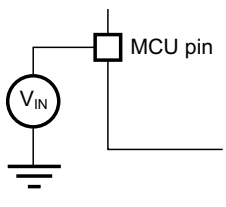


Table 32. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
I_{DD} (Standby)	Supply current in Standby mode	Independent watchdog and LSI enabled	T_A = -40 °C to 25 °C	0.8	1.6	µA
			T_A = 55 °C	0.9	1.8	
			T_A= 85 °C	1	2	
			T_A = 105 °C	1.3	3	
			T_A = 125 °C	2.15	7	
		Independent watchdog and LSI off	T_A = -40 °C to 25 °C	0.255	0.6	
			T_A = 55 °C	0.28	0.7	
			T_A = 85 °C	0.405	1	
			T_A = 105 °C	0.7	1.7	
			T_A = 125 °C	1.55	5	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified

Table 33. Average current consumption during wakeup

Symbol	parameter	System frequency	Current consumption during wakeup	Unit
I_{DD} (WU from Stop)	Supply current during wakeup from Stop mode	HSI	1	mA
		HSI/4	0.7	
		MSI 4,2 MHz	0.7	
		MSI 1,05 MHz	0.4	
		MSI 65 KHz	0.1	
I_{DD} (Reset)	Reset pin pulled down	-	0.21	
I_{DD} (Power Up)	BOR on	-	0.23	
I_{DD} (WU from StandBy)	With Fast wakeup set	MSI 2,1 MHz	0.5	
	With Fast wakeup disabled	MSI 2,1 MHz	0.12	

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

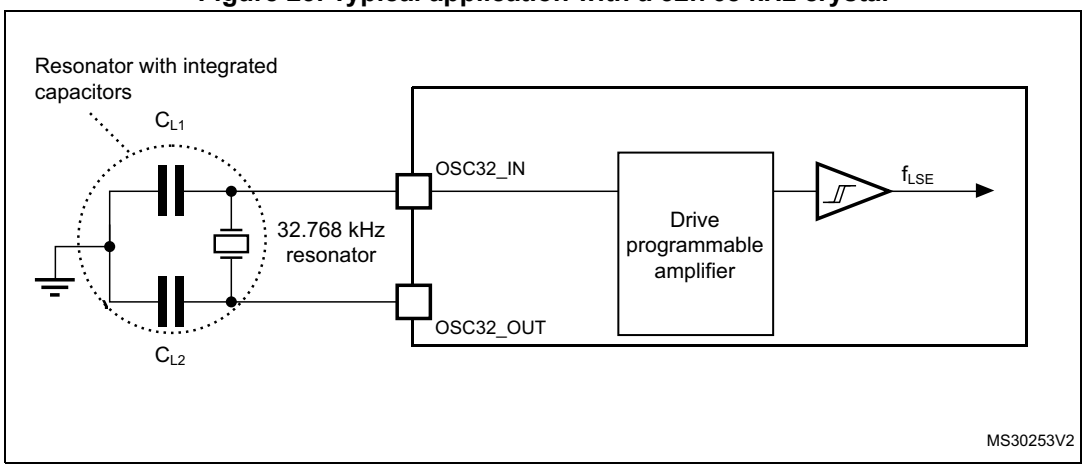
Table 40. LSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min(2)	Typ	Max	Unit
f_{LSE}	LSE oscillator frequency		-	32.768	-	kHz
G_m	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. Guaranteed by characterization results. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 23. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.7 Internal clock source characteristics

The parameters given in *Table 41* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

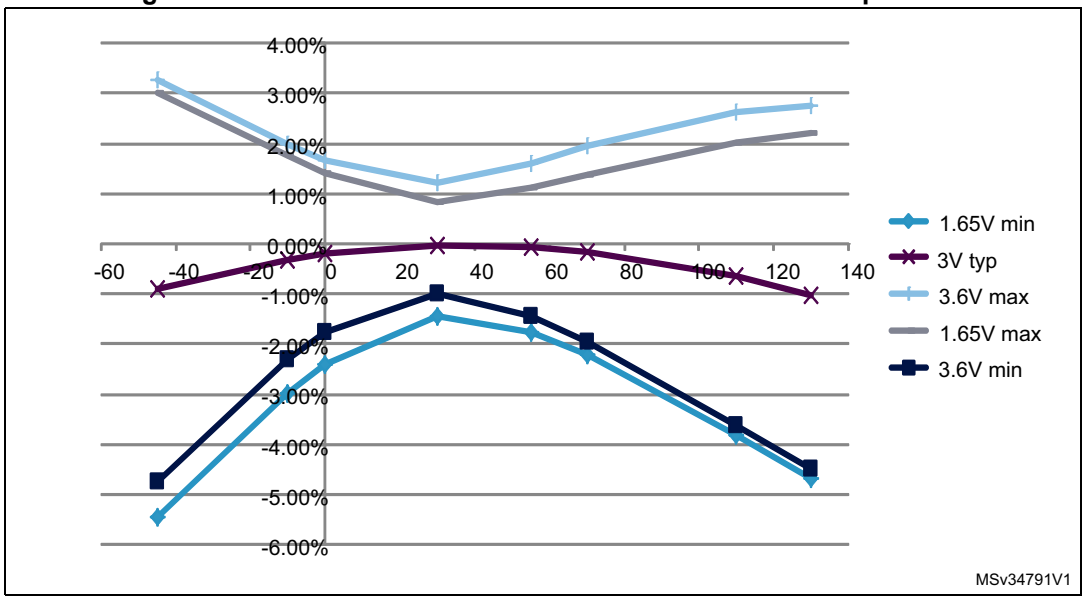
High-speed internal 16 MHz (HSI16) RC oscillator

Table 41. 16 MHz HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI16 user-trimmed resolution	Trimming code is not a multiple of 16	-	±0.4	0.7	%
		Trimming code is a multiple of 16	-	-	±1.5	%
ACC_{HSI16} (2)	Accuracy of the factory-calibrated HSI16 oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1(3)	-	1(3)	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = -40 to 125 °C	-5.45	-	3.25	%
$t_{SU(HSI16)}^{(2)}$	HSI16 oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI16)}^{(2)}$	HSI16 oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Figure 24. HSI16 minimum and maximum value versus temperature



These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 51. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the *Table 52*.

Table 52. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PA0, PA2, PA4, PA5, PC15, PH0 and PH1	-5	0	
	Injected current on any other FT and FTf pin	-5 (1)	NA	
	Injected current on any other pin	-5 (1)	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Table 57. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CAL}(3)	Calibration time	f_{ADC} = 16 MHz	5.2			µs
			83			$1/f_{ADC}$
$W_{LATENCY}$	ADC_DR register write latency	ADC clock = HSI16	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr}(3)	Trigger conversion latency	f_{ADC} = f_{PCLK}/2 = 16 MHz	0.266			µs
		f_{ADC} = f_{PCLK}/2	8.5			$1/f_{PCLK}$
		f_{ADC} = f_{PCLK}/4 = 8 MHz	0.516			µs
		f_{ADC} = f_{PCLK}/4	16.5			$1/f_{PCLK}$
		f_{ADC} = f_{HSI16} = 16 MHz	0.252	-	0.260	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	f_{ADC} = f_{HSI16}	-	1	-	$1/f_{HSI16}$
t_S(3)	Sampling time	f_{ADC} = 16 MHz	0.093	-	10.03	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(3)	Power-up time		0	0	1	µs
t_{ConV}(3)	Total conversion time (including sampling time)	f_{ADC} = 16 MHz	0.875		10.81	µs
			14 to 173 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. V_{DDA} minimum value can be decreased in specific temperature conditions. Refer to *Table 58: RAIN max for fADC = 16 MHz*.
2. A current consumption proportional to the APB clock frequency has to be added (see *Table 34: Peripheral current consumption in Run or Sleep mode*).
3. Guaranteed by design.
4. Standard channels have an extra protection resistance which depends on supply voltage. Refer to *Table 58: RAIN max for fADC = 16 MHz*.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

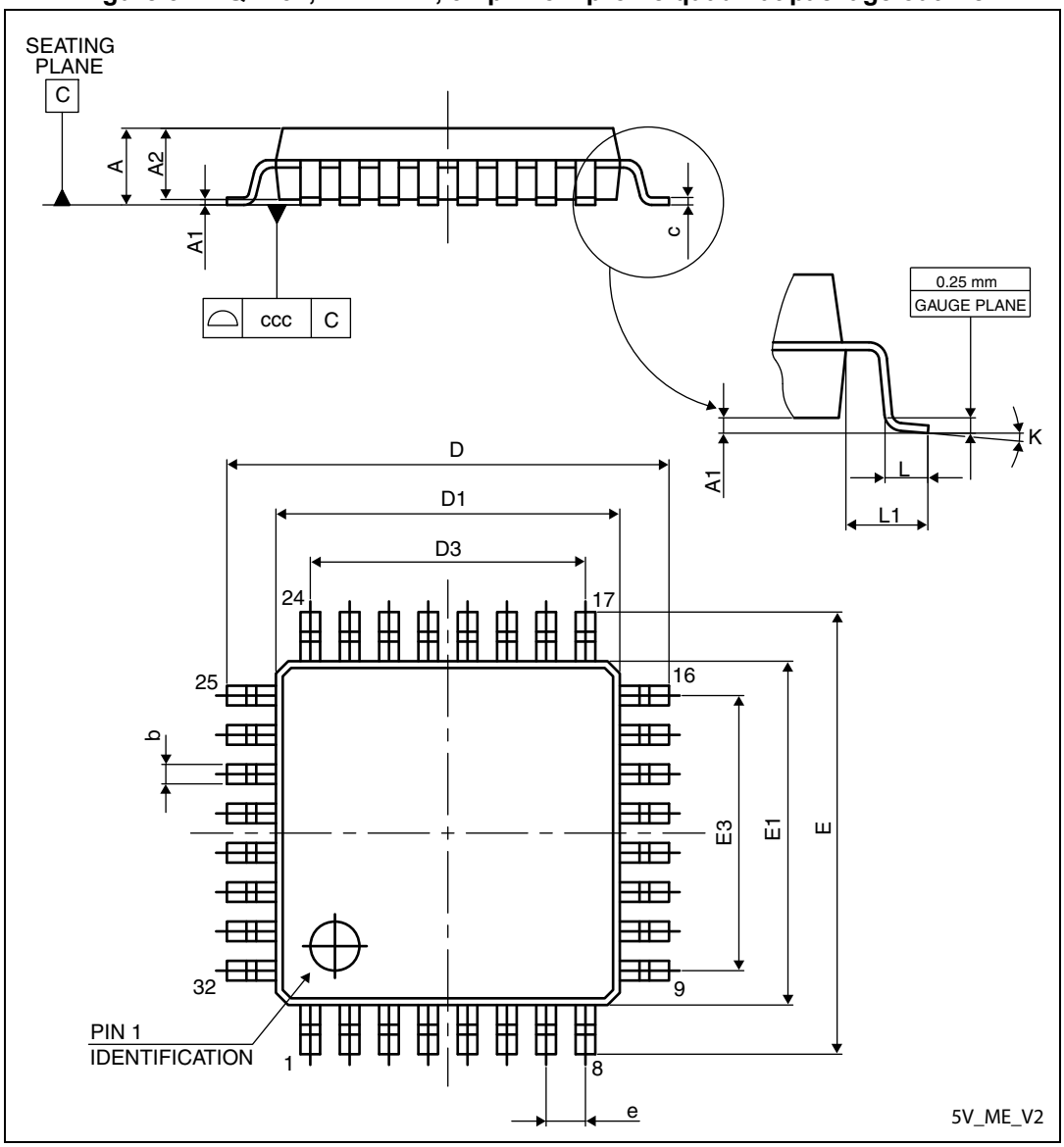
Table 70. LQFP48 - 48-pin low-profile quad flat package, 7 x 7 mm, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 LQFP32 package information

Figure 37. LQFP32, 7 x 7 mm, 32-pin low-profile quad flat package outline



1. Drawing is not to scale.

7.5 WLCSP25 package information

Figure 46. WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale package outline

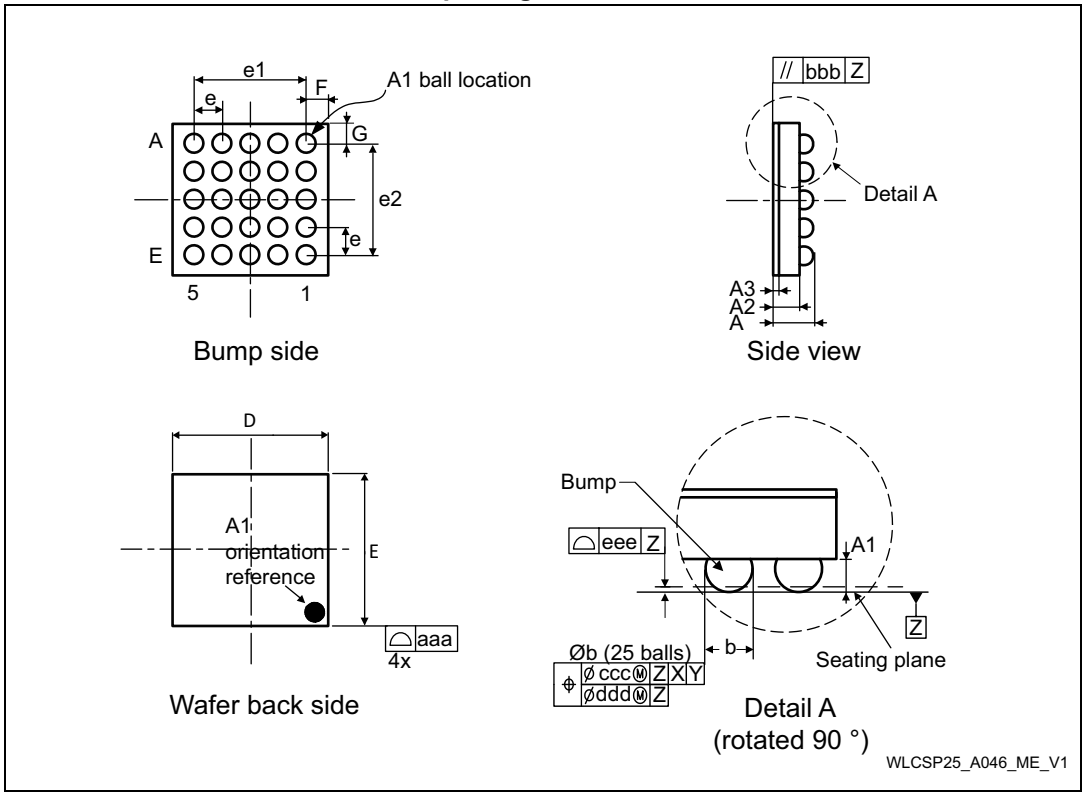


Table 74. WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale mechanical data

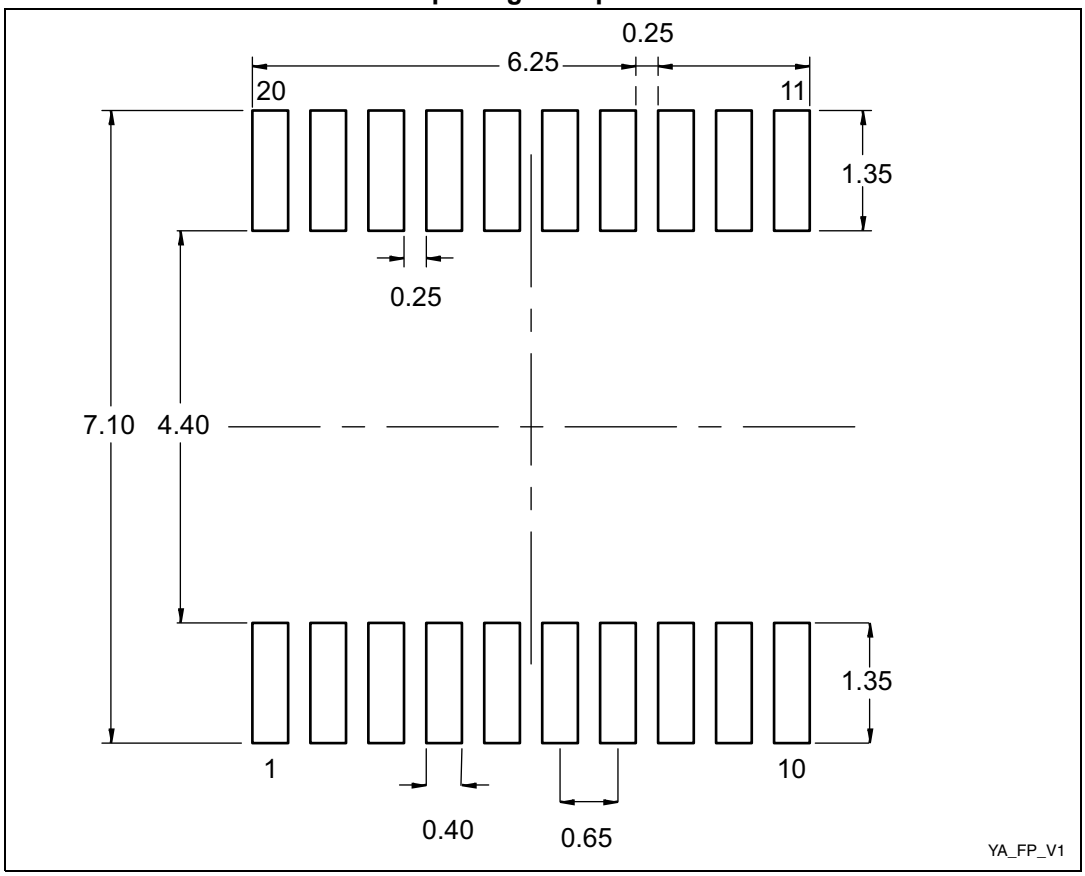
Symbol	Milimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.5250	0.5550	0.5850	0.0207	0.0219	0.0230
A1	-	0.1750	-	-	0.0069	-
A2	-	0.3800	-	-	0.0150	-
A3[2]	-	0.0250	-	-	0.0010	-
b[3]	0.2200	0.2500	0.2800	0.0087	0.0098	0.0110
D	2.0620	2.0970	2.1320	0.0812	0.0826	0.0839
E	2.4580	2.4930	2.5280	0.0968	0.0981	0.0995
e	-	0.4000	-	-	0.0157	-
e1	-	1.6000	-	-	0.0630	-
e2	-	1.6000	-	-	0.0630	-
F	-	0.2485	-	-	0.0098	-
G	-	0.4465	-	-	0.0176	-

Table 76. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 50. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint



1. Dimensions are expressed in millimeters.