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**What is "Embedded - Microcontrollers"?**

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

**Applications of "Embedded - Microcontrollers"**

| Details | |
| --- | --- |
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 10x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-UFQFN |
| Supplier Device Package | 28-UFQFPN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l041g6u6str |

# 2 Description

The access line ultra-low-power STM32L041x4/6 family incorporates the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, high-speed embedded memories (up to 32 Kbytes of Flash program memory, 1 Kbytes of data EEPROM and 8 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L041x4/6 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L041x4/6 devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, AES, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L041x4/6 devices embed standard and advanced communication interfaces: one I2C, one SPI, one USART, and a low-power UART (LPUART).

The STM32L041x4/6 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L041x4/6 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.

(if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USART/I2C/LPUART/LPTIMER wakeup events.

- **Stop mode without RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

  The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire $V_{CORE}$ domain is powered off. The PLL, MSI RC, HSE and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire $V_{CORE}$ domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

*Note:* *The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.*

### Table 3. Functionalities depending on the operating power supply range

| Operating power supply range | Functionalities depending on the operating power supply range | | |
|---|---|---|---|
| | ADC operation | Dynamic voltage scaling range | I/O operation |
| $V_{DD}$ = 1.65 to 1.71 V | Conversion time up to 570 ksps | Range 2 or range 3 | Degraded speed performance |
| $V_{DD}$ = 1.71 to 2.0 V[1] | Conversion time up to 1.14 Msps | Range 1, range 2 or range 3 | Degraded speed performance |
| $V_{DD}$ = 2.0 to 2.4 V | Conversion time up to 1.14 Msps | Range 1, range 2 or range 3 | Full speed operation |
| $V_{DD}$ = 2.4 to 3.6 V | Conversion time up to 1.14 Msps | Range 1, range 2 or range 3 | Full speed operation |

1. CPU frequency changes from initial to final must respect the condition: $f_{CPU\ initial} < 4f_{CPU\ initial}$. It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.

### Table 4. CPU frequency range depending on dynamic voltage scaling

| CPU frequency range | Dynamic voltage scaling range |
|---|---|
| 16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws) | Range 1 |
| 8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws) | Range 2 |
| 32 kHz to 4.2 MHz (0ws) | Range 3 |

### Table 5. Functionalities depending on the working mode (from Run/active down to standby) [1]

| IPs | Run/Active | Sleep | Low-power run | Low-power sleep | Stop | Wakeup capability | Standby | Wakeup capability |
|---|---|---|---|---|---|---|---|---|
| CPU | Y | -- | Y | -- | -- | | -- | |
| Flash memory | O | O | O | O | -- | | -- | |
| RAM | Y | Y | Y | Y | Y | | -- | |
| Backup registers | Y | Y | Y | Y | Y | | Y | |
| EEPROM | O | O | O | O | -- | | -- | |
| Brown-out reset (BOR) | O | O | O | O | O | O | O | O |
| DMA | O | O | O | O | -- | | -- | |
| Programmable Voltage Detector (PVD) | O | O | O | O | O | O | - | |

Note: *The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.*

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the $V_{PVD}$ threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD/VDDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

### 3.4.4 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA5, PA6, PA7), USART2 (PA2, PA3) or USART2 (PA9, PA10). See STM32™ microcontroller system memory boot mode AN2606 for details.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

## 3.11 Temperature sensor

The temperature sensor ($T_{SENSE}$) generates a voltage $V_{SENSE}$ that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

**Table 7. Temperature sensor calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| TSENSE_CAL1 | TS ADC raw data acquired at temperature of 30 °C, $V_{DDA}$= 3 V | 0x1FF8 007A - 0x1FF8 007B |
| TSENSE_CAL2 | TS ADC raw data acquired at temperature of 130 °C, $V_{DDA}$= 3 V | 0x1FF8 007E - 0x1FF8 007F |

### 3.11.1 Internal voltage reference ($V_{REFINT}$)

The internal voltage reference ($V_{REFINT}$) provides a stable (bandgap) voltage output for the ADC and Comparators. $V_{REFINT}$ is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the $V_{DD}$ value (since no external voltage, $V_{REF+}$, is available for ADC). The precise voltage of $V_{REFINT}$ is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

**Table 8. Internal voltage reference measured values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at temperature of 25 °C $V_{DDA}$ = 3 V | 0x1FF8 0078 - 0x1FF8 0079 |

### 3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

The USART interface (USART2) is able to communicate at speeds of up to 4 Mbit/s.

it provides hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART2 also supports Smartcard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock that allows to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

USART2 interface can be served by the DMA controller.

*Table 12* for the supported modes and features of USART interface.

**Table 12. USART implementation**

| USART modes/features[1] | USART2 |
|---|---|
| Hardware flow control for modem | X |
| Continuous communication using DMA | X |
| Multiprocessor communication | X |
| Synchronous mode[2] | X |
| Smartcard mode | X |
| Single-wire half-duplex communication | X |
| IrDA SIR ENDEC block | X |
| LIN mode | X |
| Dual clock domain and wakeup from Stop mode | X |
| Receiver timeout interrupt | X |
| Modbus communication | X |
| Auto baud rate detection (4 modes) | X |
| Driver Enable | X |

1. X = supported.

2. This mode allows using the USART as an SPI master.

### 3.16.3 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

• Start bit detection

• Or any received data frame

• Or a specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while

having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

### 3.16.4 Serial peripheral interface (SPI)

The SPI is able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The USARTs with synchronous capability can also be used as SPI master.

The SPI can be served by the DMA controller.

Refer to *Table 13* for the supported modes and features of SPI interface.

**Table 13. SPI implementation**

| SPI features[1] | SPI1 |
|---|---|
| Hardware CRC calculation | X |
| I2S mode | - |
| TI mode | X |

1. X = supported.

## 3.17 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

## 3.18 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

**Table 15. Pin definitions**

| Pin number | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP20 | WLCSP25 | UFQFPN28 | UFQFPN28 (STM32L041GxUxS only) | LQFP32 | UFQFPN32[1] | LQFP48 | | | | | | |
| - | - | - | - | - | - | 2 | PC13-ANTI_TAMP | I/O | FT | - | - | TAMP1/WKUP2 |
| 2 | B5 | 2 | 2 | 2 | 2 | 3 | PC14-OSC32_IN | I/O | TC | - | - | OSC32_IN |
| 3 | C5 | 3 | 3 | 3 | 3 | 4 | PC15-OSC32_OUT | I/O | TC | - | - | OSC32_OUT |
| - | - | - | - | - | - | 5 | PH0-OSC_IN | I/O | TC | - | - | - |
| - | - | - | - | - | - | 6 | PH1-OSC_OUT | I/O | TC | - | - | - |
| 4 | D5 | 4 | 4 | 4 | 4 | 7 | NRST | I/O | - | - | - | - |
| - | - | - | - | - | - | 1 | PC0 | I/O | FT | - | LPTIM1_IN1, EVENTOUT, LPUART1_RX | - |
| - | E1 | - | - | - | "0" | 8 | VSSA | S | - | - | - | - |
| 5 | C4 | 5 | 5 | 5 | 5 | 9 | VDDA | S | - | - | - | - |
| 6 | E5 | 6 | 6 | 6 | 6 | - | PA0-CK_IN | I/O | TC | - | LPTIM1_IN1, TIM2_CH1, USART2_CTS, TIM2_ETR, COMP1_OUT | COMP1_INM6, ADC_IN0, RTC_TAMP2/WKUP1 |
| - | - | - | - | - | - | 10 | PA0 | I/O | TC | - | LPTIM1_IN1, TIM2_CH1, USART2_CTS, TIM2_ETR, COMP1_OUT | COMP1_INM6, ADC_IN0, RTC_TAMP2/WKUP1 |

**Table 16. Alternate functions**

| Ports | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI1/USART2 /LPTIM/TIM21 /EVENTOUT/ SYS_AF | SPI1/I2C1/ LPTIM | LPTIM/TIM2/ EVENTOUT/ SYS_AF | I2C1/ EVENTOUT | I2C1/USART2/ LPUART1/ TIM22/ EVENTOUT | TIM2/21/22 | LPUART1/ EVENTOUT | COMP1/2 |
| Port A | PA0 | - | LPTIM1_IN1 | TIM2_CH1 | - | USART2_CTS | TIM2_ETR | - | COMP1_OUT |
| | PA1 | EVENTOUT | LPTIM1_IN2 | TIM2_CH2 | I2C1_SMBA | USART2_RTS | TIM21_ETR | - | - |
| | PA2 | TIM21_CH1 | - | TIM2_CH3 | - | USART2_TX | - | LPUART1_TX | COMP2_OUT |
| | PA3 | TIM21_CH2 | - | TIM2_CH4 | - | USART2_RX | - | LPUART1_RX | |
| | PA4 | SPI1_NSS | LPTIM1_IN1 | - | - | USART2_CK | TIM22_ETR | - | - |
| | PA5 | SPI1_SCK | LPTIM1_IN2 | TIM2_ETR | - | - | TIM2_CH1 | - | - |
| | PA6 | SPI1_MISO | LPTIM1_ETR | - | - | LPUART1_CTS | TIM22_CH1 | EVENTOUT | COMP1_OUT |
| | PA7 | SPI1_MOSI | LPTIM1_OUT | - | - | USART2_CTS | TIM22_CH2 | EVENTOUT | COMP2_OUT |
| | PA8 | MCO | - | LPTIM1_IN1 | EVENTOUT | USART2_CK | TIM2_CH1 | - | - |
| | PA9 | MCO | I2C1_SCL | - | - | USART2_TX | TIM22_CH1 | - | - |
| | PA10 | - | I2C1_SDA | - | - | USART2_RX | TIM22_CH2 | - | - |
| | PA11 | SPI1_MISO | - | EVENTOUT | - | USART2_CTS | TIM21_CH2 | - | COMP1_OUT |
| | PA12 | SPI1_MOSI | - | EVENTOUT | - | USART2_RTS | - | - | COMP2_OUT |
| | PA13 | SWDIO | LPTIM1_ETR | - | - | - | - | LPUART1_RX | - |
| | PA14 | SWCLK | LPTIM1_OUT | - | I2C1_SMBA | USART2_TX | - | LPUART1_TX | - |
| | PA15 | SPI1_NSS | - | TIM2_ETR | EVENTOUT | USART2_RX | TIM2_CH1 | - | - |

**Table 16. Alternate functions (continued)**

| Ports | | AF0 SPI1/USART2 /LPTIM/TIM21 /EVENTOUT/ SYS_AF | AF1 SPI1/I2C1/ LPTIM | AF2 LPTIM/TIM2/ EVENTOUT/ SYS_AF | AF3 I2C1/ EVENTOUT | AF4 I2C1/USART2/ LPUART1/ TIM22/ EVENTOUT | AF5 TIM2/21/22 | AF6 LPUART1/ EVENTOUT | AF7 COMP1/2 |
|---|---|---|---|---|---|---|---|---|---|
| Port B | PB0 | EVENTOUT | SPI1_MISO | - | - | USART2_RTS | TIM2_CH3 | - | - |
| | PB1 | USART2_CK | SPI1_MOSI | - | - | LPUART1_RTS | TIM2_CH4 | - | - |
| | PB2 | - | - | LPTIM1_OUT | - | - | - | - | - |
| | PB3 | SPI1_SCK | - | TIM2_CH2 | - | EVENTOUT | - | - | - |
| | PB4 | SPI1_MISO | - | EVENTOUT | - | TIM22_CH1 | - | - | - |
| | PB5 | SPI1_MOSI | - | LPTIM1_IN1 | I2C1_SMBA | TIM22_CH2 | - | - | - |
| | PB6 | USART2_TX | I2C1_SCL | LPTIM1_ETR | - | - | TIM21_CH1 | - | - |
| | PB7 | USART2_RX | I2C1_SDA | LPTIM1_IN2 | - | - | - | - | - |
| | PB8 | - | - | - | - | I2C1_SCL | - | - | - |
| | PB9 | - | - | EVENTOUT | - | I2C1_SDA | - | - | - |
| | PB10 | - | - | TIM2_CH3 | - | - | - | LPUART1_TX | - |
| | PB11 | EVENTOUT | - | TIM2_CH4 | - | - | - | LPUART1_RX | - |
| | PB12 | SPI1_NSS | - | - | - | - | - | EVENTOUT | - |
| | PB13 | SPI1_SCK | - | MCO | - | - | TIM21_CH1 | LPUART1_CTS | - |
| | PB14 | SPI1_MISO | - | RTC_OUT | - | - | TIM21_CH2 | LPUART1_RTS | - |
| | PB15 | SPI1_MOSI | - | RTC_REFIN | - | - | - | - | - |
| Port C | PC0 | LPTIM1_IN1 | - | EVENTOUT | - | - | - | LPUART1_RX | - |
| Port H | PH0 | - | - | - | - | - | - | - | - |
| | PH1 | - | - | - | - | - | - | - | - |

# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3.6 V (for the 1.65 V $\leq V_{DD} \leq$ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

### 6.1.5 Pin input voltage

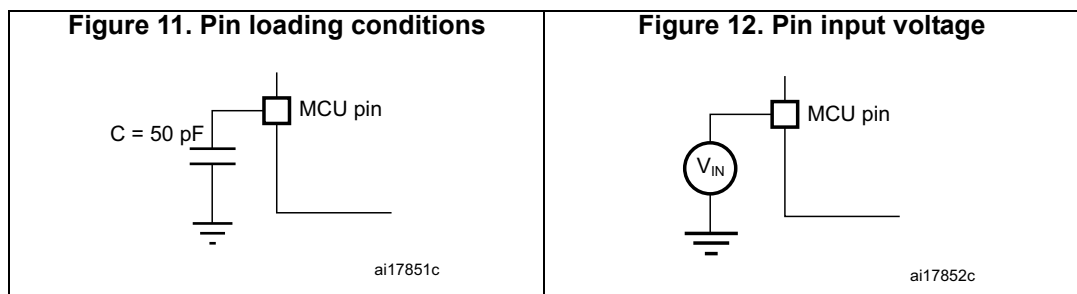The input voltage measurement on a pin of the device is described in *Figure 12*.

| Figure 11. Pin loading conditions | Figure 12. Pin input voltage |
|---|---|
|  |  |

**Table 21. Embedded reset and power control block characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $V_{BOR3}$ | Brown-out reset threshold 3 | Falling edge | 2.45 | 2.55 | 2.6 | V |
| | | Rising edge | 2.54 | 2.66 | 2.7 | |
| $V_{BOR4}$ | Brown-out reset threshold 4 | Falling edge | 2.68 | 2.8 | 2.85 | |
| | | Rising edge | 2.78 | 2.9 | 2.95 | |
| $V_{PVD0}$ | Programmable voltage detector threshold 0 | Falling edge | 1.8 | 1.85 | 1.88 | |
| | | Rising edge | 1.88 | 1.94 | 1.99 | |
| $V_{PVD1}$ | PVD threshold 1 | Falling edge | 1.98 | 2.04 | 2.09 | |
| | | Rising edge | 2.08 | 2.14 | 2.18 | |
| $V_{PVD2}$ | PVD threshold 2 | Falling edge | 2.20 | 2.24 | 2.28 | |
| | | Rising edge | 2.28 | 2.34 | 2.38 | |
| $V_{PVD3}$ | PVD threshold 3 | Falling edge | 2.39 | 2.44 | 2.48 | |
| | | Rising edge | 2.47 | 2.54 | 2.58 | |
| $V_{PVD4}$ | PVD threshold 4 | Falling edge | 2.57 | 2.64 | 2.69 | |
| | | Rising edge | 2.68 | 2.74 | 2.79 | |
| $V_{PVD5}$ | PVD threshold 5 | Falling edge | 2.77 | 2.83 | 2.88 | |
| | | Rising edge | 2.87 | 2.94 | 2.99 | |
| $V_{PVD6}$ | PVD threshold 6 | Falling edge | 2.97 | 3.05 | 3.09 | |
| | | Rising edge | 3.08 | 3.15 | 3.20 | |
| $V_{hyst}$ | Hysteresis voltage | BOR0 threshold | - | 40 | - | mV |
| | | All BOR and PVD thresholds excepting BOR0 | - | 100 | - | |

1. Guaranteed by characterization results.

2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

### 6.3.3 Embedded internal reference voltage

The parameters given in *Table 23* are based on characterization results, unless otherwise specified.

**Table 22. Embedded internal reference voltage calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at temperature of 25 °C, $V_{DDA}$= 3 V | 0x1FF8 0078 - 0x1FF8 0079 |

**Table 23. Embedded internal reference voltage[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT\ out}$[2] | Internal reference voltage | $-40\ °C < T_J < +125\ °C$ | 1.202 | 1.224 | 1.242 | V |
| $T_{VREFINT}$ | Internal reference startup time | - | - | 2 | 3 | ms |
| $V_{VREF\_MEAS}$ | $V_{DDA}$ voltage during $V_{REFINT}$ factory measure | - | 2.99 | 3 | 3.01 | V |
| $A_{VREF\_MEAS}$ | Accuracy of factory-measured $V_{REFINT}$ value[3] | Including uncertainties due to ADC and $V_{DDA}$ values | - | - | ±5 | mV |
| $T_{Coeff}$[4] | Temperature coefficient | $-40\ °C < T_J < +125\ °C$ | - | 25 | 100 | ppm/°C |
| $A_{Coeff}$[4] | Long-term stability | 1000 hours, T= 25 °C | - | - | 1000 | ppm |
| $V_{DDCoeff}$[4] | Voltage coefficient | $3.0\ V < V_{DDA} < 3.6\ V$ | - | - | 2000 | ppm/V |
| $T_{S\_vrefint}$[4][5] | ADC sampling time when reading the internal reference voltage | - | 5 | 10 | - | µs |
| $T_{ADC\_BUF}$[4] | Startup time of reference voltage buffer for ADC | - | - | - | 10 | µs |
| $I_{BUF\_ADC}$[4] | Consumption of reference voltage buffer for ADC | - | - | 13.5 | 25 | µA |
| $I_{VREF\_OUT}$[4] | VREF_OUT output current[6] | - | - | - | 1 | µA |
| $C_{VREF\_OUT}$[4] | VREF_OUT output load | - | - | - | 50 | pF |
| $I_{LPBUF}$[4] | Consumption of reference voltage buffer for VREF_OUT and COMP | - | - | 730 | 1200 | nA |
| $V_{REFINT\_DIV1}$[4] | 1/4 reference voltage | - | 24 | 25 | 26 | % $V_{REFINT}$ |
| $V_{REFINT\_DIV2}$[4] | 1/2 reference voltage | - | 49 | 50 | 51 | |
| $V_{REFINT\_DIV3}$[4] | 3/4 reference voltage | - | 74 | 75 | 76 | |

1. Refer to *Table 35: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption ($I_{REFINT}$).

2. Guaranteed by test in production.

3. The internal $V_{REF}$ value is individually measured in production and stored in dedicated EEPROM bytes.

4. Guaranteed by design.

5. Shortest sampling time can be determined in the application by multiple iterations.

6. To guarantee less than 1% VREF_OUT deviation.

**Figure 17. $I_{DD}$ vs $V_{DD}$, at $T_A$= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS**
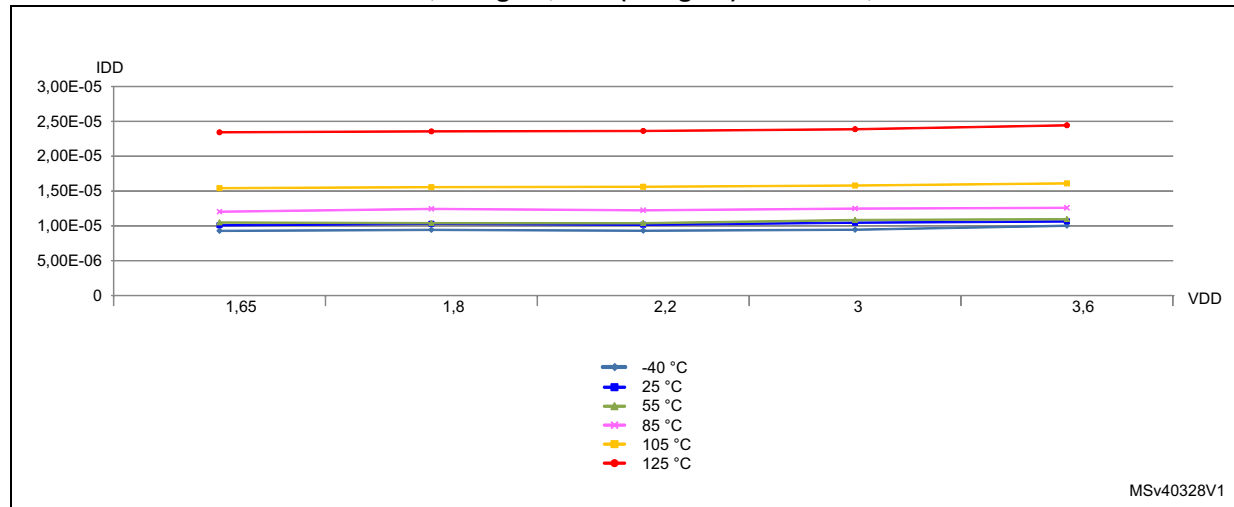


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**Table 30. Current consumption in Low-power Sleep mode**

| Symbol | Parameter | Conditions | | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ (LP Sleep) | Supply current in Low-power sleep mode | All peripherals off, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz Flash memory OFF / $T_A$ = -40 °C to 25 °C | 3.2[2] | - | µA |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz Flash memory ON / $T_A$ = -40 °C to 25 °C | 13 | 19 | |
| | | | $T_A$ = 85 °C | 16 | 21 | |
| | | | $T_A$ = 105 °C | 18.5 | 24 | |
| | | | $T_A$ = 125 °C | 23.5 | 32 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz, Flash memory ON / $T_A$ = -40 °C to 25 °C | 13.5 | 19 | |
| | | | $T_A$ = 85 °C | 16.5 | 21 | |
| | | | $T_A$ = 105 °C | 18.5 | 24 | |
| | | | $T_A$ = 125 °C | 24 | 33 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz, Flash memory ON / $T_A$ = -40 °C to 25 °C | 15.5 | 21 | |
| | | | $T_A$ = 55 °C | 17.5 | 22 | |
| | | | $T_A$ = 85 °C | 18.5 | 23 | |
| | | | $T_A$ = 105 °C | 21 | 26 | |
| | | | $T_A$ = 125 °C | 26 | 35 | |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

2. As the CPU is in Sleep mode, the difference between the current consumption with Flash memory ON and OFF (nearly 12 µA) is the same whatever the clock frequency.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 51. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|--------|-----------|------------|-------|
| LU | Static latch-up class | $T_A$ = +125 °C conforming to JESD78A | II level A |

## 6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the Table 52.

**Table 52. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|--------|-------------|------------|------------|------|
| | | **Negative injection** | **Positive injection** | |
| $I_{INJ}$ | Injected current on BOOT0 | -0 | NA | mA |
| | Injected current on PA0, PA2, PA4, PA5, PC15, PH0 and PH1 | -5 | 0 | |
| | Injected current on any other FT and FTf pin | -5 [1] | NA | |
| | Injected current on any other pin | -5 [1] | +5 | |

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

**Figure 25. V_IH/V_IL versus VDD (CMOS I/Os)**
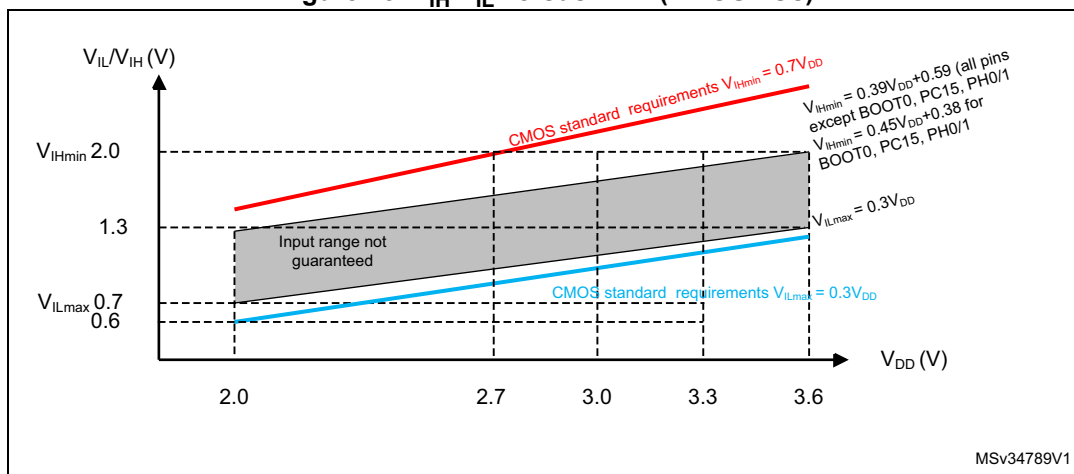


**Figure 26. V_IH/V_IL versus VDD (TTL I/Os)**
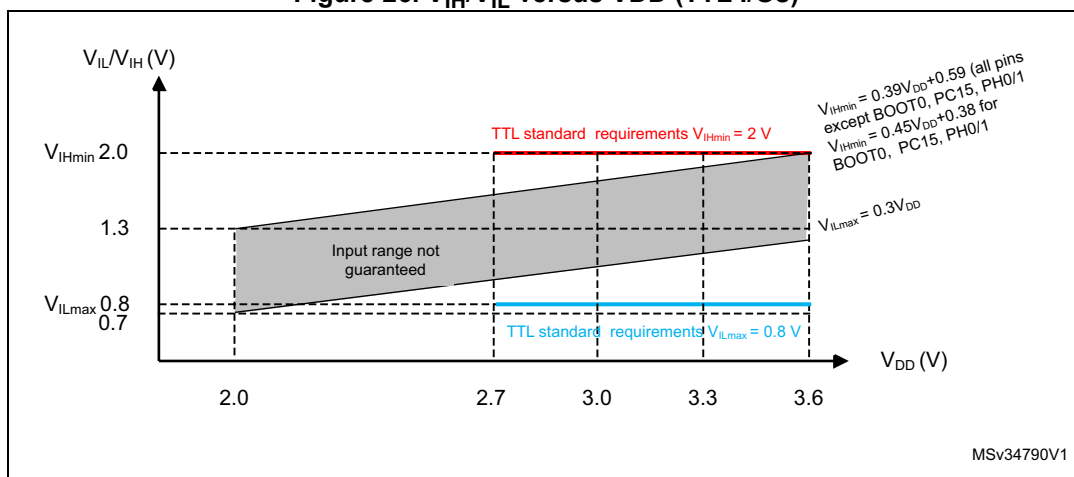


**Output driving current**

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±15 mA with the non-standard $V_{OL}/V_{OH}$ specifications given in *Table 54*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD}$, plus the maximum Run consumption of the MCU sourced on $V_{DD}$, cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 18*).

- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 18*).

**Table 57. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CAL}$[3] | Calibration time | $f_{ADC}$ = 16 MHz | | 5.2 | | µs |
| | | | | 83 | | $1/f_{ADC}$ |
| $W_{LATENCY}$ | ADC_DR register write latency | ADC clock = HSI16 | 1.5 ADC cycles + 2 $f_{PCLK}$ cycles | - | 1.5 ADC cycles + 3 $f_{PCLK}$ cycles | - |
| | | ADC clock = PCLK/2 | - | 4.5 | - | $f_{PCLK}$ cycle |
| | | ADC clock = PCLK/4 | - | 8.5 | - | $f_{PCLK}$ cycle |
| $t_{latr}$[3] | Trigger conversion latency | $f_{ADC}$ = $f_{PCLK}$/2 = 16 MHz | | 0.266 | | µs |
| | | $f_{ADC}$ = $f_{PCLK}$/2 | | 8.5 | | $1/f_{PCLK}$ |
| | | $f_{ADC}$ = $f_{PCLK}$/4 = 8 MHz | | 0.516 | | µs |
| | | $f_{ADC}$ = $f_{PCLK}$/4 | | 16.5 | | $1/f_{PCLK}$ |
| | | $f_{ADC}$ = $f_{HSI16}$ = 16 MHz | 0.252 | - | 0.260 | µs |
| $Jitter_{ADC}$ | ADC jitter on trigger conversion | $f_{ADC}$ = $f_{HSI16}$ | - | 1 | - | $1/f_{HSI16}$ |
| $t_S$[3] | Sampling time | $f_{ADC}$ = 16 MHz | 0.093 | - | 10.03 | µs |
| | | | 1.5 | - | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$[3] | Power-up time | | 0 | 0 | 1 | µs |
| $t_{ConV}$[3] | Total conversion time (including sampling time) | $f_{ADC}$ = 16 MHz | 0.875 | | 10.81 | µs |
| | | | 14 to 173 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. $V_{DDA}$ minimum value can be decreased in specific temperature conditions. Refer to *Table 58: RAIN max for fADC = 16 MHz*.

2. A current consumption proportional to the APB clock frequency has to be added (see *Table 34: Peripheral current consumption in Run or Sleep mode*).

3. Guaranteed by design.

4. Standard channels have an extra protection resistance which depends on supply voltage. Refer to *Table 58: RAIN max for fADC = 16 MHz*.

**Equation 1: $R_{AIN}$ max formula**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).
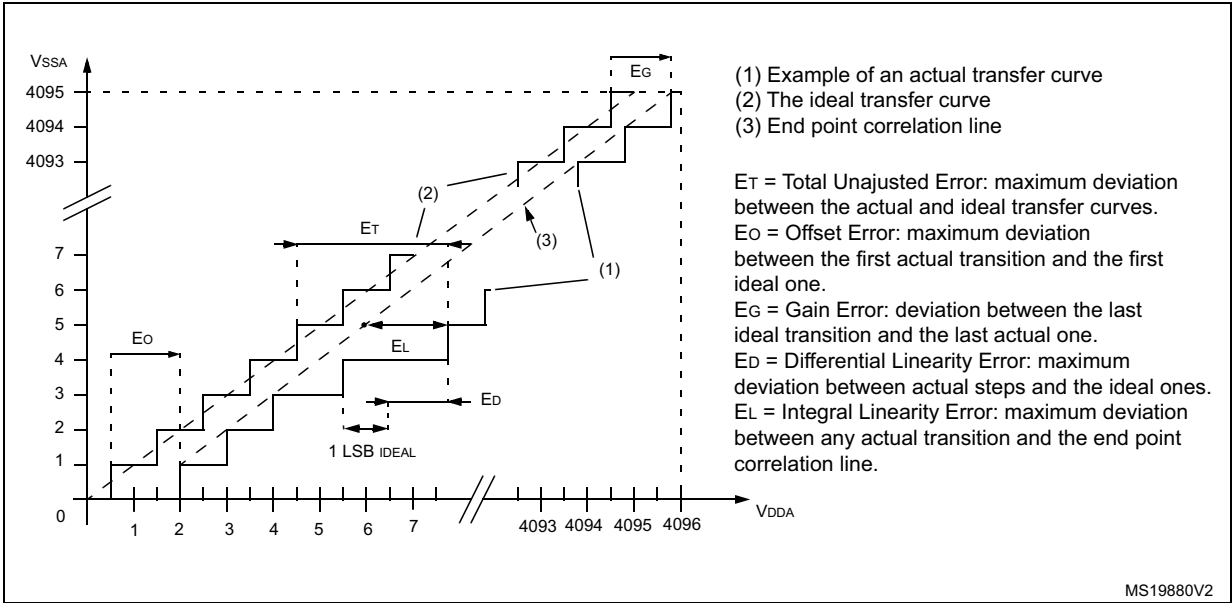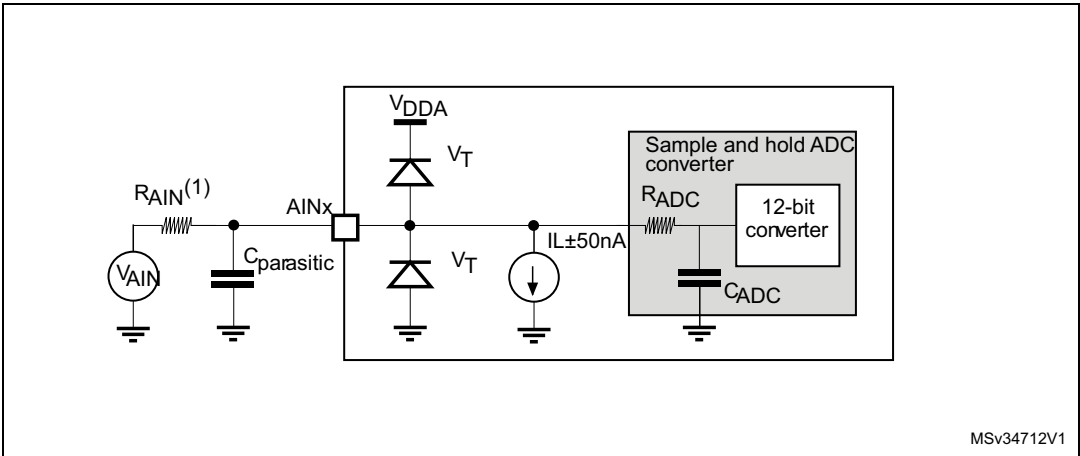
**Figure 29. ADC accuracy characteristics**



(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

$E_T$ = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
$E_O$ = Offset Error: maximum deviation between the first actual transition and the first ideal one.
$E_G$ = Gain Error: deviation between the last ideal transition and the last actual one.
$E_D$ = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
$E_L$ = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

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**Figure 30. Typical connection diagram using the ADC**



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1. Refer to *Table 57: ADC characteristics* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.

2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

## 6.3.16    Temperature sensor characteristics

**Table 60. Temperature sensor calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| TS_CAL1 | TS ADC raw data acquired at temperature of 30 °C, $V_{DDA}$= 3 V | 0x1FF8 007A - 0x1FF8 007B |
| TS_CAL2 | TS ADC raw data acquired at temperature of 130 °C $V_{DDA}$= 3 V | 0x1FF8 007E - 0x1FF8 007F |

**Table 70. LQFP48 - 48-pin low-profile quad flat package, 7 x 7 mm, package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 35. LQFP48 recommended footprint**



ai14911d
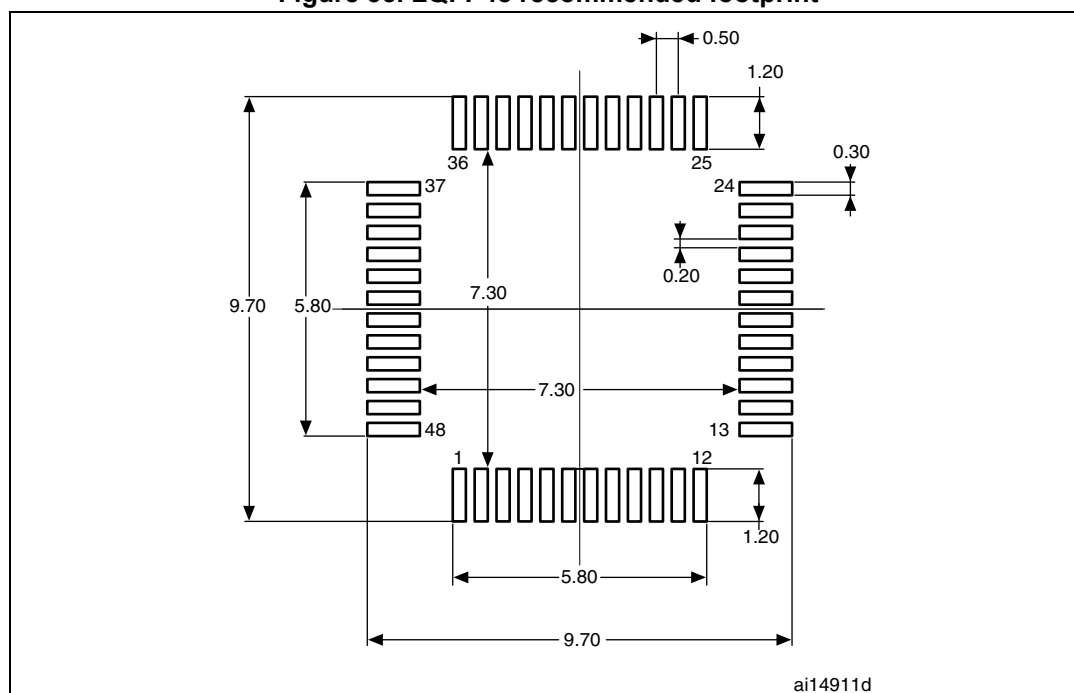
1.   Dimensions are expressed in millimeters.