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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l041k6u6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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			Low-	Low-		Stop	Standby	
IPs	Run/Active	Sleep	power run	power sleep		Wakeup capability		Wakeup capability
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	0	О			(2)			
High Speed External (HSE)	0	О	0	0				
Low Speed Internal (LSI)	0	О	0	0	0		0	
Low Speed External (LSE)	0	0	0	0	0		0	
Multi-Speed Internal (MSI)	0	0	Y	Y				
Inter-Connect Controller	Y	Y	Y	Y	Y			
RTC	0	0	0	0	0	0	0	
RTC Tamper	0	0	0	0	0	0	0	0
Auto WakeUp (AWU)	0	0	0	0	0	0	0	0
USART	0	0	0	0	O ⁽³⁾	0		
LPUART	0	0	0	0	O ⁽³⁾	0		
SPI	0	0	0	0				
12C	0	0	0	0	O ⁽⁴⁾	0		
ADC	0	0						
Temperature sensor	0	О	0	0	0			
Comparators	0	0	0	0	0	0		
16-bit timers	0	0	0	0				
LPTIMER	0	0	0	0	0	0		
IWDG	0	0	0	0	0	0	0	0
WWDG	0	0	0	0				
SysTick Timer	0	0	0	0				
GPIOs	0	0	0	0	0	0		2 pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs		3.5 µs		65 µs

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)⁽¹⁾





Figure 2. Clock tree



DocID027301 Rev 4

3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 26 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 38 GPIOs can be connected to the 16 configurable interrupt/event lines. The 10 other lines are connected to PVD, RTC, USART, I2C, LPUART, LPTIMER or comparator events.



3.8 Memories

The STM32L041x4/6 devices have the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
 - 16 or 32 Kbytes of embedded Flash program memory
 - 1 Kbytes of data EEPROM
 - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no protection
- Level 1: memory readout protected.

The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected

• Level 2: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: AES, SPI, I²C, USART, LPUART, general-purpose timers, and ADC.

3.10 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L041x4/6 devices. It has up to 10 external channels and 3 internal channels (temperature sensor, voltage reference). Three channel are fast channel, PA0, PA4 and PA5, while the others are standard channels.

It performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 μ A at 10 kSPS, ~200 μ A at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.



The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

3.11 Temperature sensor

The temperature sensor (T_{SENSE}) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Calibration value name	Description	Memory address
TSENSE_CAL1	TS ADC raw data acquired at temperature of 30 °C, V _{DDA} = 3 V	0x1FF8 007A - 0x1FF8 007B
TSENSE_CAL2	TS ADC raw data acquired at temperature of 130 °C, V _{DDA} = 3 V	0x1FF8 007E - 0x1FF8 007F

Table 7. Temperature sensor calibration values

3.11.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (since no external voltage, V_{REF+} , is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 8. Internal voltage reference measured values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V _{DDA} = 3 V	0x1FF8 0078 - 0x1FF8 0079



3.15 Timers and watchdogs

The ultra-low-power STM32L041x4/6 devices include three general-purpose timers, one low- power timer (LPTM), two watchdog timers and the SysTick timer.

Table 9 compares the features of the general-purpose and basic timers.

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No

Table 9. Timer feature compariso	วท
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3.15.1 General-purpose timers (TIM2, TIM21 and TIM22)

There are three synchronizable general-purpose timers embedded in the STM32L041x4/6 devices (see *Table 9* for differences).

TIM2

TIM2 is based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2 general-purpose timers can work together or with the TIM21 and TIM22 generalpurpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2 has independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together and be synchronized with the TIM2, full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.



Memory mapping 5



Figure 10. Memory map

1. Refer to the STM32L041x4/6 reference manual for details on the Flash memory organization for each memory size.



6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25$ °C and $T_A = T_Amax$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V \leq V_{DD} \leq 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.





6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is on, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock is applied to OSCI_IN input (LQFP48 package) and to CK_IN (other packages). It follows the characteristic specified in *Table 37: High-speed* external user clock characteristics
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption V_{DD} = V_{DDA} = 3.0 V is applied to all supply pins if not specified otherwise

The parameters given in *Table 44*, *Table 20* and *Table 21* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.



Symbol	Parameter	Conc	litions	f _{HCLK}	Тур	Max ⁽¹⁾	Unit
			Range 3.	1 MHz	36.5	87	
			V _{CORE} =1.2 V,	2 MHz	58	100	
		f f un to	VOS[1:0]=11	4 MHz	100	170	
		T _{HSE} = T _{HCLK} up to 16 MHz included.	Range 2.	4 MHz	125	190	
		$f_{HSE} = f_{HCLK}/2$	V _{CORE} =1.5 V,	8 MHz	230	310	
		above 16 MHz (PLL ON) ⁽²⁾	VOS[1:0]=10	16 MHz	450	540	
			Range 1,	8 MHz	275	360	
	Supply current		V _{CORE} =1.8 V,	16 MHz	555	650	
	mode, Flash		VOS[1:0]=01	32 MHz	1350	1600	
	memory OFF	HSI16 clock source	Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	16 MHz	585	690	
		(16 MHz)	Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	32 MHz	1500	1700	μΑ
		MSI clock	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	65 kHz	17	43	
				524 kHz	28	55	
				4.2 MHz	115	190	
IDD (Sleep)		$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON) ⁽²⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	1 MHz	49	160	
				2 MHz	69	190	
				4 MHz	115	230	
			Range 2, _{CORE} =1.5 V, VOS[1:0]=10	4 MHz	135	200	
				8 MHz	240	320	
				16 MHz	460	550	
			Range 1, V _{CORE} =1.8 V,	8 MHz	290	370	
	Supply current			16 MHz	565	670	
	mode, Flash		VOS[1:0]=01	32 MHz	1350	1600	
	memory ON	HSI16 clock source (16 MHz)	Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	16 MHz	600	700	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	32 MHz	1500	1700	
			Range 3.	65 kHz	28	55	
		MSI clock	V _{CORE} =1.2 V,	524 kHz	39.5	67	
			VOS[1:0]=11	4.2 MHz	125	200	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).



Low-speed external user clock generated from an external source

The characteristics given in the following table result from tests performed using a lowspeed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 20*.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{LSE_ext}	User external clock source frequency		1	32.768	1000	kHz
V _{LSEH}	OSC32_IN input pin high level voltage		0.7V _{DD}	-	V _{DD}	V
V _{LSEL}	OSC32_IN input pin low level voltage	-	V _{SS}	-	0.3V _{DD}	v
t _{w(LSE)} t _{w(LSE)}	OSC32_IN high or low time		465	-	-	ne
t _{r(LSE)} t _{f(LSE)}	OSC32_IN rise or fall time		-	-	10	115
C _{IN(LSE)}	OSC32_IN input capacitance	-	-	0.6	-	pF
DuCy _(LSE)	Duty cycle	-	45	-	55	%
١L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	μA

Table 38. Low-speed external user clock characteristics⁽¹⁾

1. Guaranteed by design.



Figure 21. Low-speed external clock source AC timing diagram



Cumb al	Devenueter	Conditions	Value	Unit
Symbol	Parameter	Conditions	Min ⁽¹⁾	
NCYC ⁽²⁾ Cycling (Program Cycling (EEPROM Cycling (Program Cycling (Program Cycling (EEPROM Data rete after 100 Data rete after 100	Cycling (erase / write) Program memory	T = 40°C to 105 °C	10	– kcycles
	Cycling (erase / write) EEPROM data memory		100	
	Cycling (erase / write) Program memory	T 10°C to 125 °C	0.2	
	Cycling (erase / write) EEPROM data memory		2	
	Data retention (program memory) after 10 kcycles at T _A = 85 °C	T = +85 °C	30	
	Data retention (EEPROM data memory) after 100 kcycles at $T_A = 85 \text{ °C}$	TRET - 105 C	30	
	Data retention (program memory) after 10 kcycles at T _A = 105 °C	T = +105 °C	- 10	years
RET	Data retention (EEPROM data memory) after 100 kcycles at $T_A = 105$ °C	TRET - 105 C		
	Data retention (program memory) after 200 cycles at T _A = 125 °C	T = +125 °C		
	Data retention (EEPROM data memory) after 2 kcycles at $T_A = 125 \degree C$	1 RET - 123 C		

Table 47 Flash memory	v and data EEPROM endurance and retent	tion

1. Guaranteed by characterization results.

2. Characterization is done according to JEDEC JESD22-A117.





Figure 29. ADC accuracy characteristics





^{1.} Refer to Table 57: ADC characteristics for the values of RAIN, RADC and CADC.

C_{parasitic} represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high C_{parasitic} value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.16 Temperature sensor characteristics

Table 60. Temperature sensor calibration values

Calibration value name	Description	Memory address		
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V _{DDA} = 3 V	0x1FF8 007A - 0x1FF8 007B		
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C V _{DDA} = 3 V	0x1FF8 007E - 0x1FF8 007F		



Symbol	Parameter	Min	Тур	Max	Unit
T _L ⁽¹⁾	V _{SENSE} linearity with temperature	-	±1	<u>+2</u>	°C
Avg_Slope ⁽¹⁾	Average slope	1.48	1.61	1.75	mV/°C
V ₁₃₀	Voltage at 130°C ±5°C ⁽²⁾	640	670	700	mV
I _{DDA(TEMP)} ⁽³⁾	Current consumption	-	3.4	6	μA
t _{START} ⁽³⁾	Startup time	-	-	10	
T _{S_temp} ⁽⁴⁾⁽³⁾	ADC sampling time when reading the temperature	10	-	-	μs

Table 61. Temperature sensor characteristics

1. Guaranteed by characterization results.

2. Measured at V_{DD} = 3 V ±10 mV. V130 ADC conversion result is stored in the TS_CAL2 byte.

3. Guaranteed by design.

4. Shortest sampling time can be determined in the application by multiple iterations.

6.3.17 Comparators

<u> </u>			··· (1)	-	aa (1)	
Symbol	Parameter	Conditions	Min(")	Тур	Max	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R _{400K}	R _{400K} value	-	-	400	-	kO
R _{10K}	R _{10K} value	-	-	10	-	N22
V _{IN}	Comparator 1 input voltage range	-	0.6	-	V _{DDA}	V
t _{START}	Comparator startup time	-	-	7	10	116
td	Propagation delay ⁽²⁾	-	-	3	10	μο
Voffset	Comparator offset	-	-	±3	±10	mV
d _{Voffset} /dt	Comparator offset variation in worst voltage stress conditions	$V_{DDA} = 3.6 V$ $V_{IN+} = 0 V$ $V_{IN-} = V_{REFINT}$ $T_A = 25 ° C$	0	1.5	10	mV/1000 h
I _{COMP1}	Current consumption ⁽³⁾	-	-	160	260	nA

Table 62. Comparator 1 characteristics

1. Guaranteed by characterization.

2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

3. Comparator consumption only. Internal reference voltage not included.



Symbol	Parameter	Conditions	Min	Тур	Max ⁽¹⁾	Unit
V _{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V _{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t	Comparator startun time	Fast mode	-	- 15 20		
START		Slow mode	-	20	25	
t _{d slow}	Propagation dolay ⁽²⁾ in slow mode	1.65 V ⊴V _{DDA} ⊴2.7 V	-	1.8	3.5	
	Fropagation delay in slow mode	2.7 V ≤V _{DDA} ≤3.6 V	-	2.5	6	μs
4	Propagation dolay ⁽²⁾ in fact mode	1.65 V ⊴V _{DDA} ⊴2.7 V	-	0.8	2	
^L d fast	Fropagation delay in last mode	2.7 V ≤V _{DDA} ≤3.6 V	-	1.2	4	
V _{offset}	Comparator offset error		-	±4	±20	mV
dThreshold/ dt	Threshold voltage temperature coefficient	$V_{DDA} = 3.3V$ $T_{A} = 0 \text{ to } 50 \circ C$ $V = V_{REFINT},$ $3/4 V_{REFINT},$ $1/2 V_{REFINT},$ $1/4 V_{REFINT}.$	-	15	30	ppm /°C
I _{COMP2}	Current consumption ⁽³⁾	Fast mode	- 3.5 5		5	_
		Slow mode	-	0.5	2	μΑ

Table 63. Comparator 2 characteristics

1. Guaranteed by characterization results.

2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

6.3.18 Timer characteristics

TIM timer characteristics

The parameters given in the *Table 64* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Symbol	Parameter	Conditions	Min	Мах	Unit
t Timor resolution time			1	-	t _{TIMxCLK}
res(TIM)		f _{TIMxCLK} = 32 MHz	31.25	-	ns
f	Timer external clock		0	f _{TIMxCLK} /2	MHz
^I EXT	frequency on CH1 to CH4	f _{TIMxCLK} = 32 MHz	0	16	MHz
Res _{TIM}	Timer resolution	-		16	bit

Table 64. TIMx⁽¹⁾ characteristics



7.3 UFQFPN32 package information



Figure 40. UFQFPN32, 5 x 5 mm, 32-pin package outline

1. Drawing is not to scale.

Table 72. UFQFPN32, 5 x 5 mm, 32-pin package mechanical data

Sympol	millimeters			inches ⁽¹⁾			
Symbol	Min	Тур	Мах	Min	Тур	Max	
А	0.500	0.550	0.600	0.0197	0.0217	0.0236	
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020	
A3	-	0.200	-	-	0.0079	-	
b	0.180	0.250	0.300	0.0071	0.0098	0.0118	
D	4.900	5.000	5.100	0.1929	0.1969	0.2008	
D2	3.200	3.450	3.700	0.1260	0.1358	0.1457	
E	4.900	5.000	5.100	0.1929	0.1969	0.2008	
E2	3.200	3.450	3.700	0.1260	0.1358	0.1457	
е	-	0.500	-	-	0.0197	-	
L	0.300	0.400	0.500	0.0118	0.0157	0.0197	
ddd	-	-	0.080	-	-	0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.





Figure 41. UFQFPN32 recommended footprint

1. Dimensions are expressed in millimeters.

UFQFPN32 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.



Figure 42. Example of UFQFPN32 marking (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



7.5 WLCSP25 package information



Figure 46. WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale package outline

Table 74. WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale
mechanical data

Symbol	Milimeters			Inches ⁽¹⁾		
Symbol	Min	Тур	Мах	Min	Тур	Мах
А	0.5250	0.5550	0.5850	0.0207	0.0219	0.0230
A1	-	0.1750	-	-	0.0069	-
A2	-	0.3800	-	-	0.0150	-
A3 ⁽²⁾	-	0.0250	-	-	0.0010	-
b ⁽³⁾	0.2200	0.2500	0.2800	0.0087	0.0098	0.0110
D	2.0620	2.0970	2.1320	0.0812	0.0826	0.0839
E	2.4580	2.4930	2.5280	0.0968	0.0981	0.0995
е	-	0.4000	-	-	0.0157	-
e1	-	1.6000	-	-	0.0630	-
e2	-	1.6000	-	-	0.0630	-
F	-	0.2485	-	-	0.0098	-
G	-	0.4465	-	-	0.0176	-

