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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l041k6u6tr

2 Description

The access line ultra-low-power STM32L041x4/6 family incorporates the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, high-speed embedded memories (up to 32 Kbytes of Flash program memory, 1 Kbytes of data EEPROM and 8 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L041x4/6 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L041x4/6 devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, AES, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L041x4/6 devices embed standard and advanced communication interfaces: one I2C, one SPI, one USART, and a low-power UART (LPUART).

The STM32L041x4/6 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L041x4/6 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.



3.12 Ultra-low-power comparators and reference voltage

The STM32L041x4/6 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
 - External I/O pins
 - Internal reference voltage (V_{REFINT})
 - submultiple of Internal reference voltage (1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 μ A typical).

3.13 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM21, TIM22 and LPTIM timer input captures. It also controls the routing of internal analog signals to the ADC, COMP1 and COMP2 and the internal reference voltage V_{REFINT} .

3.14 AES

The AES Hardware Accelerator can be used to encrypt and decrypt data using the AES algorithm (compatible with FIPS PUB 197, 2001 Nov 26):

- Key scheduler
- Key derivation for decryption
- 128-bit data block processed
- 128-bit key length
- 213 clock cycles to encrypt/decrypt one 128-bit block
- Electronic codebook (ECB), cypher block chaining (CBC), and counter mode (CTR) supported by hardware.

The AES can be served by the DMA controller.

3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

The USART interface (USART2) is able to communicate at speeds of up to 4 Mbit/s.

it provides hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART2 also supports Smartcard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock that allows to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

USART2 interface can be served by the DMA controller.

[Table 12](#) for the supported modes and features of USART interface.

Table 12. USART implementation

USART modes/features ⁽¹⁾	USART2
Hardware flow control for modem	X
Continuous communication using DMA	X
Multiprocessor communication	X
Synchronous mode ⁽²⁾	X
Smartcard mode	X
Single-wire half-duplex communication	X
IrDA SIR ENDEC block	X
LIN mode	X
Dual clock domain and wakeup from Stop mode	X
Receiver timeout interrupt	X
Modbus communication	X
Auto baud rate detection (4 modes)	X
Driver Enable	X

1. X = supported.

2. This mode allows using the USART as an SPI master.

3.16.3 Low-power universal asynchronous receiver transmitter (LPUART)

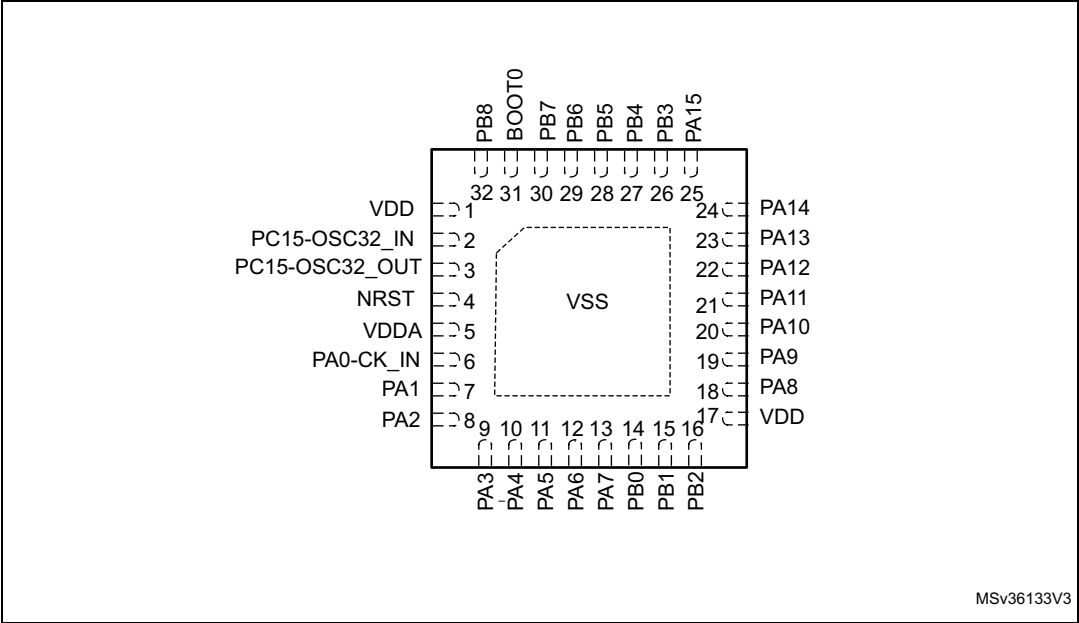
The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Or any received data frame
- Or a specific programmed data frame

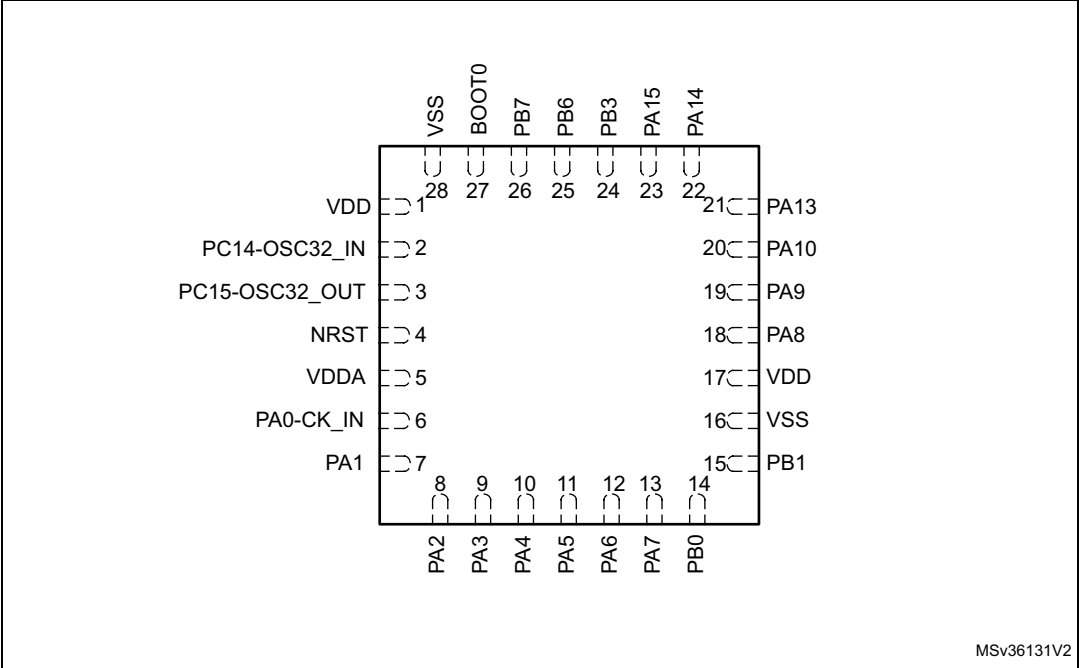
Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while

Figure 5. STM32L041x4/6 UFQFPN32 pinout



1. The above figure shows the package top view.

Figure 6. STM32L041x4/6 UFQFPN28 pinout



1. The above figure shows the package top view.
2. This pinout applies to all part numbers except for STM32L041GxUxS.

Table 15. Pin definitions (continued)

Pin number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25	UFQFPN28	UFQFPN28 (STM32L041GxUxS only)	LQFP32	UFQFPN32 ⁽¹⁾	LQFP48						
-	-	-	-	-	-	35	VSS	S	-	-	-	-
-	D1	-	-	-	-	36	VDD	S	-	-	-	-
20	A2	22	22	24	24	37	PA14	I/O	FT	-	SWCLK, LPTIM1_OUT, I2C1_SMBA, USART2_TX, LPUART1_TX	-
-	-	23	23	25	25	38	PA15	I/O	FT	-	SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1	--
-	B2	24	24	26	26	39	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, EVENTOUT	COMP2_INN
-	-	-	25	27	27	40	PB4	I/O	FT	-	SPI1_MISO, EVENTOUT, TIM22_CH1	COMP2_INP
-	-	-	26	28	28	41	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM22_CH2	COMP2_INP
-	A3	25	27	29	29	42	PB6	I/O	FTf	-	USART2_TX, I2C1_SCL, LPTIM1_ETR, TIM21_CH1	COMP2_INP
-	A4	26	28	30	30	43	PB7	I/O	FTf	-	USART2_RX, I2C1_SDA, LPTIM1_IN2	COMP2_INP, VREF_PVD_IN

Table 15. Pin definitions (continued)

Pin number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25	UFQFPN28	UFQFPN28 (STM32L041GxUxS only)	LQFP32	UFQFPN32 ⁽¹⁾	LQFP48						
1	A5	27	1	31	31	44	BOOT0	I	-	-	-	-
-	-	-	-	-	32	45	PB8	I/O	FTf	-	I2C1_SCL	-
-	-	-	-	-	-	46	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA	-
-	-	28	-	32	-	47	VSS	S	-	-	-	-
-	-	1	-	1	1	48	VDD	S	-	-	-	-

1. VSS pins are connected to the exposed pad (see [Figure 40: UFQFPN32, 5 x 5 mm, 32-pin package outline](#)).

Table 16. Alternate functions (continued)

Ports		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/USART2/ LPTIM/TIM21 /EVENTOUT/ SYS_AF	SPI1/I2C1/ LPTIM	LPTIM/TIM2/ EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART2/ LPUART1/ TIM22/ EVENTOUT	TIM2/21/22	LPUART1/ EVENTOUT	COMP1/2
Port B	PB0	EVENTOUT	SPI1_MISO	-	-	USART2_RTS	TIM2_CH3	-	-
	PB1	USART2_CK	SPI1_MOSI	-	-	LPUART1_RTS	TIM2_CH4	-	-
	PB2	-	-	LPTIM1_OUT	-	-	-	-	-
	PB3	SPI1_SCK	-	TIM2_CH2	-	EVENTOUT	-	-	-
	PB4	SPI1_MISO	-	EVENTOUT	-	TIM22_CH1	-	-	-
	PB5	SPI1_MOSI	-	LPTIM1_IN1	I2C1_SMBA	TIM22_CH2	-	-	-
	PB6	USART2_TX	I2C1_SCL	LPTIM1_ETR	-	-	TIM21_CH1	-	-
	PB7	USART2_RX	I2C1_SDA	LPTIM1_IN2	-	-	-	-	-
	PB8	-	-	-	-	I2C1_SCL	-	-	-
	PB9	-	-	EVENTOUT	-	I2C1_SDA	-	-	-
	PB10	-	-	TIM2_CH3	-	-	-	LPUART1_TX	-
	PB11	EVENTOUT	-	TIM2_CH4	-	-	-	LPUART1_RX	-
	PB12	SPI1_NSS	-	-	-	-	-	EVENTOUT	-
	PB13	SPI1_SCK	-	MCO	-	-	TIM21_CH1	LPUART1_CTS	-
	PB14	SPI1_MISO	-	RTC_OUT	-	-	TIM21_CH2	LPUART1_RTS	-
	PB15	SPI1_MOSI	-	RTC_REFIN	-	-	-	-	-
Port C	PC0	LPTIM1_IN1	-	EVENTOUT	-	-	-	LPUART1_RX	-
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 17: Voltage characteristics](#), [Table 18: Current characteristics](#), and [Table 19: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 17. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including V_{DDA} , V_{DD}) ⁽¹⁾	-0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on FT and FTf pins	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on TC pins	$V_{SS} - 0.3$	4.0	
	Input voltage on BOOT0	V_{SS}	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$ \Delta V_{DD} $	Variations between different V_{DDx} power pins	-	50	mV
$ V_{DDA}-V_{DDx} $	Variations between any V_{DDx} and V_{DDA} power pins ⁽³⁾	-	300	
$ \Delta V_{SS} $	Variations between all different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 6.3.11		

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 18](#) for maximum allowed injected current values.
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and device operation.

2. HSI oscillator is off for this measure.
3. Current consumption is negligible and close to 0 μA .

Table 35. Peripheral current consumption in Stop and Standby mode⁽¹⁾

Symbol	Peripheral	Typical consumption, $T_A = 25\text{ }^\circ\text{C}$		Unit
		$V_{DD}=1.8\text{ V}$	$V_{DD}=3.0\text{ V}$	
$I_{DD(PVD / BOR)}$	-	0.7	1.2	μA
I_{REFINT}	-	1.3	1.4	
-	LSE Low drive ⁽²⁾	0.1	0.1	
-	LSI	0.27	0.31	
-	IWDG	0.2	0.3	
-	LPTIM1, Input 100 Hz	0.01	0.01	
-	LPTIM1, Input 1 MHz	6	6	
-	LPUART1	0.2	0.2	
-	RTC (LSE in Bypass mode)	0.2	0.2	

1. LPTIM, LPUART peripherals can operate in Stop mode but not in Standby mode
2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#).

Table 47. Flash memory and data EEPROM endurance and retention

Symbol	Parameter	Conditions	Value	Unit
			Min ⁽¹⁾	
N _{CYC} ⁽²⁾	Cycling (erase / write) Program memory	T _A = -40°C to 105 °C	10	kcycles
	Cycling (erase / write) EEPROM data memory		100	
	Cycling (erase / write) Program memory	T _A = -40°C to 125 °C	0.2	
	Cycling (erase / write) EEPROM data memory		2	
t _{RET} ⁽²⁾	Data retention (program memory) after 10 kcycles at T _A = 85 °C	T _{RET} = +85 °C	30	years
	Data retention (EEPROM data memory) after 100 kcycles at T _A = 85 °C		30	
	Data retention (program memory) after 10 kcycles at T _A = 105 °C	T _{RET} = +105 °C	10	
	Data retention (EEPROM data memory) after 100 kcycles at T _A = 105 °C			
	Data retention (program memory) after 200 cycles at T _A = 125 °C	T _{RET} = +125 °C		
	Data retention (EEPROM data memory) after 2 kcycles at T _A = 125 °C			

1. Guaranteed by characterization results.

2. Characterization is done according to JEDEC JESD22-A117.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 49. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. f_{osc}/f_{CPU}	Unit
				8 MHz/32 MHz	
S _{EMI}	Peak level	V _{DD} = 3.6 V, T _A = 25 °C, LQFP48 package conforming to IEC61967-2	0.1 to 30 MHz	-10	dBμV
			30 to 130 MHz	5	
			130 MHz to 1GHz	-5	
			EMI Level	1.5	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 50. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C, conforming to ANSI/JEDEC JS-001	2	2000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T _A = +25 °C, conforming to ANSI/ESD STM5.3.1.	C4	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 51. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +125\text{ }^{\circ}\text{C}$ conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of $-5\text{ }\mu\text{A}/+0\text{ }\mu\text{A}$ range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the [Table 52](#).

Table 52. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PA0, PA2, PA4, PA5, PC15, PH0 and PH1	-5	0	
	Injected current on any other FT and FTf pin	-5 ⁽¹⁾	NA	
	Injected current on any other pin	-5 ⁽¹⁾	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Output voltage levels

Unless otherwise specified, the parameters given in [Table 54](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#). All I/Os are CMOS and TTL compliant.

Table 54. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ , $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ , $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin	TTL port ⁽²⁾ , $I_{IO} = -6 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	2.4	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = +15 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	1.3	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin	$I_{IO} = -15 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD}-1.3$	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = +4 \text{ mA}$ $1.65 \text{ V} \leq V_{DD} < 3.6 \text{ V}$	-	0.45	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin	$I_{IO} = -4 \text{ mA}$ $1.65 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD}-0.45$	-	
$V_{OLFM+}^{(1)(4)}$	Output low level voltage for an FTf I/O pin in Fm+ mode	$I_{IO} = 20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	
		$I_{IO} = 10 \text{ mA}$ $1.65 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 18](#). The sum of the currents sunk by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 18](#). The sum of the currents sourced by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
4. Guaranteed by characterization results.

Table 63. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
V _{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V _{IN}	Comparator 2 input voltage range	-	0	-	V _{DDA}	V
t _{START}	Comparator startup time	Fast mode	-	15	20	μs
		Slow mode	-	20	25	
t _{d slow}	Propagation delay ⁽²⁾ in slow mode	1.65 V ≤ V _{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V _{DDA} ≤ 3.6 V	-	2.5	6	
t _{d fast}	Propagation delay ⁽²⁾ in fast mode	1.65 V ≤ V _{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V _{DDA} ≤ 3.6 V	-	1.2	4	
V _{offset}	Comparator offset error		-	±4	±20	mV
dThreshold/ dt	Threshold voltage temperature coefficient	V _{DDA} = 3.3V T _A = 0 to 50 °C V ₋ = V _{REFINT} , 3/4 V _{REFINT} , 1/2 V _{REFINT} , 1/4 V _{REFINT}	-	15	30	ppm / °C
I _{COMP2}	Current consumption ⁽³⁾	Fast mode	-	3.5	5	μA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

6.3.18 Timer characteristics

TIM timer characteristics

The parameters given in the [Table 64](#) are guaranteed by design.

Refer to [Section 6.3.13: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 64. TIMx⁽¹⁾ characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t _{res(TIM)}	Timer resolution time		1	-	t _{TIMxCLK}
		f _{TIMxCLK} = 32 MHz	31.25	-	ns
f _{EXT}	Timer external clock frequency on CH1 to CH4		0	f _{TIMxCLK} /2	MHz
		f _{TIMxCLK} = 32 MHz	0	16	MHz
Res _{TIM}	Timer resolution	-		16	bit

SPI characteristics

Unless otherwise specified, the parameters given in the following tables are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 20](#).

Refer to [Section 6.3.12: I/O current injection characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 67. SPI characteristics in voltage Range 1 ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	16	MHz
		Slave mode receiver			16	
		Slave mode Transmitter $1.71 < V_{DD} < 3.6V$	-	-	12 ⁽²⁾	
		Slave mode Transmitter $2.7 < V_{DD} < 3.6V$	-	-	16 ⁽²⁾	
Duty _(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4* T_{pclk}	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2* T_{pclk}	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	$T_{pclk}-2$	T_{pclk}	$T_{pclk}+2$	
$t_{su(MI)}$	Data input setup time	Master mode	8.5	-	-	
$t_{su(SI)}$		Slave mode	8.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	15	-	36	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	30	
$t_{v(SO)}$	Data output valid time	Slave mode $1.71 < V_{DD} < 3.6V$	-	29	41	
		Slave mode $2.7 < V_{DD} < 3.6V$	-	22	28	
$t_{v(MO)}$		Master mode	-	10	17	
$t_{h(SO)}$	Data output hold time	Slave mode	9	-	-	
$t_{h(MO)}$		Master mode	3	-	-	

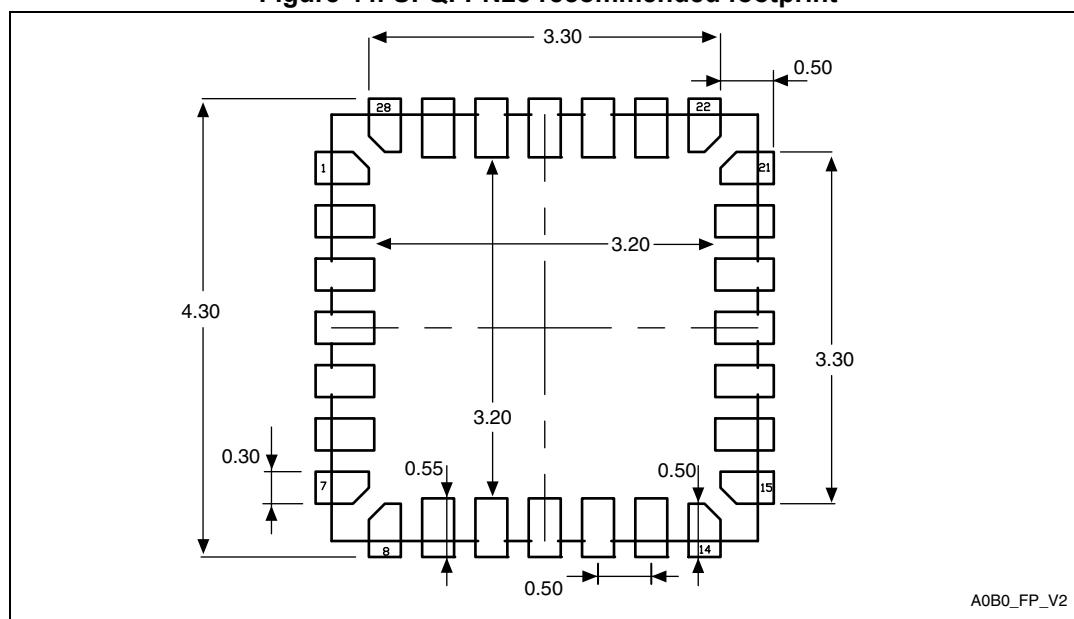
1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while Duty_(SCK) = 50%.

Table 70. LQFP48 - 48-pin low-profile quad flat package, 7 x 7 mm, package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. UFQFPN28 recommended footprint



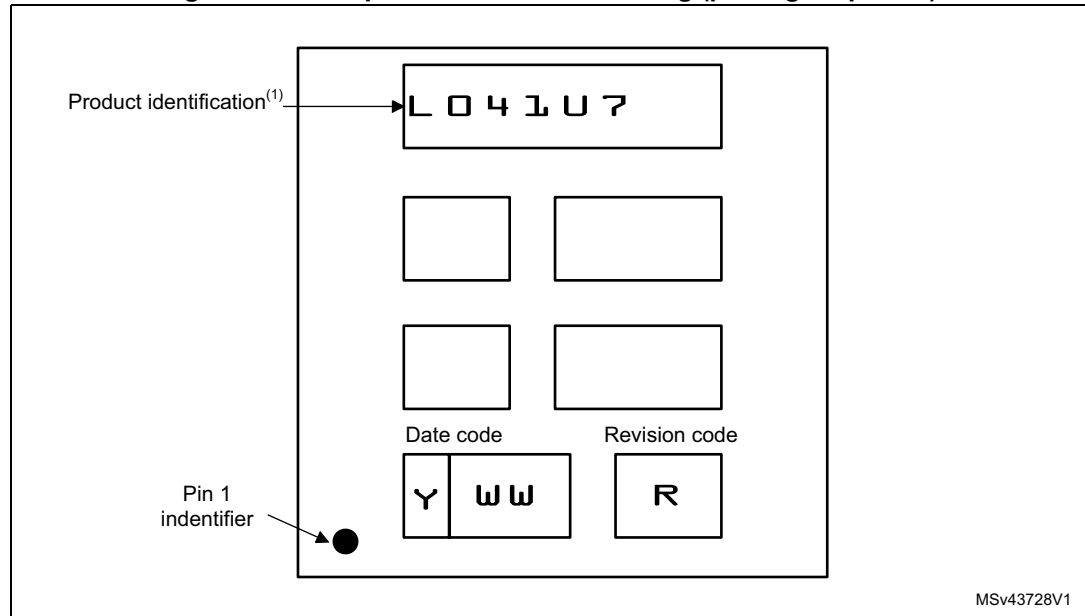
1. Dimensions are expressed in millimeters.

UFQFPN28 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 45. Example of UFQFPN28 marking (package top view)



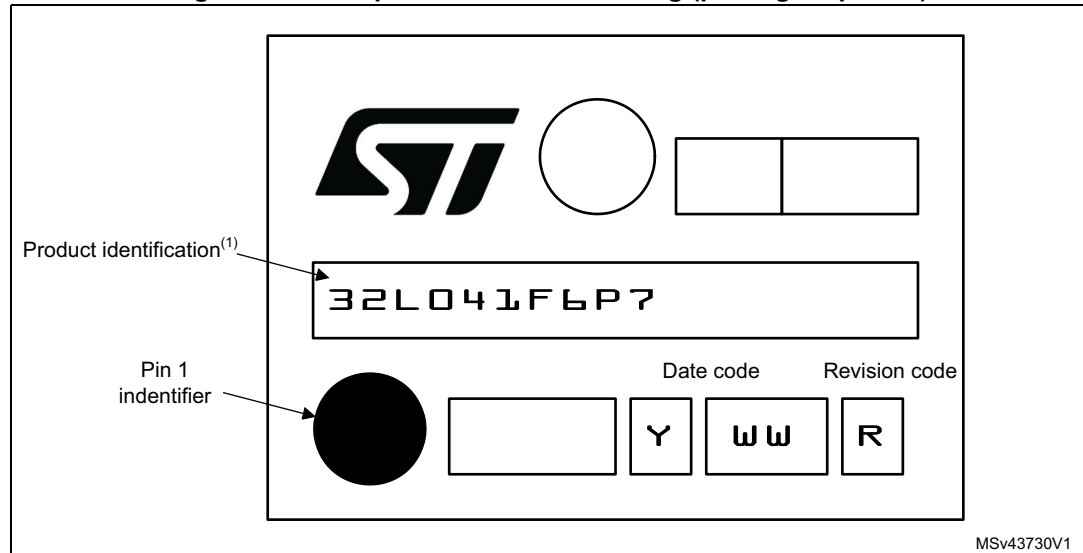
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

TSSOP20 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 51. Example of TSSOP20 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

9 Revision history

Table 79. Document revision history

Date	Revision	Changes
10-Nov-2015	1	Initial release.
14-Mar-2016	2	<p>Updated number of SPI interfaces on cover page and in Table 2: Ultra-low-power STM32L041x4/x6 device features and peripheral counts.</p> <p>Updated number of GPIOs for devices in UFQFPN28 in Table 2: Ultra-low-power STM32L041x4/x6 device features and peripheral counts.</p> <p>Updated Section 3.4.4: Boot modes.</p> <p>Updated Section 3.16.2: Universal synchronous/asynchronous receiver transmitter (USART) and Section 3.16.4: Serial peripheral interface (SPI) to mention the fact that USARTs with synchronous mode feature can be used as SPI master interfaces.</p> <p>Modified pin 2 in Figure 5: STM32L041x4/6 UFQFPN32 pinout.</p> <p>Added Figure 7: STM32L041GxUxS UFQFPN28 pinout.</p> <p>Table 15: Pin definitions:</p> <ul style="list-style-type: none"> – Added UFQFPN28 for STM32L041GxUxS part number. – Renamed PA0-WKUP-CK_IN into PA0-CK_IN – Renamed PA0-WKUP into PA0 <p>Updated Table 18: Current characteristics to add the total output current for STM32L031GxUxS.</p> <p>Added one power pair option in Table 78: STM32L041x4/6 ordering information scheme.</p>