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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	LCD, Motor control PWM, POR, PWM, WDT
Number of I/O	91
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.75V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s12hz128j3cal

1.3 Part ID Assignments and Mask Set Numbers

The part ID is located in two 8-bit registers PARTIDH and PARTIDL at addresses 0x001A and 0X001B, respectively. The rado-only value is a unique part ID for each revision of the chip. Table 1-6 shows the assigned part ID and Mask Set numbers.

Table 1-6. Assigned Part ID and Mask Set Numbers

Part Names	Mask Set	Part ID[1]
MC9S12HZ256 MC9S12HZ128 MC9S12HZ64 MC9S12HN64 MC3S12HZ256 MC3S12HZ128	2L16Y/3L16Y	0x1402/0x1403
MC3S12HZ64 MC3S12HN64 MC3S12HZ32 MC3S12HN32	1M36C	0x1501

[1] The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-8: Minor family identifier
Bit 7-4: Major mask set revision including fab transfers
Bit 3-0: Minor non-full mask set revision

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMZI1 (addresses 0x001C and 0x001D after reset). Table 1-7 shows the read-only values of these registers. Refer to the HCS12 MMC block description chapter for further details.

Table 1-7. Memory Size Registers

Part Names	MEMSIZ0	MEMSIZ1
MC9S12HZ256 MC9S12HZ128 MC9S12HZ64 MC9S12HN64 MC3S12HZ256 MC3S12HZ128	0x15	0x81
MC3S12HZ64 MC3S12HN64 MC3S12HZ32 MC3S12HN32	0x01	0x80

1.5.6.19 PM2 / RXCAN0 — Port M I/O Pin 2

PM2 is a general-purpose input or output pin. It can be configured as the receive pin RXCAN0 of the scalable controller area network controller 0 (CAN0)

1.5.6.20 PP5 / PWM5 — Port P I/O Pin 5

PP5 is a general-purpose input or output pin. It can be configured as pulse width modulator (PWM) channel output PWM5 or the serial clock pin SCL of the inter-IC bus interface (IIC).

1.5.6.21 PP4 / PWM4 — Port P I/O Pin 4

PP4 is a general-purpose input or output pin. It can be configured as pulse width modulator (PWM) channel output PWM4 or the serial data pin SDA of the inter-IC bus interface (IIC).

1.5.6.22 PP3 / PWM3 — Port P I/O Pin 3

PP3 is a general-purpose input or output pin. It can be configured as pulse width modulator (PWM) channel output PWM3.

1.5.6.23 PP2 / PWM2 — Port P I/O Pin 2

PP2 is a general-purpose input or output pin. It can be configured as pulse width modulator (PWM) channel output PWM2 or the receive pin RXD1 of the serial communication interface 1 (SCI1).

1.5.6.24 PP1 / PWM1 — Port P I/O Pin 1

PP1 is a general-purpose input or output pin. It can be configured as pulse width modulator (PWM) channel output PWM1.

1.5.6.25 PP0 / PWM0 — Port P I/O Pin 0

PP0 is a general-purpose input or output pin. It can be configured as pulse width modulator (PWM) channel output PWM0 or the transmit pin TXD1 of the serial communication interface 1 (SCI1).

1.5.6.26 PS7 / $\overline{SS}$ — Port S I/O Pin 7

PS7 is a general-purpose input or output pin. It can be configured as slave select pin $\overline{SS}$ of the serial peripheral interface (SPI).

1.5.6.27 PS6 / SCK — Port S I/O Pin 6

PS6 is a general-purpose input or output pin. It can be configured as serial clock pin SCK of the serial peripheral interface (SPI).

2.3.1 Module Memory Map

The Flash memory map is shown in Figure 2-2. The HCS12 architecture places the Flash memory addresses between 0x4000 and 0xFFFF which corresponds to three 16-Kbyte pages. The content of the HCS12 core PPAGE register is used to map the logical middle page ranging from address 0x8000 to 0xBFFF to any physical 16 Kbyte page in the Flash memory. By placing 0x3E or 0x3F in the HCS12 Core PPAGE register, the associated 16 Kbyte pages appear twice in the MCU memory map.

The FPROT register, described in Section 2.3.2.5, “Flash Protection Register (FPROT)”, can be set to globally protect a Flash block. However, three separate memory regions, one growing upward from the first address in the next-to-last page in the Flash block (called the lower region), one growing downward from the last address in the last page in the Flash block (called the higher region), and the remaining addresses in the Flash block, can be activated for protection. The Flash locations of these protectable regions are shown in Table 2-2. The higher address region of Flash block 0 is mainly targeted to hold the boot loader code because it covers the vector space. The lower address region of any Flash block can be used for EEPROM emulation in an MCU without an EEPROM module because it can remain unprotected while the remaining addresses are protected from program or erase.

Security information that allows the MCU to restrict access to the Flash module is stored in the Flash configuration field found in Flash block 0, described in Table 2-1.

Table 2-1. Flash Configuration Field

Unpaged Flash Address	Paged Flash Address (PPAGE 0x3F)	Size (Bytes)	Description
0xFF00 – 0xFF07	0xBF00 – 0xBF07	8	Backdoor Comparison Key Refer to Section 2.6.1, “Unsecuring the MCU using Backdoor Key Access”
0xFF08 – 0xFF0B	0xBF08 – 0xBF0B	4	Reserved
0xFF0C	0xBF0C	1	Block 1 Flash Protection Byte Refer to Section 2.3.2.7, “Flash Status Register (FSTAT)”
0xFF0D	0xBF0D	1	Block 0 Flash Protection Byte Refer toSection 2.3.2.7, “Flash Status Register (FSTAT)”
0xFF0E	0xBF0E	1	Flash Nonvolatile Byte Refer to Section 2.3.2.9, “Flash Control Register (FCTL)”
0xFF0F	0xBF0F	1	Flash Security Byte Refer to Section 2.3.2.2, “Flash Security Register (FSEC)”

2.4.1.3.5 Mass Erase Command

The mass erase command is used to erase a Flash memory block using an embedded algorithm. If the Flash block to be erased contains any protected area, the PVIOL flag in the FSTAT register will set and the mass erase command will not launch. After the mass erase command has successfully launched, the CCIF flag in the FSTAT register will set after the mass erase operation has completed unless a second command has been buffered.

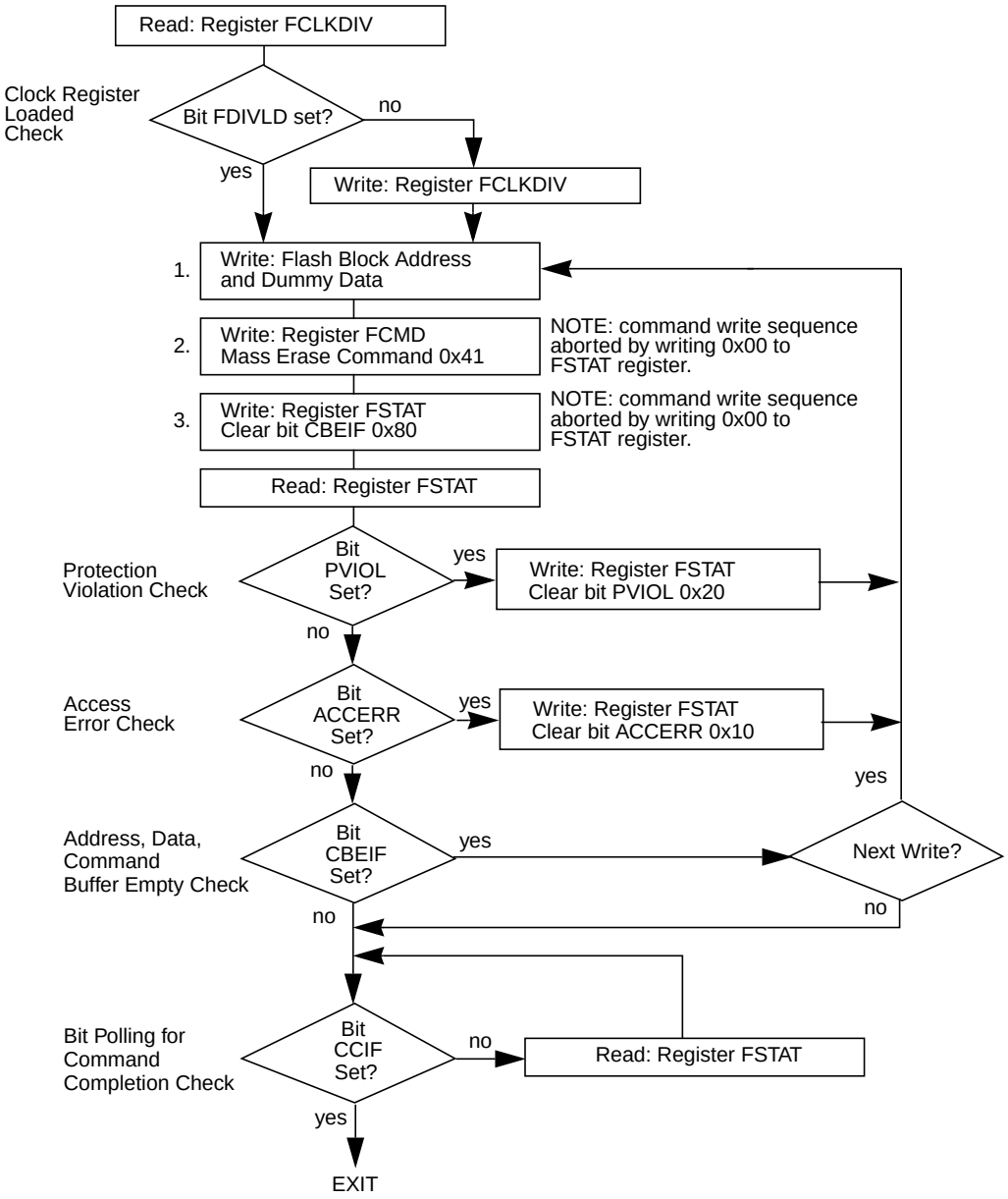


Figure 2-27. Example Mass Erase Command Flow

The PLL filter can be manually or automatically configured into one of two possible operating modes:

- Acquisition mode

  In acquisition mode, the filter can make large frequency corrections to the VCO. This mode is used at PLL start-up or when the PLL has suffered a severe noise hit and the VCO frequency is far off the desired frequency. When in acquisition mode, the TRACK status bit is cleared in the CRGFLG register.
- Tracking mode

  In tracking mode, the filter makes only small corrections to the frequency of the VCO. PLL jitter is much lower in tracking mode, but the response to noise is also slower. The PLL enters tracking mode when the VCO frequency is nearly correct and the TRACK bit is set in the CRGFLG register.

The PLL can change the bandwidth or operational mode of the loop filter manually or automatically.

In automatic bandwidth control mode (AUTO = 1), the lock detector automatically switches between acquisition and tracking modes. Automatic bandwidth control mode also is used to determine when the PLL clock (PLLCLK) is safe to use as the source for the system and core clocks. If PLL LOCK interrupt requests are enabled, the software can wait for an interrupt request and then check the LOCK bit. If CPU interrupts are disabled, software can poll the LOCK bit continuously (during PLL start-up, usually) or at periodic intervals. In either case, only when the LOCK bit is set, is the PLLCLK clock safe to use as the source for the system and core clocks. If the PLL is selected as the source for the system and core clocks and the LOCK bit is clear, the PLL has suffered a severe noise hit and the software must take appropriate action, depending on the application.

The following conditions apply when the PLL is in automatic bandwidth control mode (AUTO = 1):

- The TRACK bit is a read-only indicator of the mode of the filter.
- The TRACK bit is set when the VCO frequency is within a certain tolerance, Δ_{trk}, and is clear when the VCO frequency is out of a certain tolerance, Δ_{unt}.
- The LOCK bit is a read-only indicator of the locked state of the PLL.
- The LOCK bit is set when the VCO frequency is within a certain tolerance, Δ_{Lock}, and is cleared when the VCO frequency is out of a certain tolerance, Δ_{unl}.
- CPU interrupts can occur if enabled (LOCKIE = 1) when the lock condition changes, toggling the LOCK bit.

The PLL can also operate in manual mode (AUTO = 0). Manual mode is used by systems that do not require an indicator of the lock condition for proper operation. Such systems typically operate well below the maximum system frequency (f_{sys}) and require fast start-up. The following conditions apply when in manual mode:

- ACQ is a writable control bit that controls the mode of the filter. Before turning on the PLL in manual mode, the ACQ bit should be asserted to configure the filter in acquisition mode.
- After turning on the PLL by setting the PLLON bit software must wait a given time (t_{acq}) before entering tracking mode (ACQ = 0).
- After entering tracking mode software must wait a given time (t_{al}) before selecting the PLLCLK as the source for system and core clocks (PLLSEL = 1).

7.4.1.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 16 external analog input channels to the sample and hold machine.

7.4.1.3 Sample Buffer Amplifier

The sample amplifier is used to buffer the input analog signal so that the storage node can be quickly charged to the sample potential.

7.4.1.4 Analog-to-Digital (A/D) Machine

The A/D machine performs analog to digital conversions. The resolution is program selectable at either 8 or 10 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the stored analog sample potential with a series of digitally generated analog potentials. By following a binary search algorithm, the A/D machine locates the approximating potential that is nearest to the sampled potential.

When not converting the A/D machine disables its own clocks. The analog electronics continue drawing quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

Only analog input signals within the potential range of V_{RL} to V_{RH} (A/D reference potentials) will result in a non-railed digital output codes.

7.4.2 Digital Sub-Block

This subsection explains some of the digital features in more detail. See register descriptions for all details.

7.4.2.1 External Trigger Input

The external trigger feature allows the user to synchronize ATD conversions to the external environment events rather than relying on software to signal the ATD module when ATD conversions are to take place. The external trigger signal (out of reset ATD channel 15, configurable in ATDCTL1) is programmable to be edge or level sensitive with polarity control. Table 7-27 gives a brief description of the different combinations of control bits and their effect on the external trigger function.

Table 7-27. External Trigger Control Bits

ETRIGLE	ETRIGP	ETRIGE	SCAN	Description
X	X	0	0	Ignores external trigger. Performs one conversion sequence and stops.
X	X	0	1	Ignores external trigger. Performs continuous conversion sequences.
0	0	1	X	Falling edge triggered. Performs one conversion sequence per trigger.
0	1	1	X	Rising edge triggered. Performs one conversion sequence per trigger.
1	0	1	X	Trigger active low. Performs continuous conversions while trigger is active.
1	1	1	X	Trigger active high. Performs continuous conversions while trigger is active.

During a conversion, if additional active edges are detected the overrun error flag ETORF is set.

Module Base + 0x001C (CANIDMR4)
0x001D (CANIDMR5)
0x001E (CANIDMR6)
0x001F (CANIDMR7)

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

Figure 12-20. MSCAN Identifier Mask Registers (Second Bank) — CANIDMR4–CANIDMR7

Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 12-24. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7:0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

indicating that the received byte can be read. If the receive interrupt enable bit, RIE, in SCI control register 2 (SCICR2) is also set, the RDRF flag generates an RDRF interrupt request.

13.4.5.3 Data Sampling

The receiver samples the RXD pin at the RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock (see Figure 13-15) is re-synchronized:

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s. When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

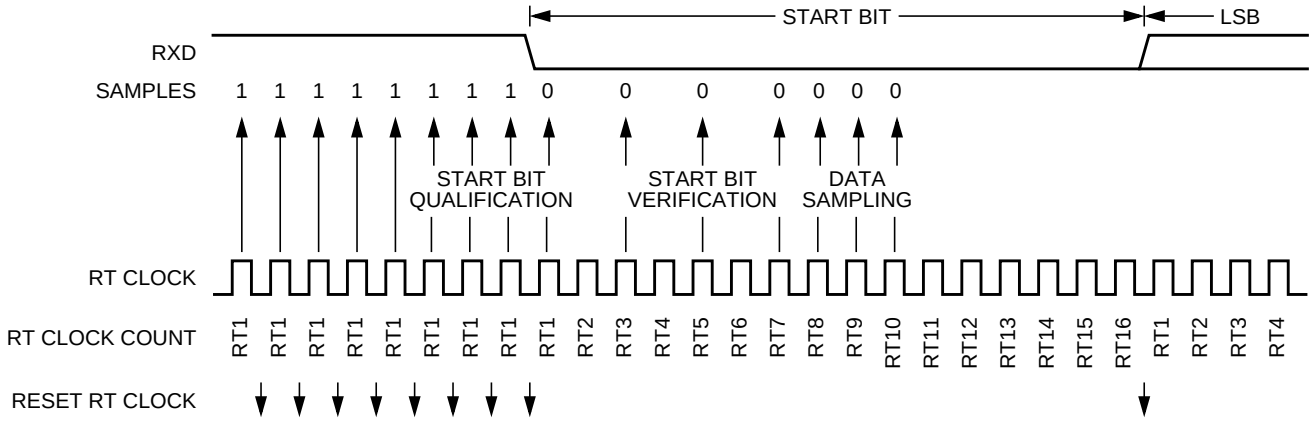


Figure 13-15. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. Table 13-14 summarizes the results of the start bit verification samples.

Table 13-14. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

The baud rate generator is activated only when the SPI is in the master mode and a serial transfer is taking place. In the other cases, the divider is disabled to decrease I_{DD} current.

$$BaudRateDivisor = (SPPR + 1) \bullet 2^{(SPR + 1)}$$

Figure 14-11. Baud Rate Divisor Equation

14.4.5 Special Features

14.4.5.1 $\overline{SS}$ Output

The $\overline{SS}$ output feature automatically drives the $\overline{SS}$ pin low during transmission to select external devices and drives it high during idle to deselect external devices. When $\overline{SS}$ output is selected, the $\overline{SS}$ output pin is connected to the $\overline{SS}$ input pin of the external device.

The $\overline{SS}$ output is available only in master mode during normal SPI operation by asserting SSOE and MODFEN bit as shown in Table 14-3.

The mode fault feature is disabled while $\overline{SS}$ output is enabled.

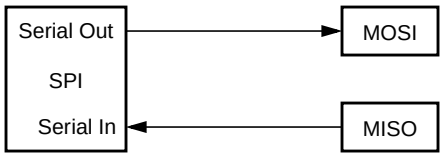
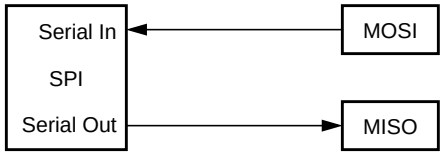
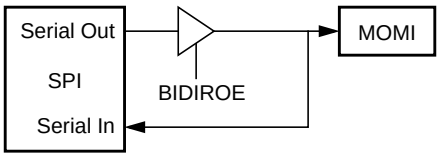
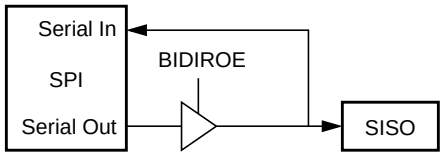
NOTE

Care must be taken when using the $\overline{SS}$ output feature in a multimaster system because the mode fault feature is not available for detecting system errors between masters.

14.4.5.2 Bidirectional Mode (MOSI or MISO)

The bidirectional mode is selected when the SPC0 bit is set in SPI Control Register 2 (see Table 14-9). In this mode, the SPI uses only one serial data pin for the interface with external device(s). The MSTR bit decides which pin to use. The MOSI pin becomes the serial data I/O (MOMI) pin for the master mode, and the MISO pin becomes serial data I/O (SISO) pin for the slave mode. The MISO pin in master mode and MOSI pin in slave mode are not used by the SPI.

Table 14-9. Normal Mode and Bidirectional Mode

When SPE = 1	Master Mode MSTR = 1	Slave Mode MSTR = 0
Normal Mode SPC0 = 0		
Bidirectional Mode SPC0 = 1		

15.3.2.1 PWM Enable Register (PWME)

Each PWM channel has an enable bit (PWMEx) to start its waveform output. When any of the PWMEx bits are set (PWMEx = 1), the associated PWM output is enabled immediately. However, the actual PWM waveform is not available on the associated PWM output until its clock source begins its next cycle due to the synchronization of PWMEx and the clock source.

NOTE

The first PWM cycle after enabling the channel can be irregular.

An exception to this is when channels are concatenated. After concatenated mode is enabled (CONxx bits set in PWMCTL register), enabling/disabling the corresponding 16-bit PWM channel is controlled by the low-order PWMEx bit. In this case, the high-order bytes PWMEx bits have no effect and their corresponding PWM output lines are disabled.

While in run mode, if all six PWM channels are disabled (PWME5–PWME0 = 0), the prescaler counter shuts off for power savings.

	7	6	5	4	3	2	1	0
R	0	0	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-3. PWM Enable Register (PWME)

Read: anytime

Write: anytime

Table 15-2. PWME Field Descriptions

Field	Description
5 PWME5	**Pulse Width Channel 5 Enable** 0 Pulse width channel 5 is disabled. 1 Pulse width channel 5 is enabled. The pulse modulated signal becomes available at PWM,output bit 5 when its clock source begins its next cycle.
4 PWME4	**Pulse Width Channel 4 Enable** 0 Pulse width channel 4 is disabled. 1 Pulse width channel 4 is enabled. The pulse modulated signal becomes available at PWM, output bit 4 when its clock source begins its next cycle. If CON45 = 1, then bit has no effect and PWM output line 4 is disabled.
3 PWME3	**Pulse Width Channel 3 Enable** 0 Pulse width channel 3 is disabled. 1 Pulse width channel 3 is enabled. The pulse modulated signal becomes available at PWM, output bit 3 when its clock source begins its next cycle.
2 PWME2	**Pulse Width Channel 2 Enable** 0 Pulse width channel 2 is disabled. 1 Pulse width channel 2 is enabled. The pulse modulated signal becomes available at PWM, output bit 2 when its clock source begins its next cycle. If CON23 = 1, then bit has no effect and PWM output line 2 is disabled.

15.4.2.1 PWM Enable

Each PWM channel has an enable bit (PWMEx) to start its waveform output. When any of the PWMEx bits are set (PWMEx = 1), the associated PWM output signal is enabled immediately. However, the actual PWM waveform is not available on the associated PWM output until its clock source begins its next cycle due to the synchronization of PWMEx and the clock source. An exception to this is when channels are concatenated. Refer to Section 15.4.2.7, “PWM 16-Bit Functions,” for more detail.

NOTE

The first PWM cycle after enabling the channel can be irregular.

On the front end of the PWM timer, the clock is enabled to the PWM circuit by the PWMEx bit being high. There is an edge-synchronizing circuit to guarantee that the clock will only be enabled or disabled at an edge. When the channel is disabled (PWMEx = 0), the counter for the channel does not count.

15.4.2.2 PWM Polarity

Each channel has a polarity bit to allow starting a waveform cycle with a high or low signal. This is shown on the block diagram as a mux select of either the Q output or the $\overline{Q}$ output of the PWM output flip-flop. When one of the bits in the PWMPOL register is set, the associated PWM channel output is high at the beginning of the waveform, then goes low when the duty count is reached. Conversely, if the polarity bit is 0, the output starts low and then goes high when the duty count is reached.

15.4.2.3 PWM Period and Duty

Dedicated period and duty registers exist for each channel and are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to 0x0000)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period and duty registers will go directly to the latches as well as the buffer.

A change in duty or period can be forced into effect “immediately” by writing the new value to the duty and/or period registers and then writing to the counter. This forces the counter to reset and the new duty and/or period values to be latched. In addition, because the counter is readable it is possible to know where the count is with respect to the duty value and software can be used to make adjustments.

NOTE

When forcing a new period or duty into effect immediately, an irregular PWM cycle can occur.

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time.

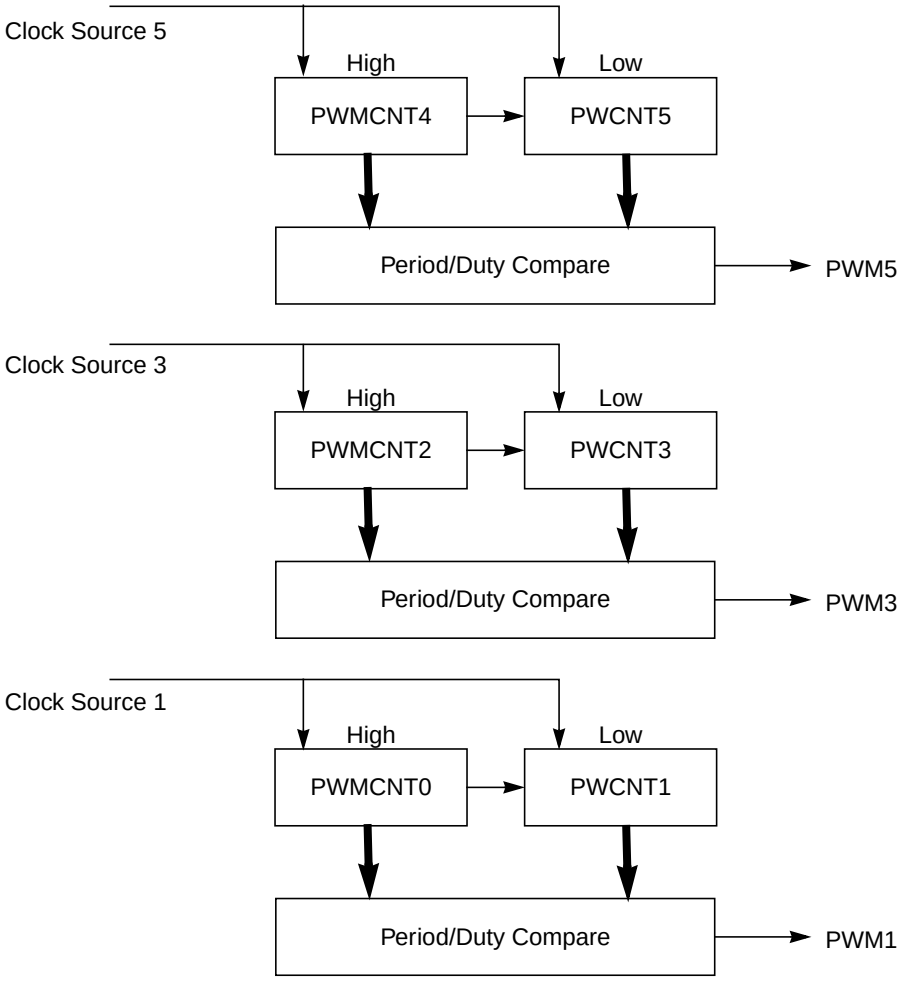


Figure 15-40. PWM 16-Bit Mode

When using the 16-bit concatenated mode, the clock source is determined by the low-order 8-bit channel clock select control bits. That is channel 5 when channels 4 and 5 are concatenated, channel 3 when channels 2 and 3 are concatenated, and channel 1 when channels 0 and 1 are concatenated. The resulting PWM is output to the pins of the corresponding low-order 8-bit channel as also shown in Figure 15-40. The polarity of the resulting PWM output is controlled by the PPOLx bit of the corresponding low-order 8-bit channel as well.

After concatenated mode is enabled (CONxx bits set in PWMCTL register), enabling/disabling the corresponding 16-bit PWM channel is controlled by the low-order PWMEx bit. In this case, the high-order bytes PWMEx bits have no effect and their corresponding PWM output is disabled.

In concatenated mode, writes to the 16-bit counter by using a 16-bit access or writes to either the low or high-order byte of the counter will reset the 16-bit counter. Reads of the 16-bit counter must be made by 16-bit access to maintain data coherency.

Either left aligned or center aligned output mode can be used in concatenated mode and is controlled by the low-order CAEx bit. The high-order CAEx bit has no effect.

Chapter 17
Dual Output Voltage Regulator (VREG3V3V2)

17.1 Introduction

The VREG3V3 is a dual output voltage regulator providing two separate 2.5 V (typical) supplies differing in the amount of current that can be sourced. The regulator input voltage range is from 3.3 V up to 5 V (typical).

17.1.1 Features

The block VREG3V3 includes these distinctive features:

- Two parallel, linear voltage regulators
  - — Bandgap reference
- Low-voltage detect (LVD) with low-voltage interrupt (LVI)
- Power-on reset (POR)
- Low-voltage reset (LVR)

17.1.2 Modes of Operation

There are three modes VREG3V3 can operate in:

- Full-performance mode (FPM) (MCU is not in stop mode)

  The regulator is active, providing the nominal supply voltage of 2.5 V with full current sourcing capability at both outputs. Features LVD (low-voltage detect), LVR (low-voltage reset), and POR (power-on reset) are available.
- Reduced-power mode (RPM) (MCU is in stop mode)

  The purpose is to reduce power consumption of the device. The output voltage may degrade to a lower value than in full-performance mode, additionally the current sourcing capability is substantially reduced. Only the POR is available in this mode, LVD and LVR are disabled.
- Shutdown mode

  Controlled by V_{REGEN} (see device overview chapter for connectivity of V_{REGEN}).

  This mode is characterized by minimum power consumption. The regulator outputs are in a high impedance state, only the POR feature is available, LVD and LVR are disabled.

  This mode must be used to disable the chip internal regulator VREG3V3, i.e., to bypass the VREG3V3 to use external supplies.

The regulator is a linear series regulator with a bandgap reference in its Full Performance Mode and a voltage clamp in Reduced Power Mode. All load currents flow from input V_{DDR} to V_{SS} or V_{SSPLL}, the reference circuits are connected to V_{DDA} and V_{SSA}.

17.4.2 Full-Performance Mode

In Full Performance Mode, a fraction of the output voltage (V_{DD}) and the bandgap reference voltage are fed to an operational amplifier. The amplified input voltage difference controls the gate of an output driver which basically is a large NMOS transistor connected to the output.

17.4.3 Reduced-Power Mode

In Reduced Power Mode, the driver gate is connected to a buffered fraction of the input voltage (V_{DDR}). The operational amplifier and the bandgap are disabled to reduce power consumption.

17.4.4 LVD — Low-Voltage Detect

sub-block LVD is responsible for generating the low-voltage interrupt (LVI). LVD monitors the input voltage (V_{DDA}–V_{SSA}) and continuously updates the status flag LVDS. Interrupt flag LVIF is set whenever status flag LVDS changes its value. The LVD is available in FPM and is inactive in Reduced Power Mode and Shutdown Mode.

17.4.5 POR — Power-On Reset

This functional block monitors output V_{DD}. If V_{DD} is below V_{PORD}, signal POR is high, if it exceeds V_{PORD}, the signal goes low. The transition to low forces the CPU in the power-on sequence.

Due to its role during chip power-up this module must be active in all operating modes of VREG3V3.

17.4.6 LVR — Low-Voltage Reset

Block LVR monitors the primary output voltage V_{DD}. If it drops below the assertion level (V_{LVRA}) signal LVR asserts and when rising above the deassertion level (V_{LVRD}) signal LVR negates again. The LVR function is available only in Full Performance Mode.

17.4.7 CTRL — Regulator Control

This part contains the register block of VREG3V3 and further digital functionality needed to control the operating modes. CTRL also represents the interface to the digital core logic.

21.3.2.9 Mode Register (MODE)

	7	6	5	4	3	2	1	0
R	MODC	MODB	MODA	0	IVIS	0	EMK	EME
W								
Reset								
Special Single Chip	0	0	0	0	0	0	0	0
Emulation Expanded Narrow	0	0	1	0	1	0	1	1
Special Test	0	1	0	0	1	0	0	0
Emulation Expanded Wide	0	1	1	0	1	0	1	1
Normal Single Chip	1	0	0	0	0	0	0	0
Normal Expanded Narrow	1	0	1	0	0	0	0	0
Peripheral	1	1	0	0	0	0	0	0
Normal Expanded Wide	1	1	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 21-13. Mode Register (MODE)

Read: Anytime (provided this register is in the map).

Write: Each bit has specific write conditions. Please refer to the descriptions of each bit on the following pages.

The MODE register is used to establish the operating mode and other miscellaneous functions (i.e., internal visibility and emulation of port E and K).

In special peripheral mode, this register is not accessible but it is reset as shown to system configuration features. Changes to bits in the MODE register are delayed one cycle after the write.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally.

2 PC Board according to EIA/JEDEC Standard 51-2
3 PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

Table A-6. 5V I/O Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	0.65*V_{DD5}	–	V_{DD5} + 0.3	V
2	P	Input Low Voltage	V_{IL}	V_{SS5} – 0.3	–	0.35*V_{DD5}	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current except PU, PV (pins in high impedance input mode)[1] V_{in} = V_{DD5} or V_{SS5}	I_{in}	–1.0	–	1.0	µA
5	P	Input Leakage Current PU, PV (pins in high impedance input mode)[2] V_{in} = V_{DD5} or V_{SS5}	I_{in}	–2.5	–	2.5	µA
6	P	Output High Voltage (pins in output mode, except PU and PV) Partial Drive I_{OH} = –1.0mA Full Drive I_{OH} = –10mA	V_{OH}	V_{DD5} – 0.8	–	–	V
7	P	Output Low Voltage (pins in output mode except PU and PV) Partial Drive I_{OL} = +1.0mA Full Drive I_{OL} = +10mA	V_{OL}	–	–	0.8	V
8	P	Output High Voltage (pins PU and PV in output mode) I_{OH} = –20mA (typical value at 25°C)	V_{OH}	V_{DD5} – 0.32	V_{DD5} – 0.2	–	V
9	P	Output Low Voltage (pins PU and PV in output mode) I_{OL} = +20mA (typical value at 25°C)	V_{OL}	–	.2	0.32	V
10	C	Output Rise Time (pins PU and PV in output mode with slew control enabled) V_{DD5}=5V, R_{load}=1KΩ, 10% to 90% of V_{OH}	t_r	60	100	130	ns
11	C	Output Fall Time (pins PU and PV in output mode with slew control enabled) V_{DD5}=5V, R_{load}=1KΩ, 10% to 90% of V_{OH}	t_f	60	100	130	ns
12	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	–	–	–130	µA
13	P	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	–10	–	–	µA
14	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	–	–	130	µA

The setup time can be ignored for this operation.

A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table A-11. NVM Timing Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5		50 [1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1			MHz
3	D	Operating Frequency	f_{NVMOP}	150		200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 [2]		74.5 [3]	µs
5	D	Flash Burst Programming consecutive word [4]	t_{bwpgm}	20.4 [2]		31 [3]	µs
6	D	Flash Burst Programming Time for 32 Words [4]	t_{brpgm}	678.4 [2]		1035.5 [3]	µs
7	P	Sector Erase Time	t_{era}	20 [5]		26.7 [3]	ms
8	P	Mass Erase Time	t_{mass}	100 [5]		133 [3]	ms
9	D	Blank Check Time Flash per block	t_{check}	11 [6]		32778 [7]	t_{cyc}
10	D	Blank Check Time EEPROM per block	t_{check}	11 [6]		2058[7]	t_{cyc}

1 Restrictions for oscillator in crystal mode apply!

2 Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.

3 Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formulae in Sections Section A.3.1.1, “Single Word Programming,” through Section A.3.1.4, “Mass Erase,” for guidance.

4 urst Programming operations are not applicable to EEPROM

5 Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}

6 Minimum time, if first word in the array is not blank

7 Maximum time to complete check on an erased block

A.5.1.3 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

A.5.1.4 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

A.5.1.5 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{wrs} the CPU starts fetching the interrupt vector.

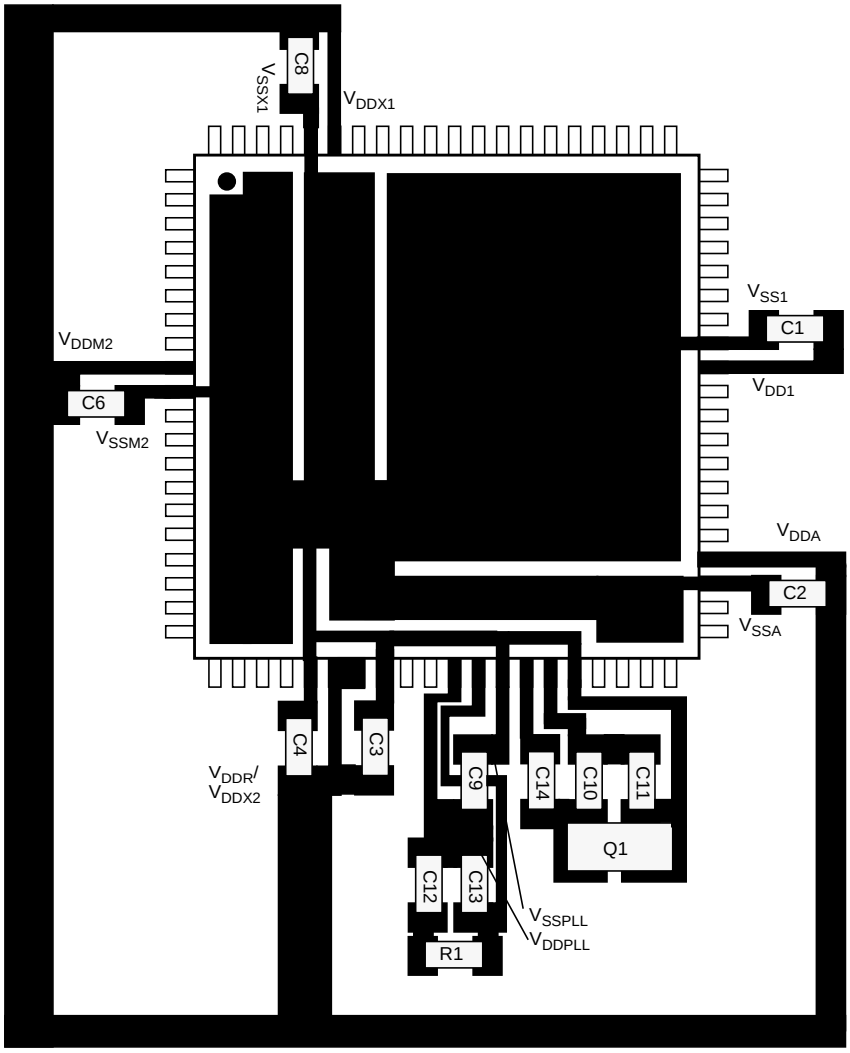


Figure B-2. Recommended PCB Layout for 80-pin QFP

0x00D0–0x00D7 SCI1 (Asynchronous Serial Interface) (continued)

Address	Name		7	6	5	4	3	2	1	0
0x00D5	SCI1SR2	R	0	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		W								
0x00D6	SCI1DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x00D7	SCI1DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

0x00D8–0x00DF SPI (Serial Peripheral Interface)

Address	Name		7	6	5	4	3	2	1	0
0x00D8	SPICR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		W								
0x00D9	SPICR2	R	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		W								
0x00DA	SPIBR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		W								
0x00DB	SPISR	R	SPIF	0	SPTEF	MODF	0	0	0	0
		W								
0x00DC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00DD	SPIDR	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x00DE–0x00DF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x00E0–0x00FF PWM (Pulse Width Modulator 8 Bit 6 Channel) (Sheet 1 of 2)

Address	Name		7	6	5	4	3	2	1	0
0x00E0	PWME	R	0	0	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		W								
0x00E1	PWMPOL	R	0	0	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		W								
0x00E2	PWMCLK	R	0	0	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		W								
0x00E3	PWMPRCLK	R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		W								
0x00E4	PWMCAE	R	0	0	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		W								
0x00E5	PWMCTL	R	0	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		W								
0x00E6	PWMTST Test Only	R	0	0	0	0	0	0	0	0
		W								
0x00E7	PWMPRSC Test Only	R	0	0	0	0	0	0	0	0
		W								
0x00E8	PWMSCLA	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								