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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	LCD, Motor control PWM, POR, PWM, WDT
Number of I/O	91
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s12hz128j3val

- Memory
  - 256K, 128K, 64K, 32K Flash EEPROM or ROM
  - 2K, 1K byte EEPROM
  - 12K, 6K, 4K, 2K byte RAM
- CRG (low current oscillator, PLL, reset, clocks, COP watchdog, real time interrupt, clock monitor)
- Analog-to-digital converter
  - 16 channels, 10-bit resolution
  - External conversion trigger capability
- Two 1-Mbps, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Timer
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels
  - Two 8-bit or one 16-bit pulse accumulators
- 6 PWM channels
  - Programmable period and duty cycle
  - 8-bit 6-channel or 16-bit 3-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
- Serial interfaces
  - Two asynchronous serial communications interfaces (SCI)
  - Synchronous serial peripheral interface (SPI)
  - Inter-integrated circuit interface (IIC)
- Liquid crystal display (LCD) driver with variable input voltage
  - Configurable for up to 32 frontplanes and 4 backplanes or general-purpose input or output
  - 5 modes of operation allow for different display sizes to meet application requirements
  - Unused frontplane and backplane pins can be used as general-purpose I/O
- PWM motor controller (MC) with 16 high current drivers
  - Each PWM channel switchable between two drivers in an H-bridge configuration
  - Left, right and center aligned outputs
  - Support for sine and cosine drive
  - Dithering
  - Output slew rate control

Chapter 2
256 Kbyte Flash Module (FTS256K2V1)

2.1 Introduction

This document describes the FTS256K2 module that includes a 256 Kbyte Flash (nonvolatile) memory. The Flash memory may be read as either bytes, aligned words, or misaligned words. Read access time is one bus cycle for bytes and aligned words, and two bus cycles for misaligned words.

The Flash memory is ideal for program and data storage for single-supply applications allowing for field reprogramming without requiring external voltage sources for program or erase. Program and erase functions are controlled by a command driven interface. The Flash module supports both block erase and sector erase. An erased bit reads 1 and a programmed bit reads 0. The high voltage required to program and erase the Flash memory is generated internally. It is not possible to read from a Flash block while it is being erased or programmed.

A Flash word must be in the erased state before being programmed.
Cumulative programming of bits within a Flash word is not allowed.

2.1.1 Glossary

Banked Register — A memory-mapped register operating on one Flash block which shares the same register address as the equivalent registers for the other Flash blocks. The active register bank is selected by the BKSEL bit in the FCNFG register.

Command Write Sequence — A three-step MCU instruction sequence to execute built-in algorithms (including program and erase) on the Flash memory.

Common Register — A memory-mapped register which operates on all Flash blocks.

2.1.2 Features

- 256 Kbytes of Flash memory comprised of two 128 Kbyte blocks with each block divided into 128 sectors of 1024 bytes
- Automated program and erase algorithm
- Interrupts on Flash command completion, command buffer empty
- Fast sector erase and word program operation
- 2-stage command pipeline for faster multi-word program times
- Sector erase abort feature for critical interrupt response
- Flexible protection scheme to prevent accidental program or erase

3.4.1.3 Valid EEPROM Commands

Table 3-10 summarizes the valid EEPROM commands. Also shown are the effects of the commands on the EEPROM array.

Table 3-10. Valid EEPROM Commands

ECMD	Meaning	Function on EEPROM Array
0x05	Erase Verify	Verify all memory bytes of the EEPROM array are erased. If the array is erased, the BLANK bit will set in the ESTAT register upon command completion.
0x20	Program	Program a word (two bytes).
0x40	Sector Erase	Erase two words (four bytes) of EEPROM array.
0x41	Mass Erase	Erase all of the EEPROM array. A mass erase of the full array is only possible when EPDIS and EPOPEN are set.
0x60	Sector Modify	Erase two words of EEPROM, re-program one word.

An EEPROM word must be in an erased state before being programmed.
Cumulative programming of bits within a word is not allowed.

The sector modify command (0x60) is a two-step command which first erases a sector (2 words) of the EEPROM array and then re-programs one of the words in that sector. The EEPROM sector which is erased by the sector modify command is the sector containing the address of the aligned array write which starts the valid command sequence. That same address is re-programmed with the data which is written. By launching a sector modify command and then pipelining a program command it is possible to completely replace the contents of an EEPROM sector.

3.4.1.4 Illegal EEPROM Operations

The ACCERR flag will be set during the command write sequence if any of the following illegal operations are performed causing the command write sequence to immediately abort:

1. Writing to the EEPROM address space before initializing ECLKDIV.
2. Writing a misaligned word or a byte to the valid EEPROM address space.
3. Writing to the EEPROM address space while CBEIF is not set.
4. Writing a second word to the EEPROM address space before executing a program or erase command on the previously written word.
5. Writing to any EEPROM register other than ECMD after writing a word to the EEPROM address space.
6. Writing a second command to the ECMD register before executing the previously written command.
7. Writing an invalid command to the ECMD register in normal mode.
8. Writing to any EEPROM register other than ESTAT (to clear CBEIF) after writing to the command register (ECMD).

4.3 Memory Map and Register Definition

This section provides a detailed description of all registers. Table 4-2 is a standard memory map of port integration module.

Table 4-2. PIM9HZ256 Memory Map

Address Offset	Use	Access
0x0000	Port T I/O Register (PTT)	R/W
0x0001	Port T Input Register (PTIT)	R
0x0002	Port T Data Direction Register (DDRT)	R/W
0x0003	Port T Reduced Drive Register (RDRT)	R/W
0x0004	Port T Pull Device Enable Register (PERT)	R/W
0x0005	Port T Polarity Select Register (PPST)	R/W
0x0006 - 0x0007	Reserved	—
0x0008	Port S I/O Register (PTS)	R/W
0x0009	Port S Input Register (PTIS)	R
0x000A	Port S Data Direction Register (DDRS)	R/W
0x000B	Port S Reduced Drive Register (RDRS)	R/W
0x000C	Port S Pull Device Enable Register (PERS)	R/W
0x000D	Port S Polarity Select Register (PPSS)	R/W
0x000E	Port S Wired-OR Mode Register (WOMS)	R/W
0x000F	Reserved	—
0x0010	Port M I/O Register (PTM)	R/W
0x0011	Port M Input Register (PTIM)	R
0x0012	Port M Data Direction Register (DDRM)	R/W
0x0013	Port M Reduced Drive Register (RDRM)	R/W
0x0014	Port M Pull Device Enable Register (PERM)	R/W
0x0015	Port M Polarity Select Register (PPSM)	R/W
0x0016	Port M Wired-OR Mode Register (WOMM)	R/W
0x0017	Reserved	—
0x0018	Port P I/O Register (PTP)	R/W
0x0019	Port P Input Register (PTIP)	R
0x001A	Port P Data Direction Register (DDRP)	R/W
0x001B	Port P Reduced Drive Register (RDRP)	R/W
0x001C	Port P Pull Device Enable Register (PERP)	R/W
0x001D	Port P Polarity Select Register (PPSP)	R/W
0x001E	Port P Wired-OR Mode Register (WOMP)	R/W
0x001F - 0x002F	Reserved	—

Table 5-12. Outcome of Clock Loss in Pseudo-Stop Mode (continued)

CME	SCME	SCMIE	CRG Actions
1	1	1	Clock failure --> – VREG enabled, – PLL enabled, – SCM activated, – Start Clock Quality Check, – SCMIF set. SCMIF generates Self-Clock Mode wakeup interrupt. – Exit Pseudo-Stop Mode in SCM using PLL clock (f_{SCM}) as system clock, – Continue to perform a additional Clock Quality Checks until OSCCLK is o.k. again.

5.4.10.2 Wake-up from Full Stop (PSTP=0)

The MCU requires an external interrupt or an external reset in order to wake-up from stop mode.

If the MCU gets an external reset during full stop mode active, the CRG asynchronously restores all configuration bits in the register space to its default settings and will perform a maximum of 50 clock *check_windows* (see Section 5.4.4, “Clock Quality Checker”). After completing the clock quality check the CRG starts the reset generator. After completing the reset sequence processing begins by fetching the normal reset vector. Full stop mode is exited and the MCU is in run mode again.

If the MCU is woken-up by an interrupt, the CRG will also perform a maximum of 50 clock *check_windows* (see Section 5.4.4, “Clock Quality Checker”). If the clock quality check is successful, the CRG will release all system and core clocks and will continue with normal operation. If all clock checks within the timeout-window are failing, the CRG will switch to self-clock mode or generate a clock monitor reset (CMRESET) depending on the setting of the SCME bit.

Because the PLL has been powered-down during stop mode the PLLSEL bit is cleared and the MCU runs on OSCCLK after leaving stop mode. The software must manually set the PLLSEL bit again, in order to switch system and core clocks to the PLLCLK.

NOTE

In full stop mode, the clock monitor is disabled and any loss of clock will not be detected.

5.5 Resets

This section describes how to reset the CRG and how the CRG itself controls the reset of the MCU. It explains all special reset requirements. Because the reset generator for the MCU is part of the CRG, this section also describes all automatic actions that occur during or as a result of individual reset conditions. The reset values of registers and signals are provided in Section 5.3, “Memory Map and Register

Table 7-3. Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple Channel Conversions (MULT = 1) Wrap Around to AN0 after Converting
0	0	0	0	Reserved
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN12
1	1	0	1	AN13
1	1	1	0	AN14
1	1	1	1	AN15

7.3.2.2 ATD Control Register 1 (ATDCTL1)

Writes to this register will abort current conversion sequence but will not start a new sequence.

	7	6	5	4	3	2	1	0
R	ETRIGSEL	0	0	0	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 7-4. ATD Control Register 1 (ATDCTL1)

Read: Anytime

Write: Anytime

Table 7-4. ATDCTL1 Field Descriptions

Field	Description
7 ETRIGSEL	**External Trigger Source Select** — This bit selects the external trigger source to be either one of the AD channels or one of the ETRIG[3:0] inputs. See device specification for availability and connectivity of ETRIG[3:0] inputs. If ETRIG[3:0] input option is not available, writing a 1 to ETRISEL only sets the bit but has no effect, that means one of the AD channels (selected by ETRIGCH[3:0]) remains the source for external trigger. The coding is summarized in Table 7-5.
3:0 ETRIGCH[3:0]	**External Trigger Channel Select** — These bits select one of the AD channels or one of the ETRIG[3:0] inputs as source for the external trigger. The coding is summarized in Table 7-5.

8.4.5.3 1/2 Duty Multiplexed with 1/3 Bias Mode

Duty = 1/2:DUTY1 = 1, DUTY0 = 0

Bias = 1/3:BIAS = 1

V_0 = VSSX, V_1 = VLCD * 1/3, V_2 = VLCD * 2/3, V_3 = VLCD

- BP2 and BP3 are not used, a maximum of 64 segments are displayed.

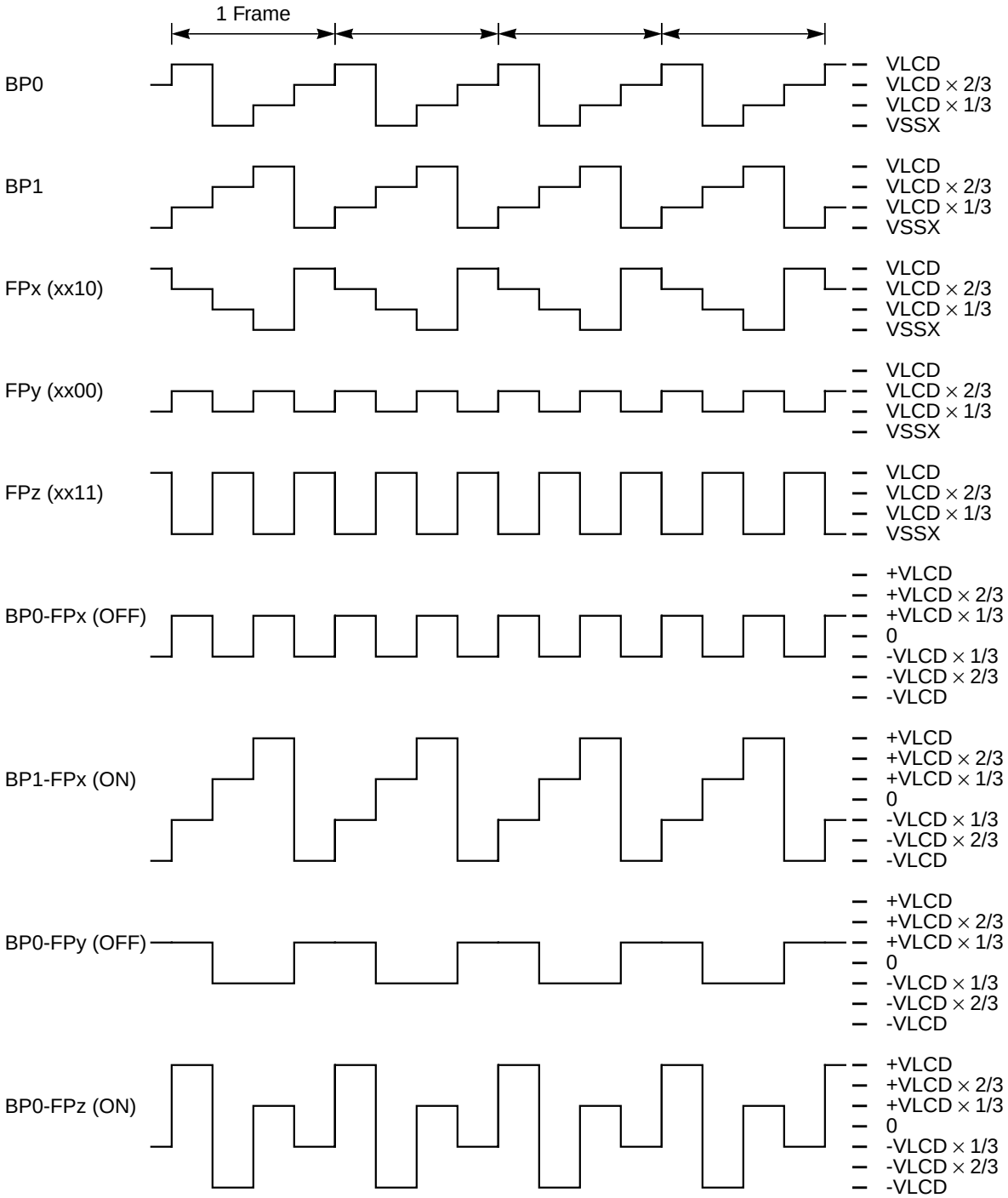

Figure 8-11. 1/2 Duty and 1/3 Bias

11.4 Functional Description

This section provides a complete functional description of the IIC.

11.4.1 I-Bus Protocol

The IIC bus system uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. All devices connected to it must have open drain or open collector outputs. Logic AND function is exercised on both lines with external pull-up resistors. The value of these resistors is system dependent.

Normally, a standard communication is composed of four parts: START signal, slave address transmission, data transfer and STOP signal. They are described briefly in the following sections and illustrated in Figure 11-8.

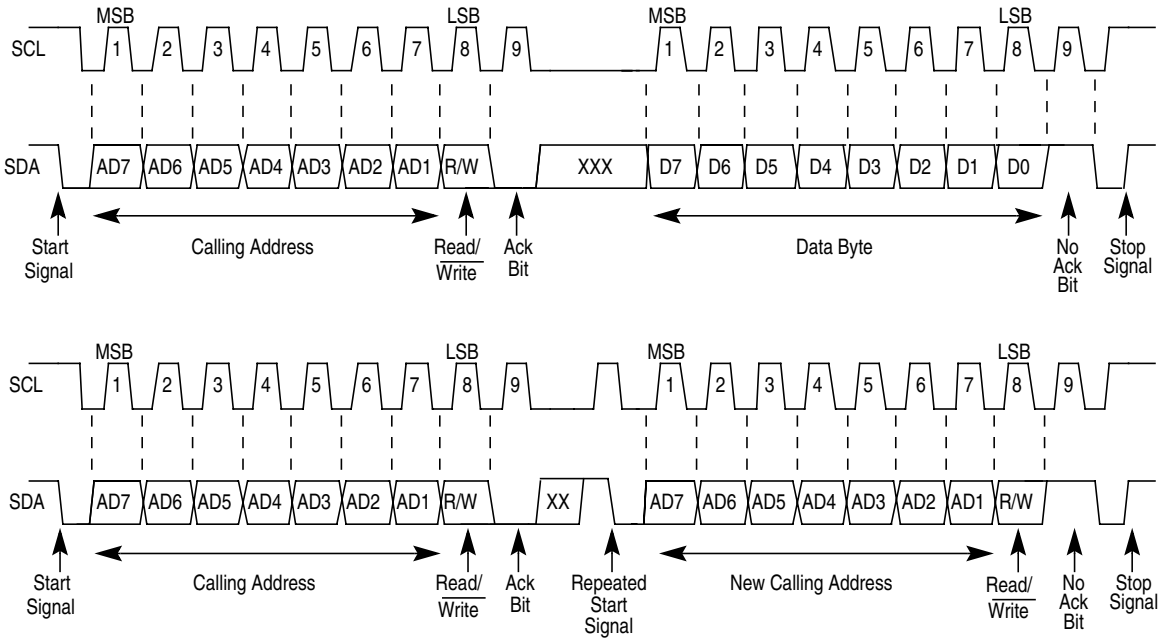

Figure 11-8. IIC-Bus Transmission Signals

11.4.1.1 START Signal

When the bus is free, i.e. no master device is engaging the bus (both SCL and SDA lines are at logical high), a master may initiate communication by sending a START signal.As shown in Figure 11-8, a START signal is defined as a high-to-low transition of SDA while SCL is high. This signal denotes the beginning of a new data transfer (each data transfer may contain several bytes of data) and brings all slaves out of their idle states.

[8] Not including WUPE, INITRQ, and SLPRQ.
[9] TSTAT1 and TSTAT0 are not affected by initialization mode.
[10] RSTAT1 and RSTAT0 are not affected by initialization mode.

12.3.2.2 MSCAN Control Register 1 (CANCTL1)

The CANCTL1 register provides various control bits and handshake status information of the MSCAN module as described below.

Read: Anytime
Write: Anytime when INITRQ = 1 and INITAK = 1, except CANE which is write once in normal and anytime in special system operation modes when the MSCAN is in initialization mode (INITRQ = 1 and INITAK = 1).

Table 12-4. CANCTL1 Register Field Descriptions

Field	Description
7 CANE	**MSCAN Enable** 0 MSCAN module is disabled 1 MSCAN module is enabled
6 CLKSRC	**MSCAN Clock Source** — This bit defines the clock source for the MSCAN module (only for systems with a clock generation module; Section 12.4.3.2, "Clock System," and Section Figure 12-40., "MSCAN Clocking Scheme,"). 0 MSCAN clock source is the oscillator clock 1 MSCAN clock source is the bus clock
5 LOOPB	**Loopback Self Test Mode** — When this bit is set, the MSCAN performs an internal loopback which can be used for self test operation. The bit stream output of the transmitter is fed back to the receiver internally. The RXCAN input pin is ignored and the TXCAN output goes to the recessive state (logic 1). The MSCAN behaves as it does normally when transmitting and treats its own transmitted message as a message received from a remote node. In this state, the MSCAN ignores the bit sent during the ACK slot in the CAN frame acknowledge field to ensure proper reception of its own message. Both transmit and receive interrupts are generated. 0 Loopback self test disabled 1 Loopback self test enabled
4 LISTEN	**Listen Only Mode** — This bit configures the MSCAN as a CAN bus monitor. When LISTEN is set, all valid CAN messages with matching ID are received, but no acknowledgement or error frames are sent out (see Section 12.4.5.4, "Listen-Only Mode"). In addition, the error counters are frozen. Listen only mode supports applications which require "hot plugging" or throughput analysis. The MSCAN is unable to transmit any messages when listen only mode is active. 0 Normal operation 1 Listen only mode activated
2 WUPM	**Wake-Up Mode** — If WUPE in CANCTL0 is enabled, this bit defines whether the integrated low-pass filter is applied to protect the MSCAN from spurious wake-up (see Section 12.4.6.4, "MSCAN Sleep Mode"). 0 MSCAN wakes up the CPU after any recessive to dominant edge on the CAN bus 1 MSCAN wakes up the CPU only in case of a dominant pulse on the CAN bus that has a length of T_{wup}

12.3.2.10 MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)

The CANTAAK register indicates the successful abort of a queued message, if requested by the appropriate bits in the CANTARQ register.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-11. MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)

NOTE

The CANTAAK register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1).

Read: Anytime
Write: Unimplemented for ABTAKx flags

Table 12-16. CANTAAK Register Field Descriptions

Field	Description
2:0 ABTAK[2:0]	**Abort Acknowledge** — This flag acknowledges that a message was aborted due to a pending abort request from the CPU. After a particular message buffer is flagged empty, this flag can be used by the application software to identify whether the message was aborted successfully or was sent anyway. The ABTAKx flag is cleared whenever the corresponding TXE flag is cleared. 0 The message was not aborted. 1 The message was aborted.

15.4.1.3 Clock Select

Each PWM channel has the capability of selecting one of two clocks. For channels 0, 1, 4, and 5 the clock choices are clock A or clock SA. For channels 2 and 3 the choices are clock B or clock SB. The clock selection is done with the PCLKx control bits in the PWMCLK register.

NOTE

Changing clock control bits while channels are operating can cause irregularities in the PWM outputs.

15.4.2 PWM Channel Timers

The main part of the PWM module are the actual timers. Each of the timer channels has a counter, a period register and a duty register (each are 8 bit). The waveform output period is controlled by a match between the period register and the value in the counter. The duty is controlled by a match between the duty register and the counter value and causes the state of the output to change during the period. The starting polarity of the output is also selectable on a per channel basis. Figure 15-35 shows a block diagram for PWM timer.

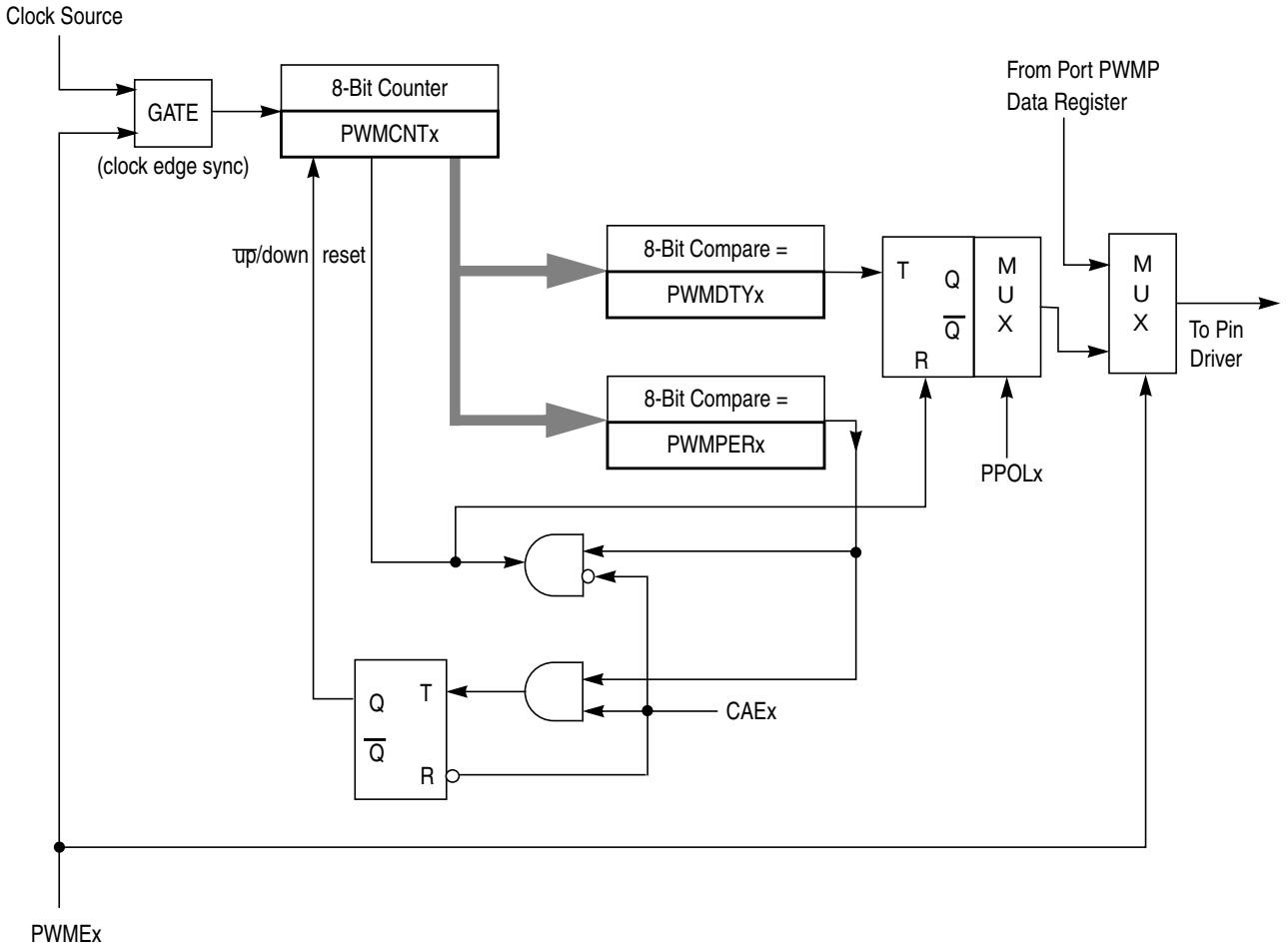

Figure 15-35. PWM Timer Channel Block Diagram

Write: Once in normal and emulation modes, anytime in special modes

NOTE

Writes to this register take one cycle to go into effect.

This register initializes the position of the internal RAM within the on-chip system memory map.

Table 22-2. INITRM Field Descriptions

Field	Description
7:3 RAM[15:11]	**Internal RAM Map Position** — These bits determine the upper five bits of the base address for the system's internal RAM array.
0 RAMHAL	**RAM High-Align** — RAMHAL specifies the alignment of the internal RAM array. 0 Aligns the RAM to the lowest address (0x0000) of the mappable space 1 Aligns the RAM to the higher address (0xFFFF) of the mappable space

22.3.2.3 Initialization of Internal EEPROM Position Register (INITEE)

	7	6	5	4	3	2	1	0
R	EE15	EE14	EE13	EE12	EE11	0	0	EEON
W								
Reset[1]	—	—	—	—	—	—	—	—

1. The reset state of this register is controlled at chip integration. Please refer to the device overview section to determine the actual reset state of this register.

= Unimplemented or Reserved

Figure 22-5. Initialization of Internal EEPROM Position Register (INITEE)

Read: Anytime

Write: The EEON bit can be written to any time on all devices. Bits E[11:15] are “write anytime in all modes” on most devices. On some devices, bits E[11:15] are “write once in normal and emulation modes and write anytime in special modes”. See device overview chapter to determine the actual write access rights.

NOTE

Writes to this register take one cycle to go into effect.

This register initializes the position of the internal EEPROM within the on-chip system memory map.

Table 22-4. INITEE Field Descriptions

Field	Description
7:3 EE[15:11]	**Internal EEPROM Map Position** — These bits determine the upper five bits of the base address for the system’s internal EEPROM array.
0 EEON	**Enable EEPROM** — This bit is used to enable the EEPROM memory in the memory map. 0 Disables the EEPROM from the memory map. 1 Enables the EEPROM in the memory map at the address selected by EE[15:11].

22.3.2.7 Memory Size Register 0 (MEMSIZ0)

	7	6	5	4	3	2	1	0
R	REG_SW0	0	EEP_SW1	EEP_SW0	0	RAM_SW2	RAM_SW1	RAM_SW0
W								
Reset	—	—	—	—	—	—	—	—

= Unimplemented or Reserved

Figure 22-9. Memory Size Register 0 (MEMSIZ0)

Read: Anytime

Write: Writes have no effect

Reset: Defined at chip integration, see device overview section.

The MEMSIZ0 register reflects the state of the register, EEPROM and RAM memory space configuration switches at the core boundary which are configured at system integration. This register allows read visibility to the state of these switches.

Table 22-7. MEMSIZ0 Field Descriptions

Field	Description
7 REG_SW0	**Allocated System Register Space** 0 Allocated system register space size is 1K byte 1 Allocated system register space size is 2K byte
5:4 EEP_SW[1:0]	**Allocated System EEPROM Memory Space** — The allocated system EEPROM memory space size is as given in Table 22-8.
2 RAM_SW[2:0]	**Allocated System RAM Memory Space** — The allocated system RAM memory space size is as given in Table 22-9.

Table 22-8. Allocated EEPROM Memory Space

eep_sw1:eep_sw0	Allocated EEPROM Space
00	0K byte
01	2K bytes
10	4K bytes
11	8K bytes

Table 22-9. Allocated RAM Memory Space

ram_sw2:ram_sw0	Allocated RAM Space	RAM Mappable Region	INITRM Bits Used	RAM Reset Base Address[1]
000	2K bytes	2K bytes	RAM[15:11]	0x0800
001	4K bytes	4K bytes	RAM[15:12]	0x0000
010	6K bytes	8K bytes[2]	RAM[15:13]	0x0800
011	8K bytes	8K bytes	RAM[15:13]	0x0000
100	10K bytes	16K bytes [2]	RAM[15:14]	0x1800

Table 22-11. Allocated FLASH/ROM Physical Memory Space

rom_sw1:rom_sw0	Allocated FLASH or ROM Space
00	0K byte
01	16K bytes
10	48K bytes(1)
11	64K bytes(1)

NOTES:

1. The ROMHM software bit in the MISC register determines the accessibility of the FLASH/ROM memory space. Please refer to Section 22.3.2.8, “Memory Size Register 1 (MEMSIZ1),” for a detailed functional description of the ROMHM bit.

Table 22-12. Allocated Off-Chip Memory Options

pag_sw1:pag_sw0	Off-Chip Space	On-Chip Space
00	876K bytes	128K bytes
01	768K bytes	256K bytes
10	512K bytes	512K bytes
11	0K byte	1M byte

NOTE

As stated, the bits in this register provide read visibility to the system memory space and on-chip/off-chip partitioning allocations defined at system integration. The actual array size for any given type of memory block may differ from the allocated size. Please refer to the device overview chapter for actual sizes.

22.3.2.9 Program Page Index Register (PPAGE)

	7	6	5	4	3	2	1	0
R	0	0	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
W								
Reset[1]	—	—	—	—	—	—	—	—

1. The reset state of this register is controlled at chip integration. Please refer to the device overview section to determine the actual reset state of this register.

= Unimplemented or Reserved

Figure 22-11. Program Page Index Register (PPAGE)

Read: Anytime

Write: Determined at chip integration. Generally it’s: “write anytime in all modes;” on some devices it will be: “write only in special modes.” Check specific device documentation to determine which applies.

Reset: Defined at chip integration as either 0x00 (paired with write in any mode) or 0x3C (paired with write only in special modes), see device overview chapter.

Table A-14. Voltage Regulator - Capacitive Loads

Num	Characteristic	Symbol	Min	Typical	Max	Unit
1	VDD external capacitive load	C_{DDext}	200	440	12000	nF
3	VDDPLL external capacitive load	$C_{DDPLLext}$	90	220	5000	nF

A.5 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

A.5.1 Startup

Table A-15 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block User Guide.

Table A-15. Startup Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	T	POR release level	V_{PORR}			2.07	V
2	T	POR assert level	V_{PORA}	0.97			V
3	D	Reset input pulse width, minimum input time	PW_{RSTL}	2			t_{osc}
4	D	Startup from Reset	n_{RST}	192		196	n_{osc}
5	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20			ns
6	D	Wait recovery startup time	t_{WRS}			14	t_{cyc}

A.5.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the VDD supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

A.5.1.2 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when VDD5 is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

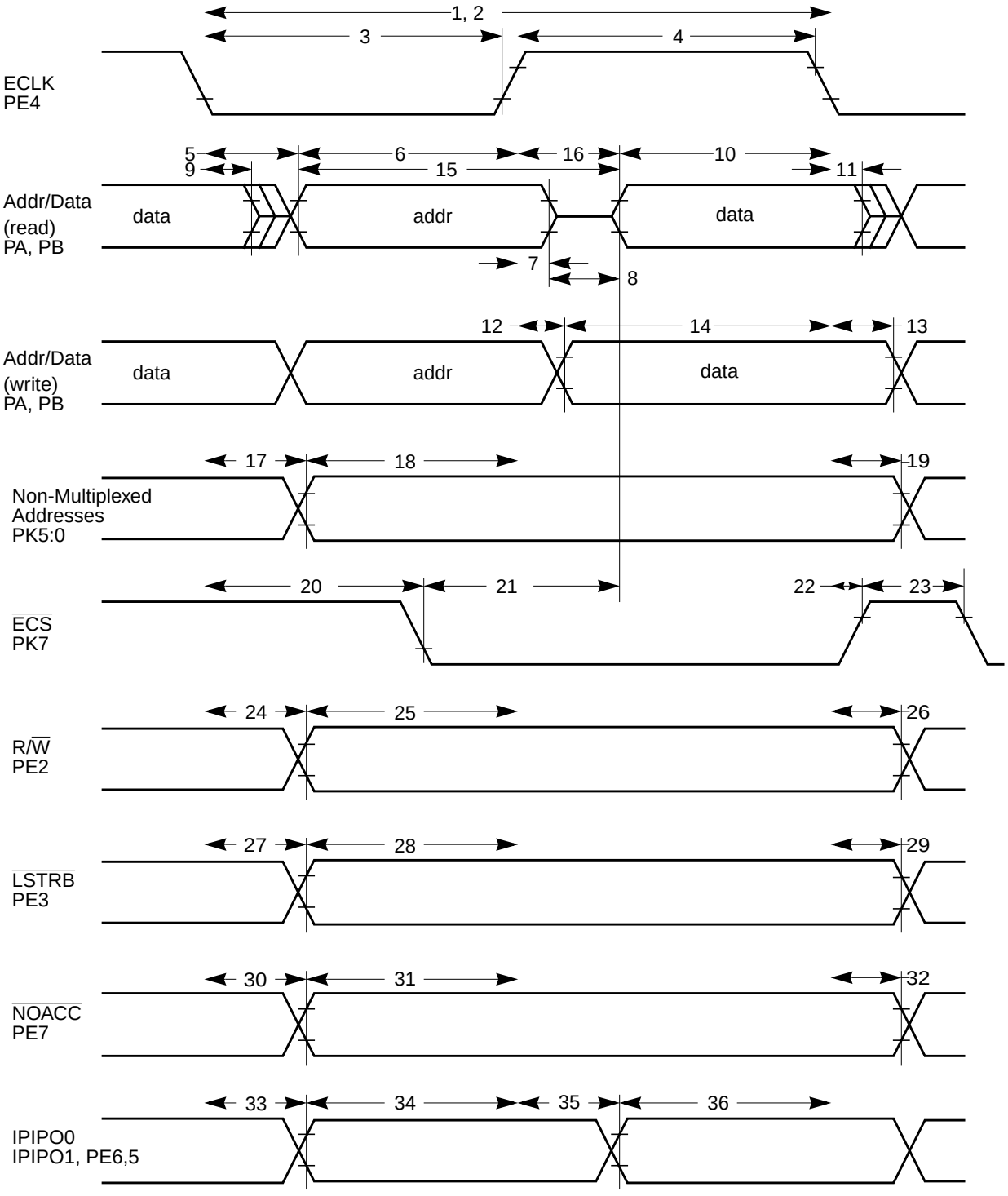

Figure A-10. General External Bus Timing

0x00D0–0x00D7 SCI1 (Asynchronous Serial Interface) (continued)

Address	Name		7	6	5	4	3	2	1	0
0x00D5	SCI1SR2	R	0	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		W								
0x00D6	SCI1DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x00D7	SCI1DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

0x00D8–0x00DF SPI (Serial Peripheral Interface)

Address	Name		7	6	5	4	3	2	1	0
0x00D8	SPICR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		W								
0x00D9	SPICR2	R	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		W								
0x00DA	SPIBR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		W								
0x00DB	SPISR	R	SPIF	0	SPTEF	MODF	0	0	0	0
		W								
0x00DC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00DD	SPIDR	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x00DE–0x00DF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x00E0–0x00FF PWM (Pulse Width Modulator 8 Bit 6 Channel) (Sheet 1 of 2)

Address	Name		7	6	5	4	3	2	1	0
0x00E0	PWME	R	0	0	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		W								
0x00E1	PWMPOL	R	0	0	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		W								
0x00E2	PWMCLK	R	0	0	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		W								
0x00E3	PWMPRCLK	R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		W								
0x00E4	PWMCAE	R	0	0	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		W								
0x00E5	PWMCTL	R	0	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		W								
0x00E6	PWMTST Test Only	R	0	0	0	0	0	0	0	0
		W								
0x00E7	PWMPRSC Test Only	R	0	0	0	0	0	0	0	0
		W								
0x00E8	PWMSCLA	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

0x0200–0x027F PIM (Port Integration Module) (Sheet 4 of 4)

Address	Name		7	6	5	4	3	2	1	0
0x0244	PERV	R	PERV7	PERV6	PERV5	PERV4	PERV3	PERV2	PERV1	PERV0
		W								
0x0245	PPSV	R	PPSV7	PPSV6	PPSV5	PPSV4	PPSV3	PPSV2	PPSV1	PPSV0
		W								
0x0246–0x024F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0250	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0251	PTAD	R	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
		W								
0x0252	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0253	PTIAD	R	PTIAD7	PTIAD6	PTIAD5	PTIAD4	PTIAD3	PTIAD2	PTIAD1	PTIAD0
		W								
0x0254	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0255	DDRAD	R	DDRAD7	DDRAD6	DDRAD5	DDRAD4	DDRAD3	DDRAD2	DDRAD1	DDRAD0
		W								
0x0256	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0257	RDRAD	R	RDRAD7	RDRAD6	RDRAD5	RDRAD4	RDRAD3	RDRAD2	RDRAD1	RDRAD0
		W								
0x0258	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0259	PERAD	R	PERAD7	PERAD6	PERAD5	PERAD4	PERAD3	PERAD2	PERAD1	PERAD0
		W								
0x025A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x025B	PPSAD	R	PPSAD7	PPSAD6	PPSAD5	PPSAD4	PPSAD3	PPSAD2	PPSAD1	PPSAD0
		W								
0x025C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x025D	PIEAD	R	PIEAD7	PIEAD6	PIEAD5	PIEAD4	PIEAD3	PIEAD2	PIEAD1	PIEAD0
		W								
0x025E	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x025F	PIFAD	R	PIFAD7	PIFAD6	PIFAD5	PIFAD4	PIFAD3	PIFAD2	PIFAD1	PIFAD0
		W								

0x0260–0x0287 Reserved

Address	Name		7	6	5	4	3	2	1	0
0x0260–0x0287	Reserved	R	0	0	0	0	0	0	0	0
		W								