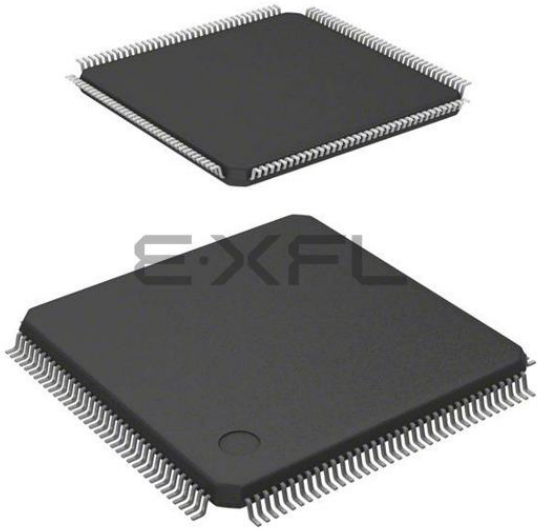

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10r167-q3-tr

II - PIN DATA (continued)

Table 1 : Pin list

Symbol	Pin	Type	Function		
P6.0 - P6.7	1 - 8	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bits. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The following Port 6 pins have alternate functions:		
	1	O	P6.0	$\overline{CS0}$	Chip Select 0 Output
	...	...	...	...	...
	5	O	P6.4	$\overline{CS4}$	Chip Select 4 Output
	6	I	P6.5	$\overline{HOLD}$	External Master Hold Request Input
	7	O	P6.6	$\overline{HLDA}$	Hold Acknowledge Output
	8	O	P6.7	$\overline{BREQ}$	Bus Request Output
P8.0 - P8.7	9 - 16	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bits. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins have alternate functions:		
	9	I/O	P8.0	CC16IO	CAPCOM2: CC16 Capture Input/Compare Output
	...	...	...	...	...
	16	I/O	P8.7	CC23IO	CAPCOM2: CC23 Capture Input/Compare Output
P7.0 - P7.7	19 - 26	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bits. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins have alternate functions:		
	19	O	P7.0	POUT0	PWM Channel 0 Output
	...	...	...	...	...
	22	O	P7.3	POUT3	PWM Channel 3 Output
	23	I/O	P7.4	CC28IO	CAPCOM2: CC28 Capture Input/Compare Output
	...	...	...	...	...
	26	I/O	P7.7	CC31IO	CAPCOM2: CC31 Capture Input/Compare Output
P5.0 - P5.9 P5.10 - P5.15	27 - 36 39 - 44	I I	Port 5 is a 16-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as the (up to 16) analog input channels for the A/D converter, where P5.x equals ANx (Analog input channel x), or they serve as timer inputs:		
	39	I	P5.10	T6EUD	GPT2 Timer T6 External Up/Down Control Input
	40	I	P5.11	T5EUD	GPT2 Timer T5 External Up/Down Control Input
	41	I	P5.12	T6IN	GPT2 Timer T6 Count Input
	42	I	P5.13	T5IN	GPT2 Timer T5 Count Input
	43	I	P5.14	T4EUD	GPT1 Timer T4 External Up/Down Control Input
	44	I	P5.15	T2EUD	GPT1 Timer T2 External Up/Down Control Input

IV - MEMORY ORGANIZATION

The memory space of the ST10R167 is configured in a Von-Neumann architecture. Code memory, data memory, registers and I/O ports are organized within the same linear address space of 16M Byte.

The entire memory space can be accessed Byte-wise or Wordwise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

ROM : 32K Byte of on-chip ROM.

RAM : 2K Byte of on-chip internal RAM (dual-port) is provided as a storage for data, system stack, general purpose register banks and code. The register bank can consist of up to 16 wordwide (R0 to R15) and/or Bytewide (RL0, RH0, …, RL7, RH7) general purpose registers.

XRAM : 2K Byte of on-chip extension RAM (single port XRAM) is provided as a storage for data, user stack and code.

The XRAM is connected to the internal XBUS and is accessed like an external memory in 16-bit demultiplexed bus-mode without waitstate or read/write delay (80ns access at 25MHz CPU clock). Byte and Word access is allowed.

The XRAM address range is 00'E000h - 00'E7FFh if the XRAM is enabled (XPEN bit 2 of SYSCON register). As the XRAM appears like external memory, it cannot be used for the ST10R167's system stack or register banks. The XRAM is not provided for single bit storage and therefore is not bit addressable. If bit XRAMEN is cleared, then any access in the address range 00'E000h - 00'E7FFh will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register.

SFR/ESFR : 1024 Byte (2 * 512 Byte) of address space is reserved for the special function register areas. SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units.

CAN : Address range 00'EF00h - 00'EFFFh is reserved for the CAN Module access. The CAN is enabled by setting XPEN bit 2 of the SYSCON register. Accesses to the CAN Module use demultiplexed addresses and a 16-bit data bus (Byte accesses are possible). Two wait states give an access time of 160ns at 25MHz CPU clock. No tristate waitstate is used.

Note If the CAN module is used, Port 4 can not be programmed to output all 8 segment address lines. Thus, only 4 segment address lines can be used, reducing the external memory space to 5M Byte (1M Byte per CS line).

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16M Byte of external RAM and/or ROM can be connected to the microcontroller.

VII - INTERRUPT SYSTEM

The interrupt response time for internal program execution is from 200ns to 480ns.

The ST10R167 architecture supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single Byte or Word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The ST10R167 has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A interrupt control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield is dedicated to each existing interrupt source. Thanks to its related register, each source can be programmed to one of sixteen interrupt priority levels. Once starting to be processed by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

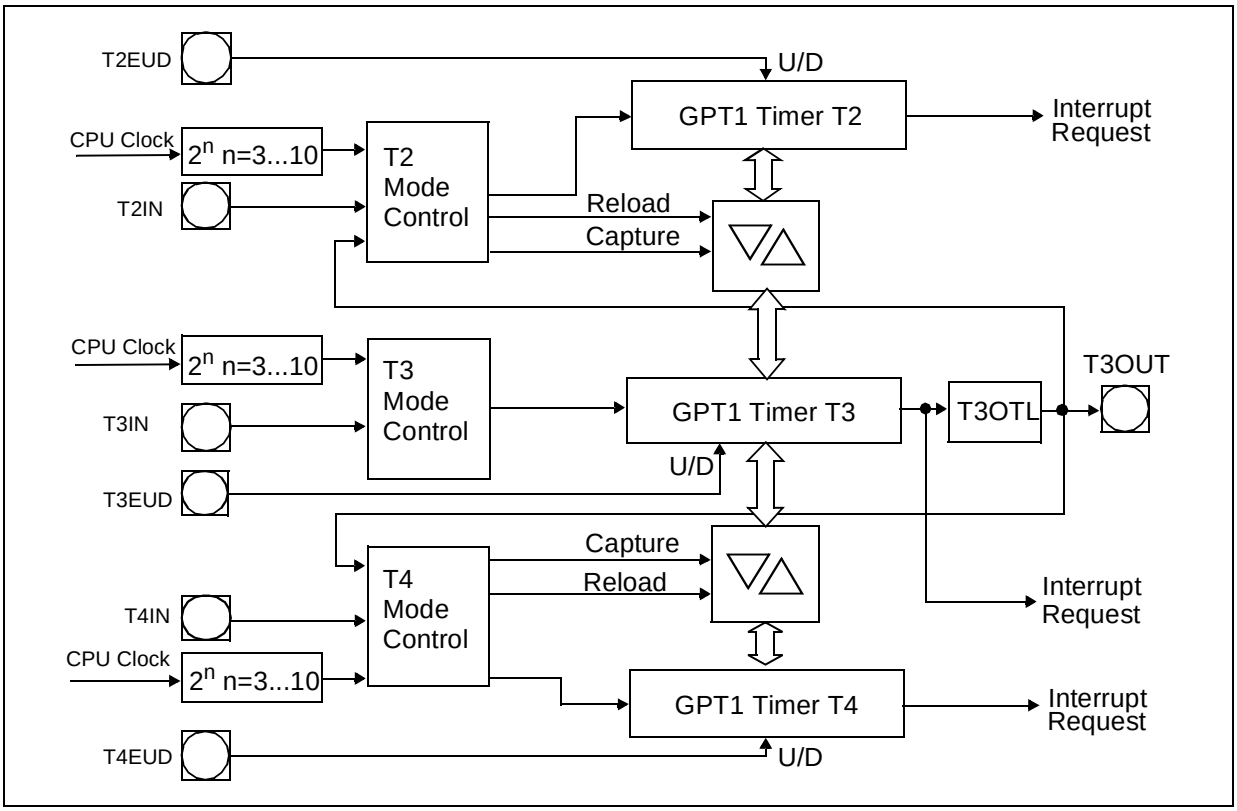
Table 2 shows all the available ST10R167 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers :

Table 2 : Interrupt sources

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	00'0040h	10h
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	00'0044h	11h
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	00'0048h	12h
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	00'004Ch	13h
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	00'0050h	14h
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	00'0054h	15h
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	00'0058h	16h
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	00'005Ch	17h
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	00'0060h	18h
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	00'0064h	19h
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	00'0068h	1Ah
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	00'006Ch	1Bh
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	00'0070h	1Ch
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	00'0074h	1Dh
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	00'0078h	1Eh
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	00'007Ch	1Fh
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	00'00C0h	30h
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	00'00C4h	31h

IX - GENERAL PURPOSE TIMER UNIT (continued)

Figure 5 : Block diagram of GPT1



IX.2 - GPT2

The GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6 which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT). The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is advantageous when T3 operates in Incremental Interface Mode.

Table 7 lists the timer input frequencies, resolution and periods for each pre-scaler option at 25MHz CPU clock.

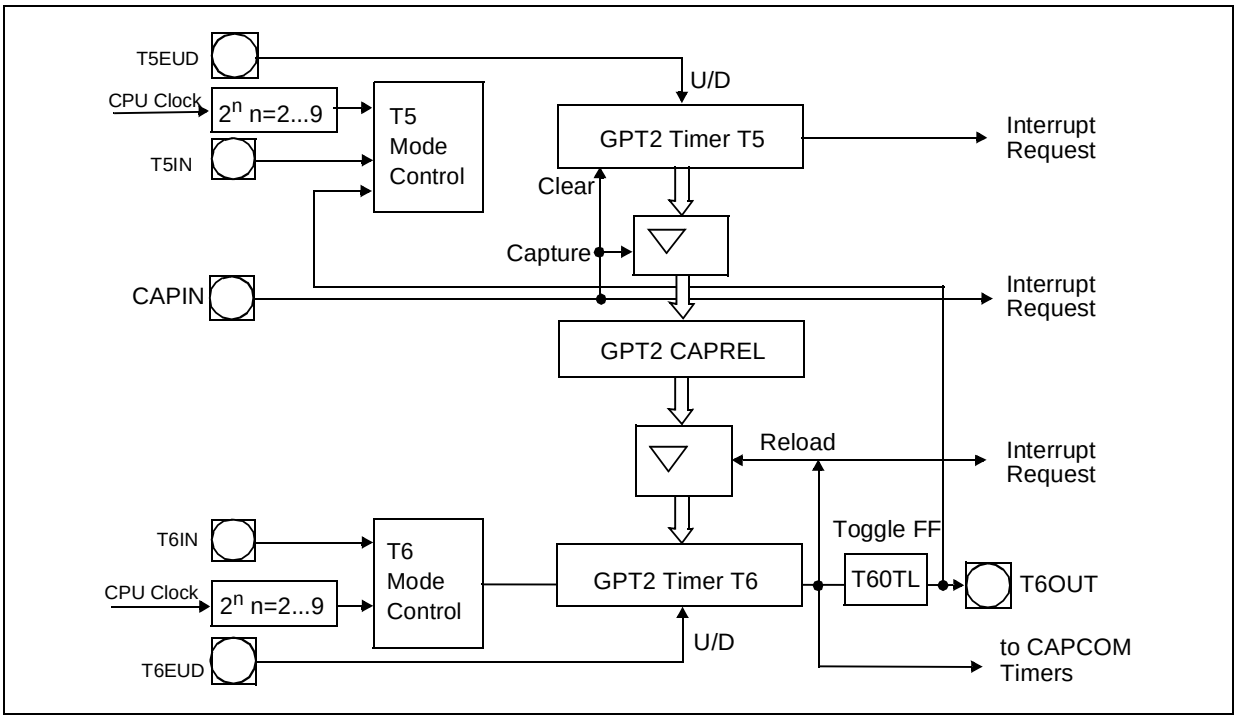
This also applies to the Gated Timer Mode of T6 and to the auxiliary timer T5 in Timer and Gated Timer Mode.

IX - GENERAL PURPOSE TIMER UNIT (continued)

Table 7 : GPT2 timer input frequencies, resolution and periods

f_{CPU} = 25MHz	Timer Input Selection T5I / T6I							
	000B	**001B**	**010B**	**011B**	**100B**	**101B**	**110B**	**111B**
Pre-scaler factor	4	8	16	32	64	128	256	512
Input Frequency	6.25MHz	3.125MHz	1.563MHz	781.3KHz	390.6KHz	195.3KHz	97.66KHz	48.83KHz
Resolution	160ns	320ns	640ns	1.28µs	2.56µs	5.12µs	10.24µs	20.48µs
Period	10.49ms	21.0ms	41.9ms	83.9ms	167ms	336ms	671ms	1.34s

Figure 6 : Block diagram of GPT2



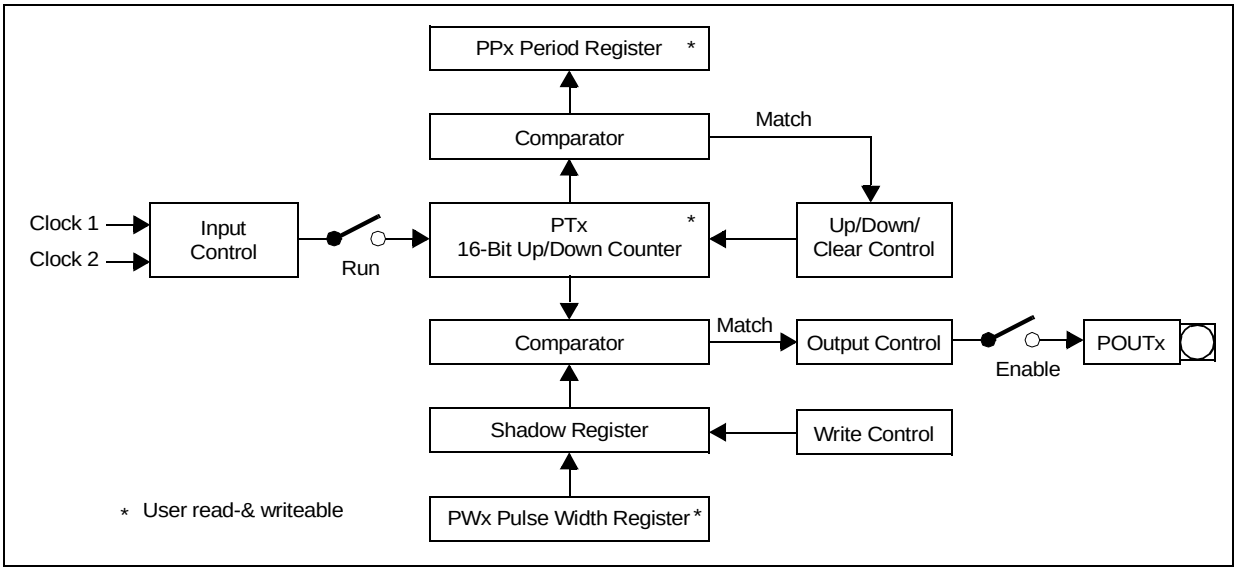
X - PWM MODULE

The pulse width modulation module can generate up to four PWM output signals using edge-aligned or centre-aligned PWM. In addition, the PWM module can generate PWM burst signals and single shot outputs. Table 8 shows the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM module can generate interrupt requests.

Table 8 : PWM unit frequencies and resolution at 25MHz clock

Mode 0	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU Clock/1	40ns	97.66KHz	24.41KHz	6.104KHz	1.526KHz	0.381KHz
CPU Clock/64	2.56ns	1.526KHz	381.5Hz	95.37Hz	23.84Hz	5.96Hz
Mode 1	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU Clock/1	40ns	48.82KHz	12.20KHz	3.05KHz	762.9Hz	190.7Hz
CPU Clock/64	2.56ns	762.9Hz	190.7 Hz	47.68Hz	11.92Hz	2.98Hz

Figure 7 : Block diagram of PWM module



XI - PARALLEL PORTS

The ST10R167 provides up to 111 I/O lines organized into eight input/output ports and one input port.

All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as input or output via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs.

The output drivers of five I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The input threshold of Port 2, Port 3, Port 7 and Port 8 is selectable (TTL-or CMOS-like), where the special CMOS-like input threshold reduces noise sensitivity due to the input hysteresis.

The input thresholds are selected with bit of PICON register dedicated to blocks of 8 input pins (2-bit for port2, 2-bit for port3, 1-bit for port7, 1-bit for port8).

All pins of I/O ports also support an alternate programmable function:

– Port0 and Port1 may be used as address and data lines when accessing external memory.

– Port 2, Port 7 and Port 8 are associated with the capture inputs or with the compare outputs of the CAPCOM units and/or with the outputs of the PWM module.

– Port 3 includes the alternate functions of timers, serial interfaces, the optional bus control signal $\overline{BHE}$ and the system clock output (CLKOUT).

– Port 4 outputs the additional segment address bits A16 to A23 in systems where segmentation is enabled to access more than 64K Byte of memory.

– Port 5 is used as analog input channels of the A/D converter or as timer control signals.

– Port 6 provides optional bus arbitration signals ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) and chip select signals.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

XII - A/D CONVERTER

A10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit is integrated on-chip. The sample time (for loading the capacitors) and the conversion time is programmable and can be adjusted to the external circuitry. Overrun error detection/protection is controlled by the ADDAT register. Either an interrupt request is generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended until the previous result has been read. For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins. The AD converter of the ST10F168 supports different conversion modes :

– **Single channel single conversion** : the analog level of the selected channel is sampled once and converted. The result of the conversion is stored in the ADDAT register.

– **Single channel continuous conversion** : the analog level of the selected channel is repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register.

– **Auto scan single conversion** : the analog level of the selected channels are sampled once and converted. After each conversion the result is stored in the ADDAT register. The data can be transfered to the RAM by interrupt software management or using the powerfull Peripheral Event Controller data transfert.

– **Auto scan continuous conversion** : the analog level of the selected channels are repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register. The data can be transfered to the RAM by interrupt software management or using the powerfull Peripheral Event Controller data transfert.

– **Wait for ADDAT read mode** : when using continuous modes, in order to avoid to overwrite the result of the current conversion by the next one, the ADWR bit of ADCON control register must be activated. Then, until the ADDAT register is read, the new result is stored in a temporary buffer and the conversion is on hold.

– **Channel injection mode** : when using continuous modes, a selected channel can be converted in between without changing the current operating mode. The 10 bit data of the conversion are stored in ADRES field of ADDAT2. The current continuous mode remains active after the single conversion is completed.

The Table : 9 ADC sample clock and conversion time shows the ADC unit conversion clock, sample clock.

A complete conversion will take $14t_{CC}$ + 2 t_{SC} + 4 TCL. This time includes the conversion it-self, the sampling time and the time required to transfer the digital value to the result register. For example, at 25MHz of CPU clock, minimum complete conversion time is 7.76µs.

The A/D converter provides automatic offset and linearity self calibration. The calibration operation is performed in two ways:

– A full calibration sequence is performed after a reset and lasts 1.6ms minimum (at 25MHz CPU clock). During this time, the ADBSY flag is set to indicate the operation. Normal conversion can be performed during this time. The duration of the calibration sequence is then extended by the time consumed by the conversions.
Note : After a power-on reset, the total unadjusted error (TUE) of the ADC might be worse than ±2LSB (max. ±4LSB). During the full calibration sequence, the TUE is constantly improved until at the end of the cycle, TUE is within the specified limits of ±2LSB.

– One calibration cycle is performed after each conversion : each calibration cycle takes 4 ADC clock cycles. These operation cycles ensure constant updating of the ADC accuracy, compensating changing operating conditions.

Table 9 : ADC sample clock and conversion time

ADCTC	Conversion Clock t_{CC}		ADSTC	Sample Clock t_{SC}	
	TCL[1] = 1/2 x f_{XTAL}	**At f_{CPU} = 25MHz**		**-**	**At f_{CPU} = 25MHz**
00	TCL x 24	0.48µs	00	t_{CC}	0.48µs[2]
01	Reserved, do not use	-	01	t_{CC} x 2	0.96µs[2]
10	TCL x 96	1.92µs	10	t_{CC} x 4	1.92µs[2]
11	TCL x 48	0.96µs	11	t_{CC} x 8	3.84µs[2]

Note 1. See chapter XX.
2. t_{CC} = TCL x 24.

XIX - SPECIAL FUNCTION REGISTER OVERVIEW (continued)

Table 14 : Special function registers listed by name (continued)

Name	Physical address	8-bit address	Description	Reset value
CC8IC b	FF88h	C4h	CAPCOM Register 8 Interrupt Control Register	0000h
CC9	FE92h	49h	CAPCOM Register 9	0000h
CC9IC b	FF8Ah	C5h	CAPCOM Register 9 Interrupt Control Register	0000h
CC10	FE94h	4Ah	CAPCOM Register 10	0000h
CC10IC b	FF8Ch	C6h	CAPCOM Register 10 Interrupt Control Register	0000h
CC11	FE96h	4Bh	CAPCOM Register 11	0000h
CC11IC b	FF8Eh	C7h	CAPCOM Register 11 Interrupt Control Register	0000h
CC12	FE98h	4Ch	CAPCOM Register 12	0000h
CC12IC b	FF90h	C8h	CAPCOM Register 12 Interrupt Control Register	0000h
CC13	FE9Ah	4Dh	CAPCOM Register 13	0000h
CC13IC b	FF92h	C9h	CAPCOM Register 13 Interrupt Control Register	0000h
CC14	FE9Ch	4Eh	CAPCOM Register 14	0000h
CC14IC b	FF94h	CAh	CAPCOM Register 14 Interrupt Control Register	0000h
CC15	FE9Eh	4Fh	CAPCOM Register 15	0000h
CC15IC b	FF96h	CBh	CAPCOM Register 15 Interrupt Control Register	0000h
CC16	FE60h	30h	CAPCOM Register 16	0000h
CC16IC b	F160h **E**	B0h	CAPCOM Register 16 Interrupt Control Register	0000h
CC17	FE62h	31h	CAPCOM Register 17	0000h
CC17IC b	F162h **E**	B1h	CAPCOM Register 17 Interrupt Control Register	0000h
CC18	FE64h	32h	CAPCOM Register 18	0000h
CC18IC b	F164h **E**	B2h	CAPCOM Register 18 Interrupt Control Register	0000h
CC19	FE66h	33h	CAPCOM Register 19	0000h
CC19IC b	F166h **E**	B3h	CAPCOM Register 19 Interrupt Control Register	0000h
CC20	FE68h	34h	CAPCOM Register 20	0000h
CC20IC b	F168h **E**	B4h	CAPCOM Register 20 Interrupt Control Register	0000h
CC21	FE6Ah	35h	CAPCOM Register 21	0000h
CC21IC b	F16Ah **E**	B5h	CAPCOM Register 21 Interrupt Control Register	0000h
CC22	FE6Ch	36h	CAPCOM Register 22	0000h
CC22IC b	F16Ch **E**	B6h	CAPCOM Register 22 Interrupt Control Register	0000h
CC23	FE6Eh	37h	CAPCOM Register 23	0000h
CC23IC b	F16Eh **E**	B7h	CAPCOM Register 23 Interrupt Control Register	0000h
CC24	FE70h	38h	CAPCOM Register 24	0000h
CC24IC b	F170h **E**	B8h	CAPCOM Register 24 Interrupt Control Register	0000h
CC25	FE72h	39h	CAPCOM Register 25	0000h
CC25IC b	F172h **E**	B9h	CAPCOM Register 25 Interrupt Control Register	0000h
CC26	FE74h	3Ah	CAPCOM Register 26	0000h
CC26IC b	F174h **E**	BAh	CAPCOM Register 26 Interrupt Control Register	0000h
CC27	FE76h	3Bh	CAPCOM Register 27	0000h

XX - ELECTRICAL CHARACTERISTICS

XX.1 - Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{SS}	Voltage on V_{DD} pins with respect to ground	-0.5, +6.5	V
V_{SS}	Voltage on any pin with respect to ground	-0.3 to V_{DD} +0.3	V
	Input current on any pin during overload condition	-10, +10	mA
	Absolute sum of all input currents during overload condition	|100|	mA
P_{tot}	Power Dissipation	1.5	W
T_{amb}	Ambient Temperature under bias	-40, +125	°C
T_{stg}	Storage Temperature	-65, +150	°C

Note Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN}>V_{DD} or V_{IN}<V_{SS}) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

XX.2 - Parameter interpretation

The parameters listed in the following tables represent the characteristics of the ST10C167 and its demands on the system. Where the ST10C167 logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the “Symbol” column.

Where the external system must provide signals with their respective timing characteristics to the ST10C167, the symbol “SR” for System Requirement is included in the “Symbol” column.

XX - ELECTRICAL CHARACTERISTICS (continued)

Notes 1. V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2. During the sample time the input capacitance C_I can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{SC} depend on programming and can be taken from the table above.

3. This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result. Values for the conversion clock t_{CC} depend on programming and can be taken from the table above.

4. This parameter is fixed by ADC control logic.

5. TUE is tested at V_{AREF} = 5.0V, V_{AGND} = 0V, V_{CC} = 4.9V. It is guaranteed by design characterization for all other voltages within the defined voltage range. The specified TUE is guaranteed only if an overload condition (see I_{OV} specification) occurs on maximum of 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10mA. During the reset calibration sequence the maximum TUE may be ±4 LSB.

6. During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within t_{CC}. The maximum internal resistance results from the programmed conversion timing.

7. Partially tested, guaranteed by design characterization.

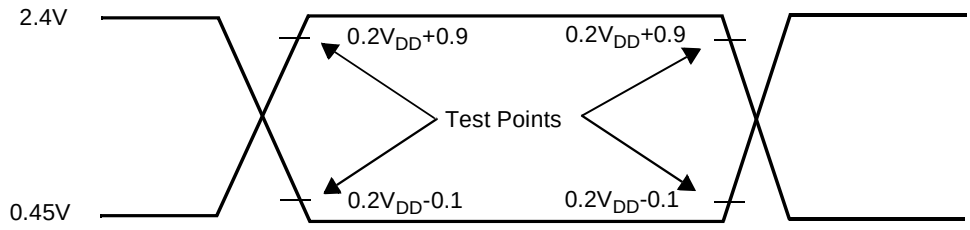
Sample time and conversion time of the ST10C167's ADC are programmable. The table below should be used to calculate the above timings.

ADCON.15|14 (ADCTC)	Conversion clock t_{CC}	ADCON.13|12 (ADSTC)	Sample clock t_{SC}
00	TCL * 24	00	t_{CC}
01	Reserved, do not use	01	t_{CC} * 2
10	TCL * 96	10	t_{CC} * 4
11	TCL * 48	11	t_{CC} * 8

XX.4 - AC characteristics

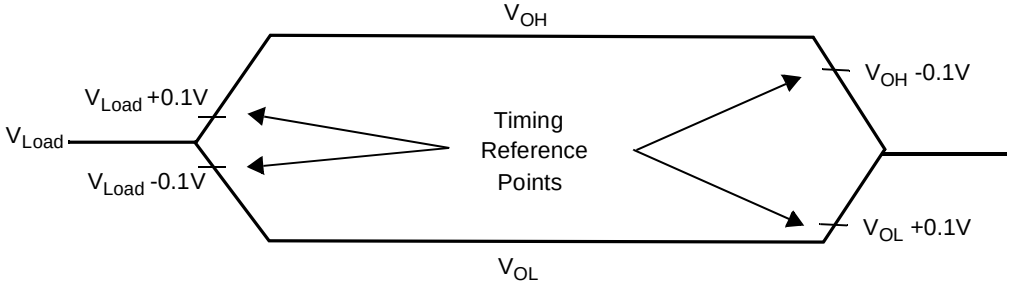
Test waveforms

Figure 9 : Input output waveforms



AC inputs during testing are driven at 2.4V for a logic '1' and 0.4V for a logic '0'.
Timing measurements are made at VIH min for a logic '1' and VIL max for a logic '0'.

Figure 10 : Float waveforms



For timing purposes a port pin is no longer floating when V_{LOAD} changes of ±100mV.
It begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20mA).

XX - ELECTRICAL CHARACTERISTICS (continued)

Table 18 : Multiplexed bus characteristics (continued)

Symbol		Parameter	Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			Min.	Max.	Min.	Max.	
t_{10}[1]	**CC**	Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	–	6	–	6	ns
t_{11}[1]	**CC**	Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	–	26	–	TCL + 6	ns
t_{12}	**CC**	$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	30 + t_C	–	2TCL - 10 + t_C	–	ns
t_{13}	**CC**	$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	50 + t_C	–	3TCL - 10 + t_C	–	ns
t_{14}	**SR**	$\overline{RD}$ to valid data in (with RW-delay)	–	20 + t_C	–	2TCL - 20+ t_C	ns
t_{15}	**SR**	$\overline{RD}$ to valid data in (no RW-delay)	–	40 + t_C	–	3TCL - 20+ t_C	ns
t_{16}	**SR**	ALE low to valid data in	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
t_{17}	**SR**	Address/Unlatched $\overline{CS}$ to valid data in	–	50 + 2t_A + t_C	–	4TCL - 30 + 2t_A + t_C	ns
t_{18}	**SR**	Data hold after $\overline{RD}$ rising edge	0	–	0	–	ns
t_{19}[1]	**SR**	Data float after $\overline{RD}$	–	26 + t_F	–	2TCL - 14 + t_F	ns
t_{22}	**CC**	Data valid to $\overline{WR}$	20 + t_C	–	2TCL - 20 + t_C	–	ns
t_{23}	**CC**	Data hold after $\overline{WR}$	26 + t_F	–	2TCL - 14 + t_F	–	ns
t_{25}	**CC**	ALE rising edge after $\overline{RD}$, $\overline{WR}$	26 + t_F	–	2TCL - 14 + t_F	–	ns
t_{27}	**CC**	Address/Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	26 + t_F	–	2TCL - 14 + t_F	–	ns
t_{38}	**CC**	ALE falling edge to Latched $\overline{CS}$	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
t_{39}	**SR**	Latched $\overline{CS}$ low to valid data in	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C + 2t_A	ns
t_{40}	**CC**	Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	46 + t_F	–	3TCL - 14 + t_F	–	ns
t_{42}	**CC**	ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	16 + t_A	–	TCL - 4 + t_A	–	ns
t_{43}	**CC**	ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	-4 + t_A	–	-4 + t_A	–	ns
t_{44}[1]	**CC**	Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	–	0	–	0	ns
t_{45}[1]	**CC**	Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	–	20	–	TCL	ns
t_{46}	**SR**	$\overline{RdCS}$ to Valid Data In (with RW delay)	–	16 + t_C	–	2TCL - 24 + t_C	ns
t_{47}	**SR**	$\overline{RdCS}$ to Valid Data In (no RW delay)	–	36 + t_C	–	3TCL - 24 + t_C	ns

XX - ELECTRICAL CHARACTERISTICS (continued)

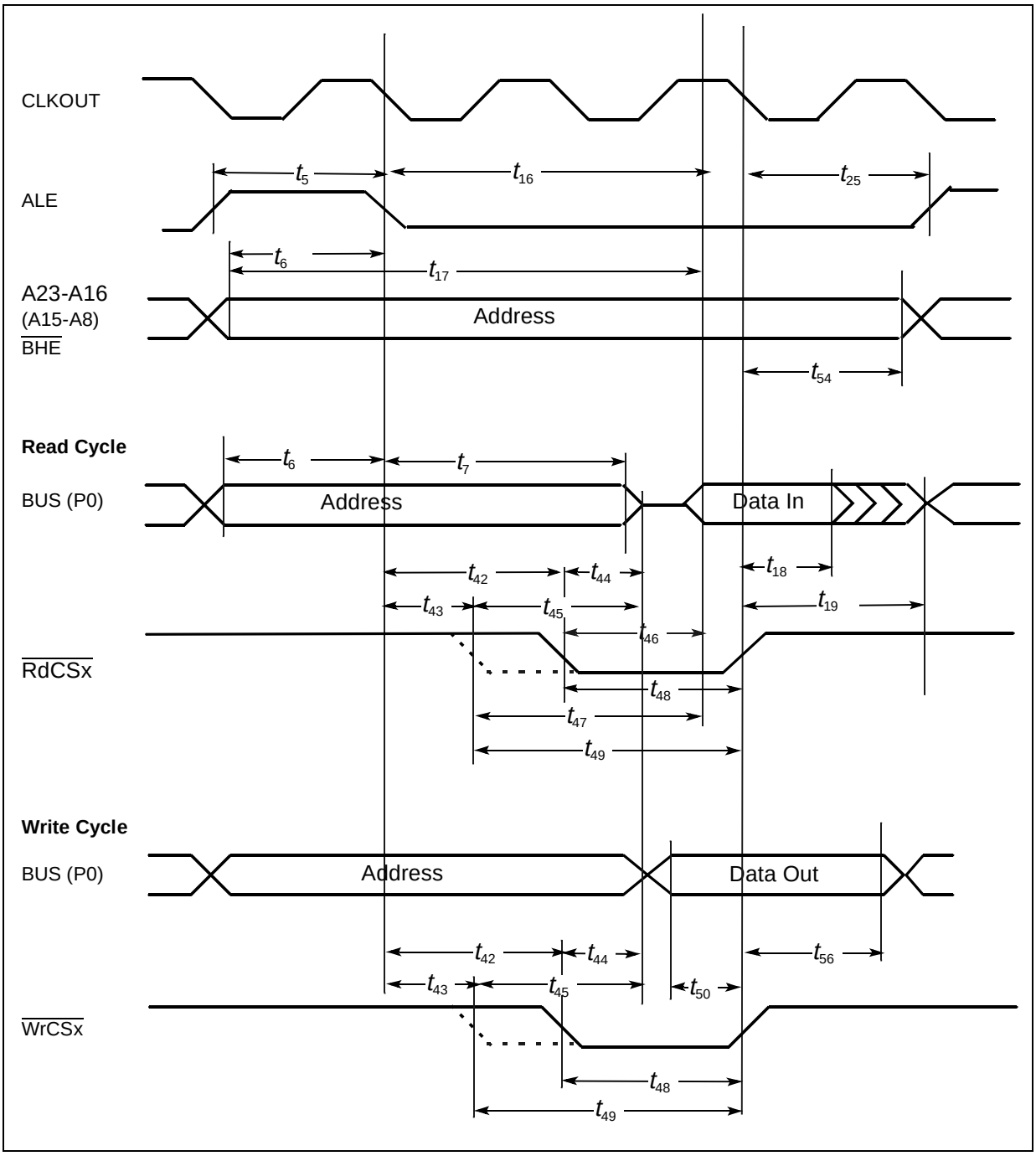
Table 18 : Multiplexed bus characteristics (continued)

Symbol		Parameter	Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			Min.	Max.	Min.	Max.	
t_{48}	**CC**	$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	30 + t_C	–	2TCL - 10 + t_C	–	ns
t_{49}	**CC**	$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	50 + t_C	–	3TCL - 10 + t_C	–	ns
t_{50}	**CC**	Data valid to $\overline{WrCS}$	26 + t_C	–	2TCL - 14+ t_C	–	ns
t_{51}	**SR**	Data hold after $\overline{RdCS}$	0	–	0	–	ns
t_{52}[1]	**SR**	Data float after $\overline{RdCS}$	–	20 + t_F	–	2TCL - 20 + t_F	ns
t_{54}	**CC**	Address hold after $\overline{RdCS}$, $\overline{WrCS}$	20 + t_F	–	2TCL - 20 + t_F	–	ns
t_{56}	**CC**	Data hold after $\overline{WrCS}$	20 + t_F	–	2TCL - 20 + t_F	–	ns

Note 1. Guaranteed by design characterization.

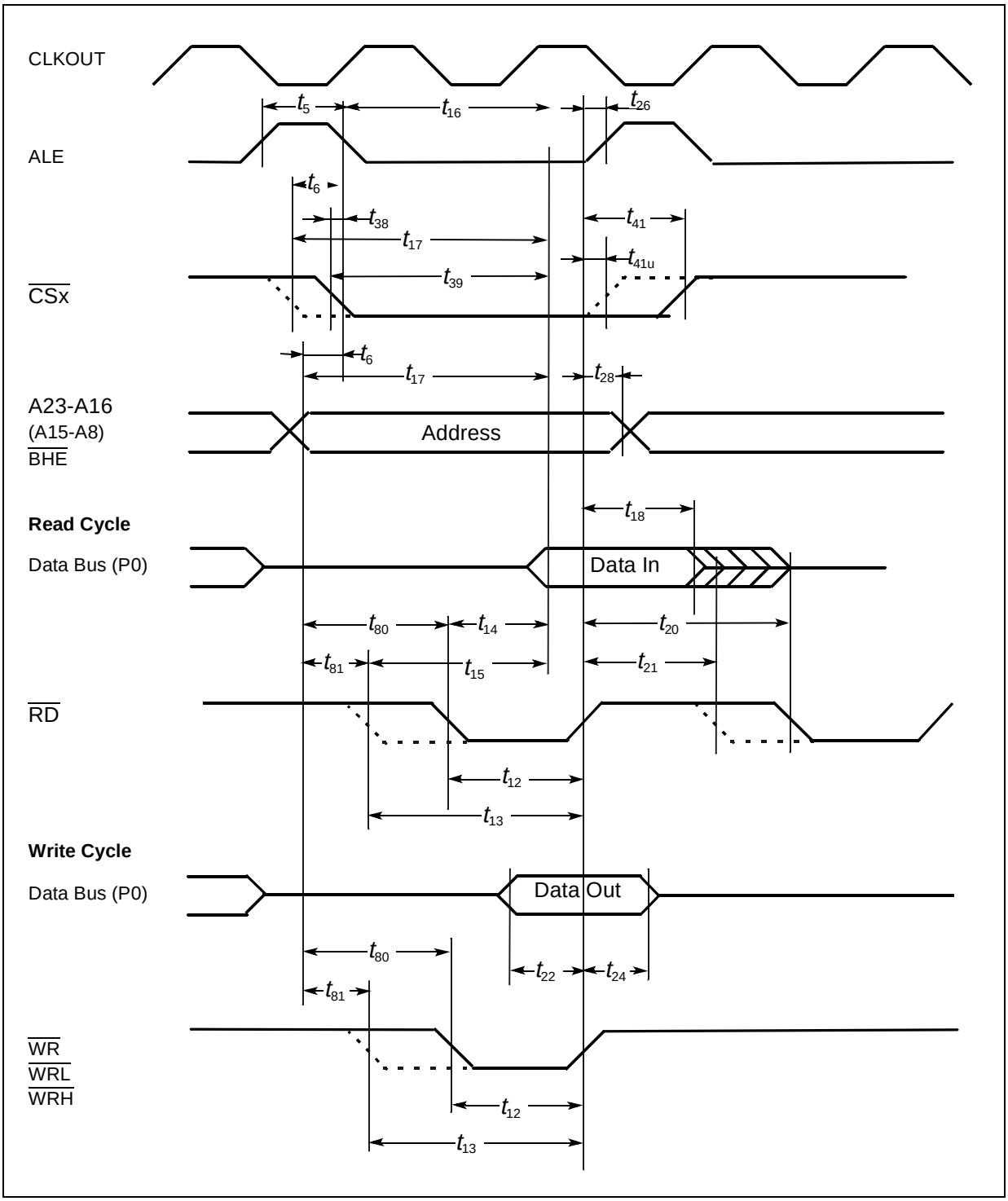
XX - ELECTRICAL CHARACTERISTICS (continued)

Figure 17 : External Memory Cycle: multiplexed bus, with/without read/write delay, extended ALE, read/write chip select



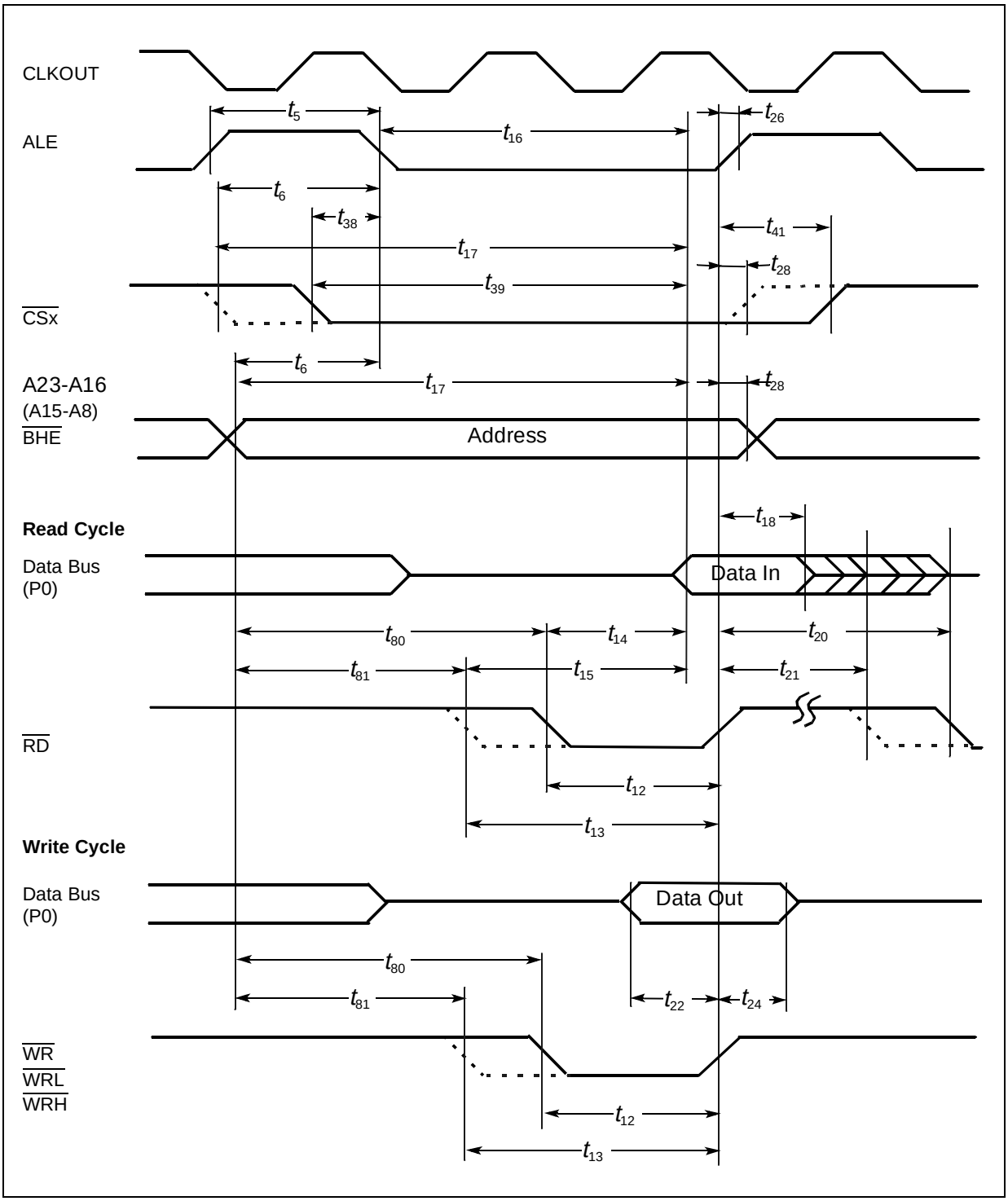
XX - ELECTRICAL CHARACTERISTICS (continued)

Figure 18 : External Memory Cycle: demultiplexed bus, with/without read/write delay, normal ALE



XX - ELECTRICAL CHARACTERISTICS (continued)

Figure 19 : External Memory Cycle: demultiplexed bus, with/without read/write delay, extended ALE



XX - ELECTRICAL CHARACTERISTICS (continued)

XX.4.11 - CLKOUT and $\overline{\text{READY}}$

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40 to +125°C
C_L (for Port0, Port1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100pF
C_L (for Port 6, $\overline{CS}$) = 100pF

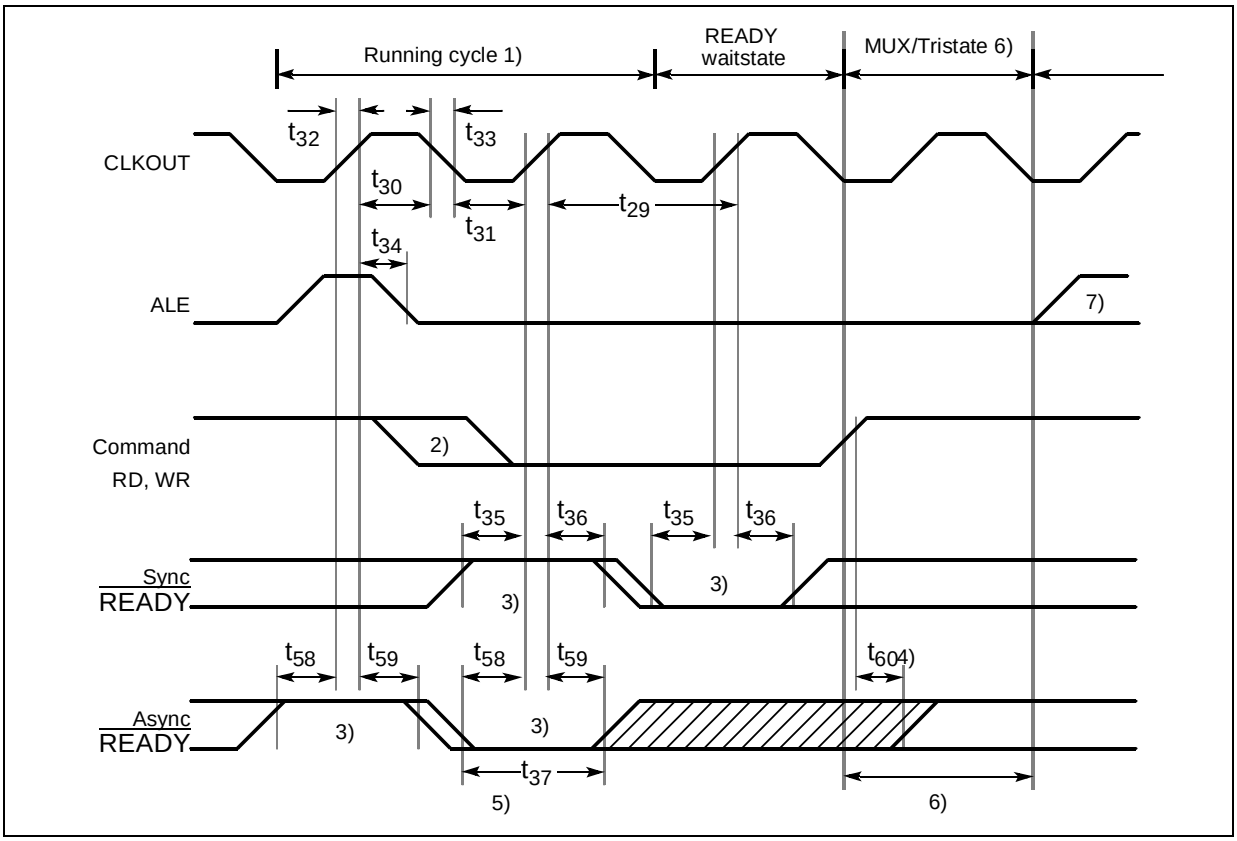
Table 20 : CLKOUT and $\overline{\text{READY}}$ characteristics

Symbol		Parameter	Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			Min.	Max.	Min.	Max.	
t_{29}	**CC**	CLKOUT cycle time	40	40	2TCL	2TCL	ns
t_{30}	**CC**	CLKOUT high time	14	–	TCL – 6	–	ns
t_{31}	**CC**	CLKOUT low time	10	–	TCL – 10	–	ns
t_{32}	**CC**	CLKOUT rise time	–	4	–	4	ns
t_{33}	**CC**	CLKOUT fall time	–	4	–	4	ns
t_{34}	**CC**	CLKOUT rising edge to ALE falling edge	$0 + t_A$	$10 + t_A$	$0 + t_A$	$10 + t_A$	ns
t_{35}	**SR**	Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	14	–	14	–	ns
t_{36}	**SR**	Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	4	–	4	–	ns
t_{37}	**SR**	Asynchronous $\overline{\text{READY}}$ low time	54	–	2TCL + 14	–	ns
t_{58}	**SR**	Asynchronous $\overline{\text{READY}}$ setup time [1]	14	–	14	–	ns
t_{59}	**SR**	Asynchronous $\overline{\text{READY}}$ hold time [1]	4	–	4	–	ns
t_{60}	**SR**	Async. $\overline{\text{READY}}$ hold time after $\overline{RD}$, $\overline{WR}$ high (Demultiplexed Bus) [2]	0	$0 + 2t_A + t_C + t_F$ [2]	0	TCL - 20 $+ 2t_A + t_C + t_F$ [2]	ns

Notes 1.These timings are given for test purposes only, in order to assure recognition at a specific clock edge.
2. Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating READY.
The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.

XX - ELECTRICAL CHARACTERISTICS (continued)

Figure 22 : CLKOUT and $\overline{\text{READY}}$



Notes 1. Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).

2. The leading edge of the respective command depends on RW-delay.

3. $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a READY controlled wait state, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.

4. $\overline{\text{READY}}$ may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).

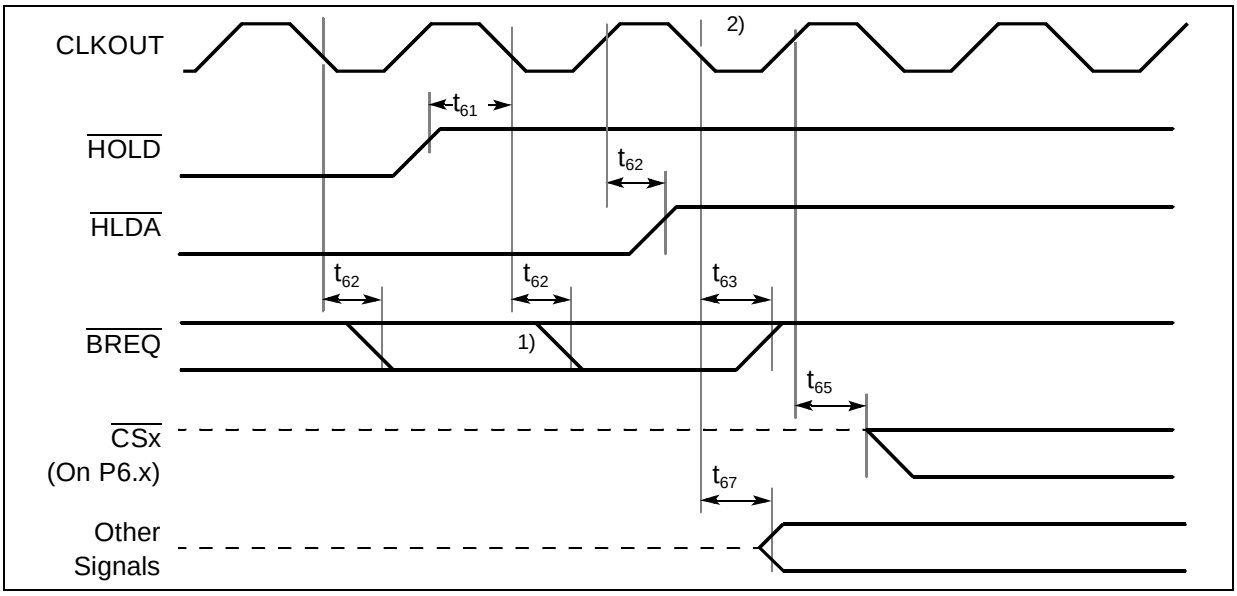
5. If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t 37 in order to be safely synchronized. This is guaranteed, if READY is removed in response to the command (see Note 4)).

6. Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here. For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.

7. The next external bus cycle may start here.

XX - ELECTRICAL CHARACTERISTICS (continued)

Figure 24 : External bus arbitration, (regaining the bus)



Notes 1. This is the last opportunity for BREQ to trigger the indicated regain-sequence. Even if BREQ is activated earlier, the regain-sequence is initiated by HOLD going high. Please note that HOLD may also be deactivated without the ST10C167 requesting the bus.
2. The next ST10C167 driven bus cycle may start here.