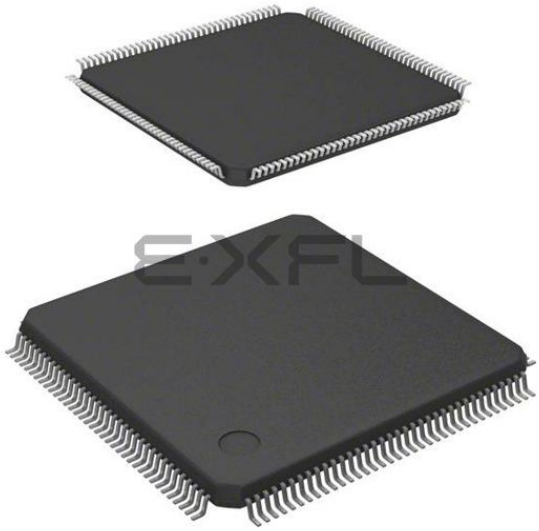

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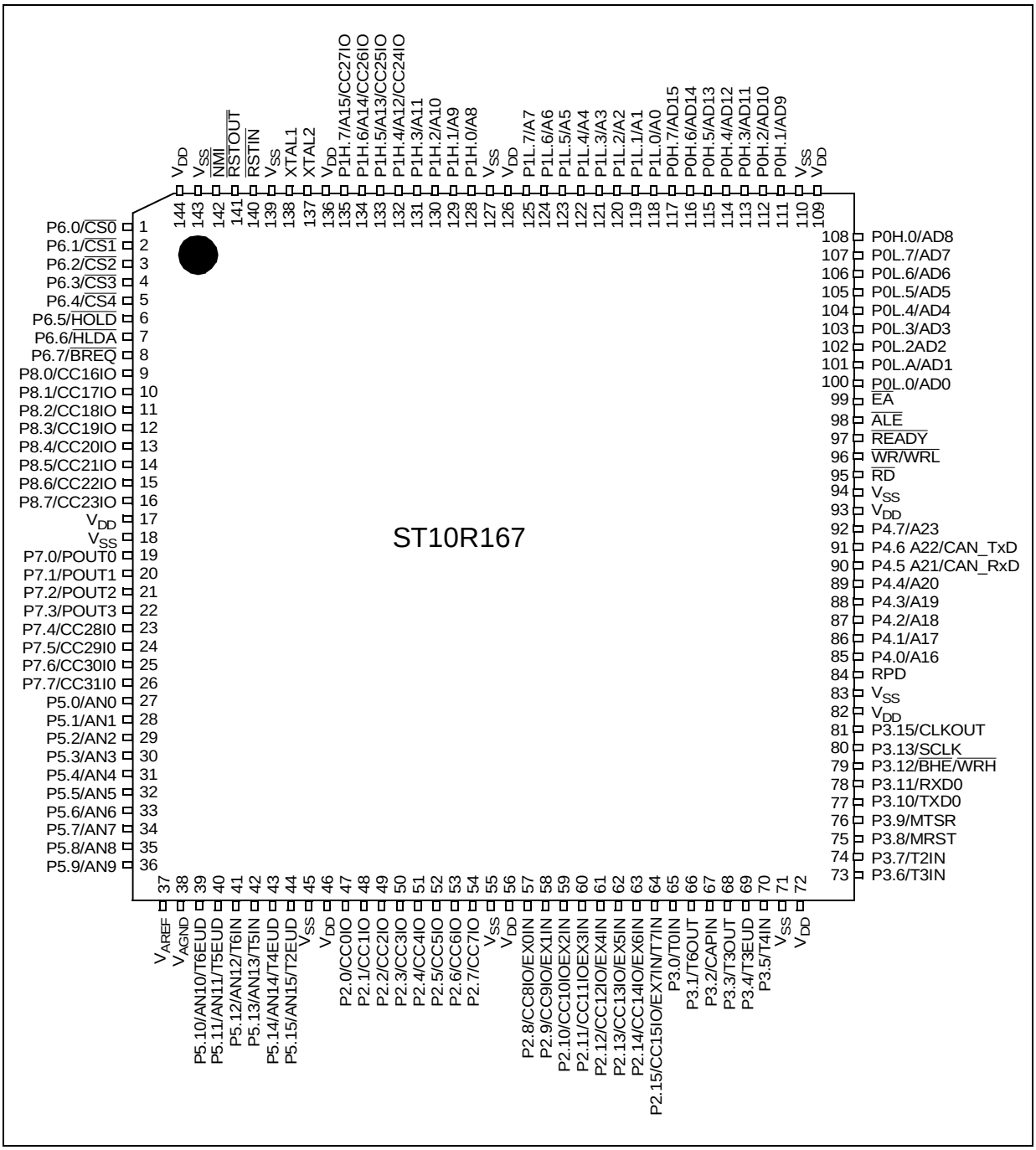
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	144-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10r167-q3

II - PIN DATA

Figure 2 : Pin Configuration (top view)



II - PIN DATA (continued)

Table 1 : Pin list (continued)

Symbol	Pin	Type	Function
P2.0 - P2.7 P2.8 - P2.15	47 - 54 57 - 64	I/O	16-bit bidirectional I/O port, bit-wise programmable for input or output via direction bits. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins have alternate functions:
	47 ... 54 57 ... 64	I/O ... I/O I/O I ... I/O I I	P2.0 CC0IO CAPCOM: CC0 Capture Input/Compare Output ... ... P2.7 CC7IO CAPCOM: CC7 Capture Input/Compare Output P2.8 CC8IO CAPCOM: CC8 Capture Input/Compare Output EX0IN Fast External Interrupt 0 Input ... ... P2.15 CC15IO CAPCOM: CC15 Capture Input/Compare Output EX7IN Fast External Interrupt 7 Input T7IN CAPCOM2 Timer T7 Count Input
P3.0 - P3.5 P3.6 - P3.13 P3.15	65 - 70 73 - 80 81	I/O I/O I/O	15-bit (P3.14 is missing) bidirectional I/O port, bit-wise programmable for input or output via direction bits. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins have alternate functions:
	65 66 67 68 69 70 73 74 75 76 77 78 79 80 81	I O I O I I I I I/O I/O I/O O O I/O O	P3.0 T0IN CAPCOM Timer T0 Count Input P3.1 T6OUT GPT2 Timer T6 Toggle Latch Output P3.2 CAPIN GPT2 Register CAPREL Capture Input P3.3 T3OUT GPT1 Timer T3 Toggle Latch Output P3.4 T3EUD GPT1 Timer T3 External Up/Down Control Input P3.5 T4IN GPT1 Timer T4 Input for Count/Gate/Reload/Capture P3.6 T3IN GPT1 Timer T3 Count/Gate Input P3.7 T2IN GPT1 Timer T2 Input for Count/Gate/Reload/Capture P3.8 MRST SSC Master-Receive/Slave-Transmit I/O P3.9 MTSR SSC Master-Transmit/Slave-Receive O/I P3.10 TxD0 ASC0 Clock/Data Output (Asynchronous/Synchronous) P3.11 $\overline{\text{RxD0}}$ ASC0 Data Input (Asyn.) or I/O (Synchronous) P3.12 $\overline{\text{BHE}}$ External Memory High Byte Enable Signal, $\overline{\text{WRH}}$ External Memory High Byte Write Strobe P3.13 SCLK SSC Master Clock Output/Slave Clock Input P3.15 CLKOUT System Clock Output (=CPU Clock)
P4.0 - P4.7	85 - 92	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bits. Programming an I/O pin as input forces the corresponding output driver to high impedance state. For external bus configuration, Port 4 can be used to output the segment address lines:
	85 - 89 90 91 92	O O I O O O	P4.0 - P4.4 A16 - A20 Least Significant Segment Address Line P4.5 A21 Segment Address Line CAN_RxD CAN Receive Data Input P4.6 A22 Segment Address Line, CAN_TxD CAN Transmit Data Output P4.7 A23 Most Significant Segment Address Line
$\overline{\text{RD}}$	95	O	External Memory Read Strobe. $\overline{\text{RD}}$ is activated for every external instruction or data read access.

II - PIN DATA (continued)

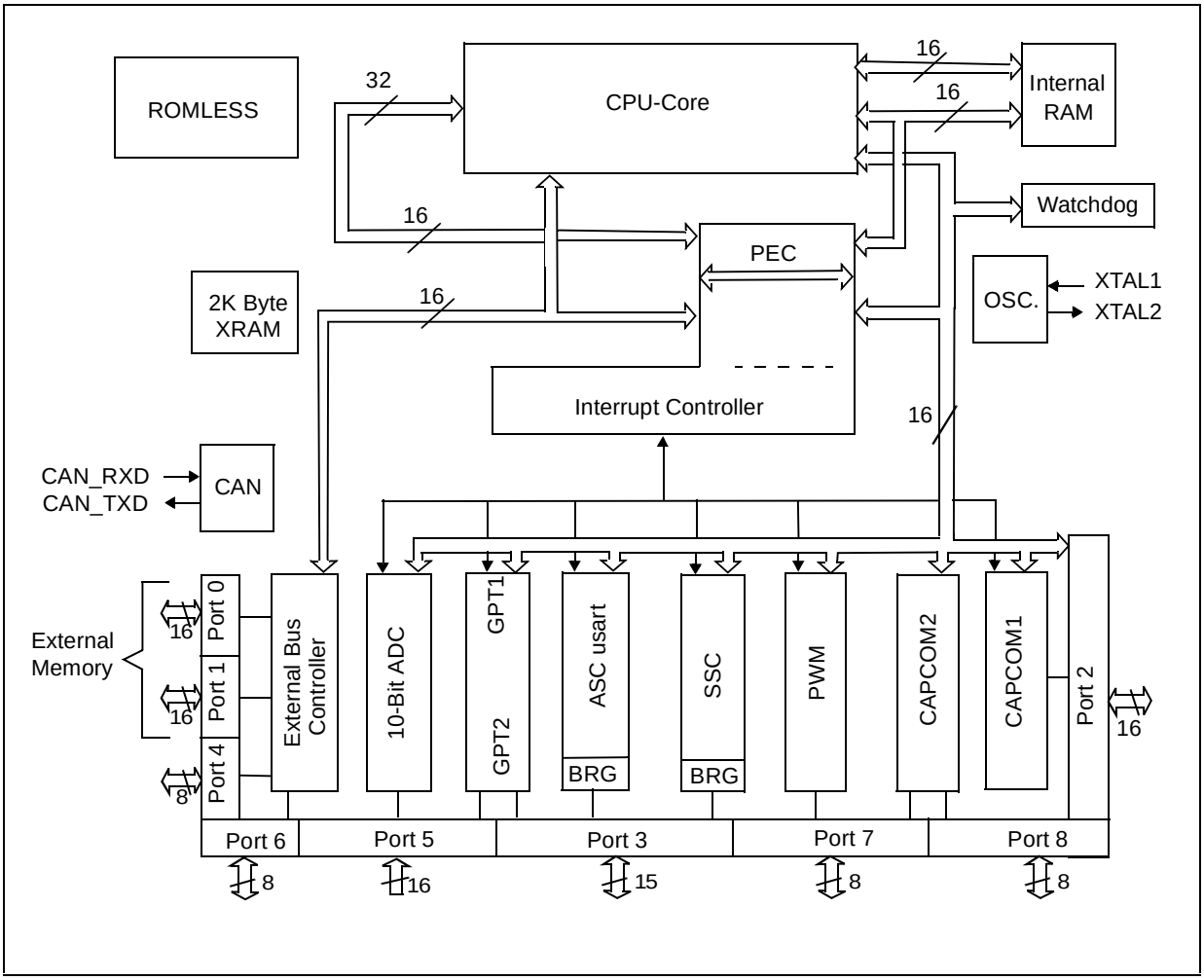
Table 1 : Pin list (continued)

Symbol	Pin	Type	Function
$\overline{\text{RSTOUT}}$	141	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog-timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	142	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. If bit PWDCFG = '0' in SYSCON register, when the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the ST10R167 to go into power down mode. If $\overline{\text{NMI}}$ is high and PWDCFG ='0', when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.
V_{AREF}	37	-	Reference voltage for the A/D converter.
V_{AGND}	38	-	Reference ground for the A/D converter.
RPD	84	-	This pin is used as the timing pin for the return from powerdown circuit and power-up asynchronous reset.
V_{DD}	17, 46, 56, 72, 82, 93, 109, 126, 136, 144	-	Digital Supply Voltage: = + 5V during normal operation and idle mode. $\geq$ + 2.5V during power down mode
V_{SS}	18, 45, 55, 71, 83, 94, 110, 127, 139, 143	-	Digital Ground.

III - FUNCTIONAL DESCRIPTION

The architecture of the ST10R167 combines advantages of both RISC and CISC processors and an advanced peripheral subsystem. The block diagram gives an overview of the different on-chip components and the high bandwidth internal bus structure of the ST10R167.

Figure 3 : Block diagram



VI - EXTERNAL BUS CONTROLLER

All of the external memory accesses are performed by the on-chip external bus controller. The EBC can be programmed to single chip mode when no external memory is required, or to one of four different external memory access modes:

– 16-/18-/20-/24-bit addresses and 16-bit data, demultiplexed.
– 16-/18-/20-/24-bit addresses and 16-bit data, multiplexed.
– 16-/18-/20-/24-bit addresses and 8-bit data, multiplexed.
– 16-/18-/20-/24-bit addresses and 8-bit data, demultiplexed.

In demultiplexed bus modes addresses are output on Port1 and data is input/output on Port0 or P0L, respectively. In the multiplexed bus modes both addresses and data use Port0 for input/output.

Timing characteristics of the external bus interface (memory cycle time, memory tri-state time, length of ALE and read/write delay) are programmable giving the choice of a wide range of memories and external peripherals. Up to 4 independent address windows may be defined (using register pairs ADDRSELx / BUSCONx) to access different resources and bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0. Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported by a 'Ready' function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration which shares external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register SYSCON. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In master mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to'1' the slave mode is selected where pin $\overline{HLDA}$ is switched to input. This directly connects the slave controller to another master controller without glue logic.

For applications which require less external memory space, the address space can be restricted to 1M Byte, 256K Byte or to 64K Byte. Port 4 outputs all 8 address lines if an address space of 16M Byte is used, otherwise four, two or no address lines.

Chip select timing can be made programmable. By default (after reset), the CSx lines change half a CPU clock cycle after the rising edge of ALE. With the CSCFG bit set in the SYSCON register the CSx lines change with the rising edge of ALE.

The active level of the READY pin can be set by bit RDYPOL in the BUSCONx registers. When the READY function is enabled for a specific address window, each bus cycle within the window must be terminated with the active level defined by bit RDYPOL in the associated BUSCON register.

VIII - CAPTURE/COMPARE (CAPCOM) UNIT

The ST10R167 has two 16 channel CAPCOM units. They support generation and control of timing sequences on up to 32 channels with a maximum resolution of 320ns at 25MHz CPU clock. The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/ underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Each of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare functions. Each register has one associated port pin which serves as an input pin for triggering the capture function, or as an output pin (except for CC24...CC27) to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (captured) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/ compare register, specific actions will be taken based on the selected compare mode (see Table 4).

The input frequencies f_{TX} for Tx are determined as a function of the CPU clocks. The formulas are detailed in the user manual. The timer input frequencies, resolution and periods which result from the selected pre-scaler option in TxI when using a 25MHz CPU clock are listed in the table below. The numbers for the timer periods are based on a reload value of 0000_H. Note that some numbers may be rounded to 3 significant figures (see Table 5).

Table 4 : Compare modes

Compare Modes	Function
Mode 0	Interrupt-only compare mode ; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match ; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode ; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare time overflow ; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match ; several compare events per timer period are possible.

Table 5 : CAPCOM timer input frequencies, resolution and periods

f_{CPU} = 25MHz	Timer Input Selection TxI							
	000_B	001_B	010_B	011_B	100_B	101_B	110_B	111_B
Pre-scaler for f_{CPU}	8	16	32	64	128	256	512	1024
Input Frequency	3.125MHz	1.56MHz	781KHz	391KHz	195KHz	97.7KHz	48.8KHz	24.4KHz
Resolution	320ns	640ns	1.28µs	2.56µs	5.12µs	10.24µs	20.48µs	40.96µs
Period	21.0ms	41.9ms	83.9ms	167ms	336ms	671ms	1.34s	2.68s

IX - GENERAL PURPOSE TIMER UNIT

The GPT unit is a flexible multifunctional timer/ counter structure which is used for time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication. The GPT unit contains five 16-bit timers organized into two separate modules GPT1 and GPT2. Each timer in each module may operate independently in several different modes, or may be concatenated with another timer of the same module.

IX.1 - GPT1

Each of the three timers T2, T3, T4 of the GPT1 module can be configured individually for one of four basic modes of operation: **timer**, **gated timer**, **counter mode and incremental interface mode**. In timer mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler. In counter mode, the timer is clocked in reference to external events. Pulse width or duty cycle measurement is supported in gated timer mode where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which is the gate or the clock input.

The table below lists the timer input frequencies, resolution and periods for each pre-scaler option at 25MHz CPU clock. This also applies to the Gated Timer Mode of T3 and to the auxiliary timers T2 and T4 in Timer and Gated Timer Mode (see Table 6).

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD).

In Incremental Interface Mode, the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B by their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has output toggle latches (TxOTL) which changes state on each timer over-flow/underflow. The state of this latch may be output on port pins (TxOUT) e. g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for high resolution measurement of long time periods.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

Table 6 : GPT1 timer input frequencies, resolution and periods

f_{CPU} = 25MHz	Timer Input Selection T2I / T3I / T4I							
	000_B	001_B	010_B	011_B	100_B	101_B	110_B	111_B
Pre-scaler factor	8	16	32	64	128	256	512	1024
Input Frequency	3.125MHz	1.563MHz	781.3KHz	390.6KHz	195.3KHz	97.66KHz	48.83KHz	24.41KHz
Resolution	320ns	640ns	1.28µs	2.56µs	5.12µs	10.24µs	20.48µs	40.96µs
Period	21.0ms	41.9ms	83.9ms	167ms	336ms	671ms	1.34s	2.68s

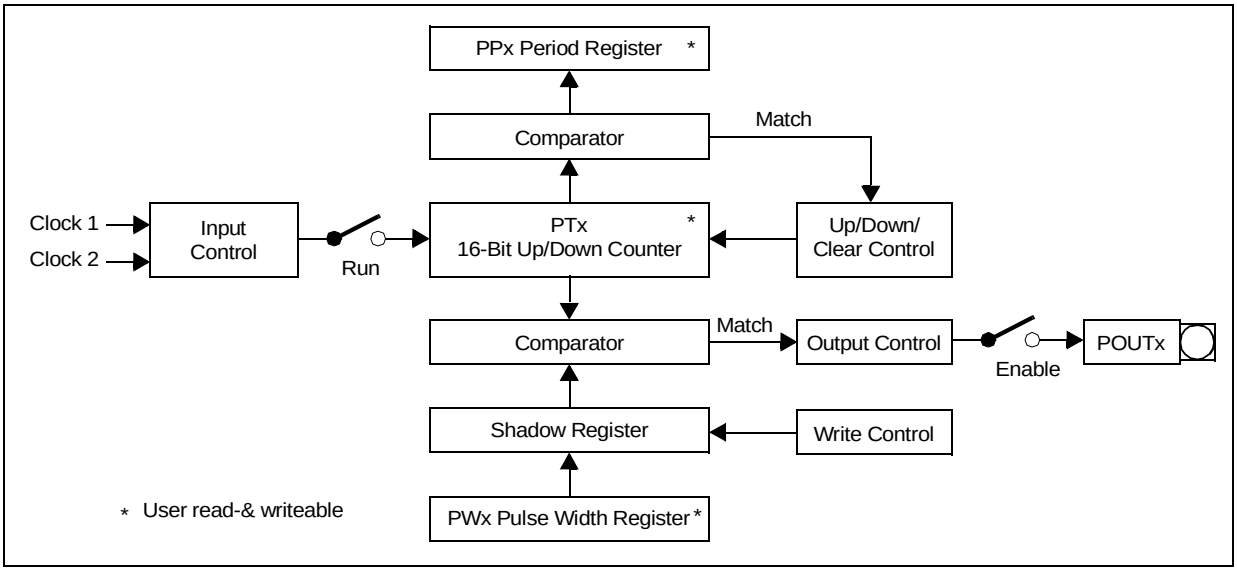
X - PWM MODULE

The pulse width modulation module can generate up to four PWM output signals using edge-aligned or centre-aligned PWM. In addition, the PWM module can generate PWM burst signals and single shot outputs. Table 8 shows the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM module can generate interrupt requests.

Table 8 : PWM unit frequencies and resolution at 25MHz clock

Mode 0	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU Clock/1	40ns	97.66KHz	24.41KHz	6.104KHz	1.526KHz	0.381KHz
CPU Clock/64	2.56ns	1.526KHz	381.5Hz	95.37Hz	23.84Hz	5.96Hz
Mode 1	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU Clock/1	40ns	48.82KHz	12.20KHz	3.05KHz	762.9Hz	190.7Hz
CPU Clock/64	2.56ns	762.9Hz	190.7 Hz	47.68Hz	11.92Hz	2.98Hz

Figure 7 : Block diagram of PWM module



XII - A/D CONVERTER

A10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit is integrated on-chip. The sample time (for loading the capacitors) and the conversion time is programmable and can be adjusted to the external circuitry. Overrun error detection/protection is controlled by the ADDAT register. Either an interrupt request is generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended until the previous result has been read. For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins. The AD converter of the ST10F168 supports different conversion modes :

– **Single channel single conversion** : the analog level of the selected channel is sampled once and converted. The result of the conversion is stored in the ADDAT register.

– **Single channel continuous conversion** : the analog level of the selected channel is repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register.

– **Auto scan single conversion** : the analog level of the selected channels are sampled once and converted. After each conversion the result is stored in the ADDAT register. The data can be transfered to the RAM by interrupt software management or using the powerfull Peripheral Event Controller data transfert.

– **Auto scan continuous conversion** : the analog level of the selected channels are repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register. The data can be transfered to the RAM by interrupt software management or using the powerfull Peripheral Event Controller data transfert.

– **Wait for ADDAT read mode** : when using continuous modes, in order to avoid to overwrite the result of the current conversion by the next one, the ADWR bit of ADCON control register must be activated. Then, until the ADDAT register is read, the new result is stored in a temporary buffer and the conversion is on hold.

– **Channel injection mode** : when using continuous modes, a selected channel can be converted in between without changing the current operating mode. The 10 bit data of the conversion are stored in ADRES field of ADDAT2. The current continuous mode remains active after the single conversion is completed.

The Table : 9 ADC sample clock and conversion time shows the ADC unit conversion clock, sample clock.

A complete conversion will take $14t_{CC}$ + 2 t_{SC} + 4 TCL. This time includes the conversion it-self, the sampling time and the time required to transfer the digital value to the result register. For example, at 25MHz of CPU clock, minimum complete conversion time is 7.76µs.

The A/D converter provides automatic offset and linearity self calibration. The calibration operation is performed in two ways:

– A full calibration sequence is performed after a reset and lasts 1.6ms minimum (at 25MHz CPU clock). During this time, the ADBSY flag is set to indicate the operation. Normal conversion can be performed during this time. The duration of the calibration sequence is then extended by the time consumed by the conversions.
Note : After a power-on reset, the total unadjusted error (TUE) of the ADC might be worse than ±2LSB (max. ±4LSB). During the full calibration sequence, the TUE is constantly improved until at the end of the cycle, TUE is within the specified limits of ±2LSB.

– One calibration cycle is performed after each conversion : each calibration cycle takes 4 ADC clock cycles. These operation cycles ensure constant updating of the ADC accuracy, compensating changing operating conditions.

Table 9 : ADC sample clock and conversion time

ADCTC	Conversion Clock t_{CC}		ADSTC	Sample Clock t_{SC}	
	TCL[1] = 1/2 x f_{XTAL}	**At f_{CPU} = 25MHz**		**-**	**At f_{CPU} = 25MHz**
00	TCL x 24	0.48µs	00	t_{CC}	0.48µs[2]
01	Reserved, do not use	-	01	t_{CC} x 2	0.96µs[2]
10	TCL x 96	1.92µs	10	t_{CC} x 4	1.92µs[2]
11	TCL x 48	0.96µs	11	t_{CC} x 8	3.84µs[2]

Note 1. See chapter XX.
2. t_{CC} = TCL x 24.

XVII - SYSTEM RESET

The internal system reset function is invoked either by asserting a hardware reset signal on pin RSTIN (Hardware Reset Input), by the execution of the SRST instruction (Software Reset) or by an overflow of the watchdog timer. Whenever one of these conditions occurs, the microcontroller is reset into its predefined default state. The following type of reset are implemented on the ST10R167:

Asynchronous hardware reset

Asynchronous reset does not require a stabilized clock signal on XTAL1, as it is not internally resynchronized. It immediately resets the microcontroller into its default reset state.

This asynchronous reset is required upon power-up of the chip and may be used during catastrophic situations. The rising edge of the RSTIN pin is internally resynchronized before exiting the reset condition. Therefore, only the entry of this hardware reset is asynchronous.

Synchronous hardware reset (warm reset)

A warm synchronous hardware reset is triggered when the reset input signal RSTIN is latched low and RPD (Pin 84) is high. The I/Os are immediately (asynchronously) set in high impedance, RSTOUT is driven low. After negation of RSTIN is detected, a short transition period elapses, during which pending internal hold states are cancelled and any current internal access cycles are completed, external bus cycles are aborted.

Then, the internal reset sequence starts for 1024 TCL (512 CPU clock cycles). During this reset sequence, if bit BDRSTEN was previously set by software (bit 5 in SYSCON register), RSTIN pin is driven low and internal reset signal is asserted to reset the microcontroller in its default state. Note that after all reset sequences, bit BDRSTEN is cleared.

After the reset sequence has been completed, the RSTIN input is sampled. If the reset input signal is active at that time the internal reset condition is prolonged until RSTIN becomes inactive.

Software reset

The reset sequence can be triggered at any time by the protected instruction SRST (software reset). This instruction can be executed deliberately within a program, e.g. to leave bootstrap loader mode, or on a hardware trap that reveals a system failure. As for a synchronous hardware reset, the reset sequence lasts 1024 TCL (512 CPU clock cycles), and drives the RSTIN pin low.

Watchdog timer reset

When the watchdog timer is not disabled during the initialization or serviced regularly during program execution it will overflow and trigger the reset sequence.

Unlike hardware and software resets, the watchdog reset completes a running external bus cycle if this bus cycle either does not use READY, or if READY is sampled active (low) after the programmed waitstates.

When READY is sampled inactive (high) after the programmed waitstates the running external bus cycle is aborted. The internal reset sequence is then started. The watchdog reset cannot occur while the ST10R167 is in bootstrap loader mode.

Bidirectional reset

This feature is enabled by bit 3 of the SYSCON register. The bidirectional reset makes the watchdog timer reset and software reset externally visible. It is active for the duration of an internal reset sequences caused by a watchdog timer reset and software reset.

This means that the bidirectional reset transforms an internal watchdog timer reset or software reset into an external hardware reset with a minimum duration of 1024 TCL. The consequence is that during a watchdog timer reset or software reset, the behavior of the ST10R167 is equal to an external hardware reset.

XIX - SPECIAL FUNCTION REGISTER OVERVIEW

Table 14 lists all SFRs which are implemented in the ST10R167 in alphabetical order.
Bit-addressable SFRs are marked with the letter “b” in column “Name”. SFRs within the Extended SFR-Space (ESFRs) are marked with the letter “E” in column “Physical Address”.

An SFR can be specified by its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Table 14 : Special function registers listed by name

Name	Physical address	8-bit address	Description	Reset value
ADCIC b	FF98h	CCh	A/D Converter End Of Conversion Interrupt Control Register	0000h
ADCON b	FFA0h	D0h	A/D Converter Control Register	0000h
ADDAT	FEA0h	50h	A/D Converter Result Register	0000h
ADDAT2	F0A0h **E**	50h	A/D Converter 2 Result Register	0000h
ADDRSEL1	FE18h	0Ch	Address Select Register 1	0000h
ADDRSEL2	FE1Ah	0Dh	Address Select Register 2	0000h
ADDRSEL3	FE1Ch	0Eh	Address Select Register 3	0000h
ADDRSEL4	FE1Eh	0Fh	Address Select Register 4	0000h
ADEIC b	FF9Ah	CDh	A/D Converter Overrun Error Interrupt Control Register	0000h
BUSCON0 b	FF0Ch	86h	Bus Configuration Register 0	0XX0h
BUSCON1 b	FF14h	8Ah	Bus Configuration Register 1	0000h
BUSCON2 b	FF16h	8Bh	Bus Configuration Register 2	0000h
BUSCON3 b	FF18h	8Ch	Bus Configuration Register 3	0000h
BUSCON4 b	FF1Ah	8Dh	Bus Configuration Register 4	0000h
CAPREL	FE4Ah	25h	GPT2 Capture/Reload Register	0000h
CC8IC b	FF88h	C4h	EX0IN Interrupt Control Register	0000h
CC0	FE80h	40h	CAPCOM Register 0	0000h
CC0IC b	FF78h	BCh	CAPCOM Register 0 Interrupt Control Register	0000h
CC1	FE82h	41h	CAPCOM Register 1	0000h
CC1IC b	FF7Ah	BDh	CAPCOM Register 1 Interrupt Control Register	0000h
CC2	FE84h	42h	CAPCOM Register 2	0000h
CC2IC b	FF7Ch	BEh	CAPCOM Register 2 Interrupt Control Register	0000h
CC3	FE86h	43h	CAPCOM Register 3	0000h
CC3IC b	FF7Eh	BFh	CAPCOM Register 3 Interrupt Control Register	0000h
CC4	FE88h	44h	CAPCOM Register 4	0000h
CC4IC b	FF80h	C0h	CAPCOM Register 4 Interrupt Control Register	0000h
CC5	FE8Ah	45h	CAPCOM Register 5	0000h
CC5IC b	FF82h	C1h	CAPCOM Register 5 Interrupt Control Register	0000h
CC6	FE8Ch	46h	CAPCOM Register 6	0000h
CC6IC b	FF84h	C2h	CAPCOM Register 6 Interrupt Control Register	0000h
CC7	FE8Eh	47h	CAPCOM Register 7	0000h
CC7IC b	FF86h	C3h	CAPCOM Register 7 Interrupt Control Register	0000h
CC8	FE90h	48h	CAPCOM Register 8	0000h

XX - ELECTRICAL CHARACTERISTICS (continued)

XX.3 - DC characteristics

V_{DD} = 5V ±10%, V_{SS} = 0V, f_{CPU} = 25MHz, Reset active, T_A = -40 to +125°C, unless otherwise specified.

Table 15 : DC characteristics

Symbol		Parameter	Test Conditions	Mininmum	Maximum	Unit
V_{IL}	**SR**	Input low voltage	–	– 0.5	0.2 V_{DD} – 0.1	V
V_{ILS}	**SR**	Input low voltage (special threshold)	–	– 0.5	2.0	V
V_{IH}	**SR**	Input high voltage (all except $\overline{RSTIN}$ and XTAL1)	–	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	**SR**	Input high voltage $\overline{RSTIN}$	–	0.6 V_{DD}	V_{DD} + 0.5	V
V_{IH2}	**SR**	Input high voltage XTAL1	–	0.7 V_{DD}	V_{DD} + 0.5	V
V_{IHS}	**SR**	Input high voltage (Special Threshold)	–	0.8 V_{DD} - 0.2	V_{DD}+ 0.5	V
HYS		Input Hysteresis (Special Threshold)	–	400	-	mV
V_{OL}	**CC**	Output low voltage (Port0, Port1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	I_{OL} = 2.4 mA	–	0.45	V
V_{OL1}	**CC**	Output low voltage (all other outputs)	I_{OL1} = 1.6 mA	–	0.45	V
V_{OH}	**CC**	Output high voltage (Port0, Port1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	I_{OH} = – 500 µA I_{OH} = –2.4 mA	0.9 V_{DD} 2.4	–	V
V_{OH1}	**CC**	Output high voltage [1] (all other outputs)	I_{OH} = – 250 µA I_{OH} = – 1.6 mA	0.9 V_{DD} 2.4	–	V V
I_{OZ1}	**CC**	Input leakage current (Port 5)	0 V < V_{IN} < V_{DD}	–	±0.5	µA
I_{OZ2}	**CC**	Input leakage current (all other)	0 V < V_{IN} < V_{DD}	–	±1	µA
I_{OV}	**SR**	Overload current	[5] [8]	–	±5	mA
R_{RST}	**CC**	$\overline{RSTIN}$ pull-up resistor [5]	–	50	250	kΩ
I_{RWH} [2]		Read/Write inactive current [4]	V_{OUT} = 2.4 V	–	-40	µA
I_{RWL} [3]		Read/Write active current [4]	V_{OUT} = V_{OLmax}	-500	–	µA
I_{ALEL} [2]		ALE inactive current [4]	V_{OUT} = V_{OLmax}	40	–	µA
I_{ALEH} [3]		ALE active current [4]	V_{OUT} = 2.4 V	–	500	µA
I_{P6H} [2]		Port 6 inactive current [4]	V_{OUT} = 2.4 V	–	-40	µA
I_{P6L} [3]		Port 6 active current [4]	V_{OUT} = V_{OL1max}	-500	–	µA
I_{P0H} [2]		Port0 configuration current [4]	V_{IN} = V_{IHmin}	–	-10	µA
I_{P0L} [3]			V_{IN} = V_{ILmax}	-100	–	µA
I_{IL}	**CC**	XTAL1 input current	0 V < V_{IN} < V_{DD}	–	±20	µA
C_{IO}	**CC**	Pin capacitance [5] (digital inputs/outputs)	f = 1 MHz T_A = 25 °C	–	10	pF
I_{CC}		Power supply current	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] [6]	20 + 6 * f_{CPU}	20 + 7 * f_{CPU}	mA
I_{ID}		Idle mode supply current	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] [6]	–	20 + 3 * f_{CPU}	mA
I_{PD}		Power-down mode supply current	V_{DD} = 5.5 V [7]	100	400	µA

XX - ELECTRICAL CHARACTERISTICS (continued)

Notes 1. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

2. The maximum current may be drawn while the respective signal line remains inactive.

3. The minimum current must be drawn in order to drive the respective signal line active.

4. This specification is only valid during Reset, or during Hold- or Adapt-mode. Port 6 pins are only affected if they are used as $\overline{CSx}$ output and the open drain function is not enabled.

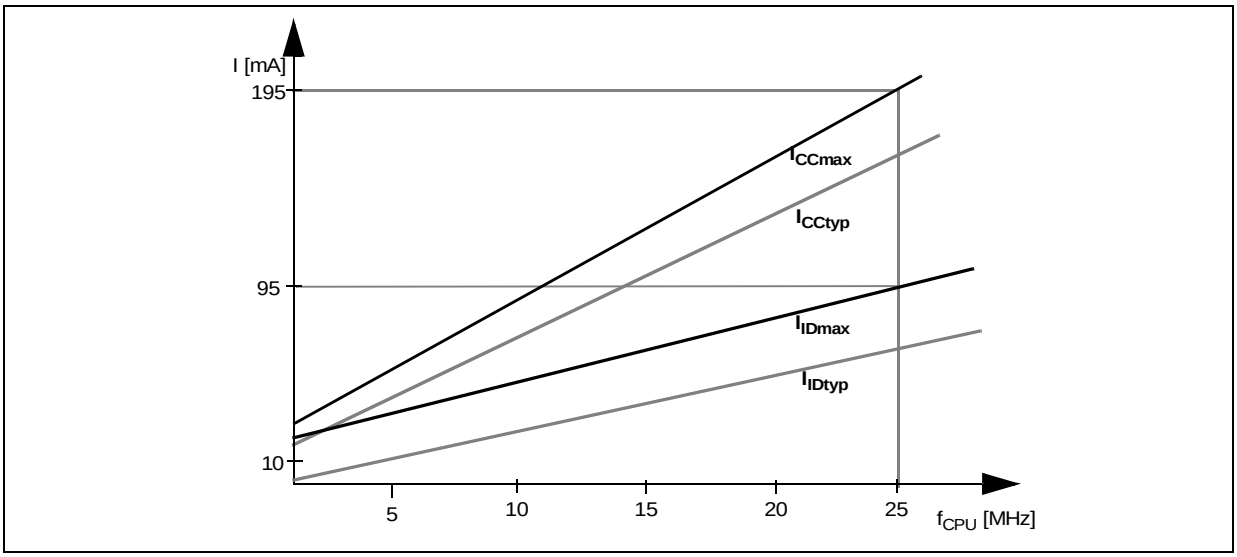
5. Partially tested, guaranteed by design characterization.

6. The supply current is a function of the operating frequency. This dependency is illustrated in the figure below. These parameters are tested at V_{DDmax} and 20MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

7. This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0V to 0.1V or at V_{DD} – 0.1V to V_{DD}, V_{REF} = 0V, all outputs (including pins configured as outputs) disconnected.

*8. Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$+0.5V or $V_{OV} < V_{SS}$-0.5V). The absolute sum of input overload currents on all port pins may not exceed **50mA** (see Figure 8).*

Figure 8 : Supply/idle current as a function of operating frequency



XX.3.1 - A/D converter characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40 to +125°C
4.0V ≤ V_{AREF} ≤ V_{DD} + 0.1V, V_{SS} - 0.1V ≤ V_{AGND} ≤ V_{SS} + 0.2V (see Table 16)

Table 16 : A/D converter characteristics

Symbol		Parameter	Test Conditions	Min.	Max.	Unit
V_{AIN}	**SR**	Analog input voltage range	1	V_{AGND}	V_{AREF}	V
t_S	**CC**	Sample time	2 4	–	2 t_{SC}	
t_C	**CC**	Conversion time	3 4	–	14 t_{CC} + t_S + 4TCL	
TUE	**CC**	Total unadjusted error	5	–	± 2	LSB
R_{AREF}	**SR**	Internal resistance of reference voltage source	t_{CC} in [ns] 6 7	–	t_{CC} /165 - 0.25	kΩ
R_{ASRC}	**SR**	Internal resistance of analog source	t_S in [ns] 2 7	–	t_S / 330 - 0.25	kΩ
C_{AIN}	**CC**	ADC input capacitance	7	–	33	pF

XX - ELECTRICAL CHARACTERISTICS (continued)

XX.4.1 - Definition of internal timing

The internal operation of the ST10C167 is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” periods (see Figure 11).

The CPU clock signal can be generated by different mechanisms. The duration of TCL periods and their variation (and also the derived external timing) depends on the mechanism used to generate f_{CPU}. This influence must be regarded when calculating the timings for the ST10C167.

The example for PLL operation shown in Figure 11 refers to a PLL factor of 4.

The mechanism used to generate the CPU clock is selected during reset by the logic levels on pins P0.15-13 (P0H.7-5).

XX.4.2 - Clock generation modes

Table 18 shows the association of the combinations of these three bits with the respective clock generation mode.

Figure 11 : Generation mechanisms for the CPU clock

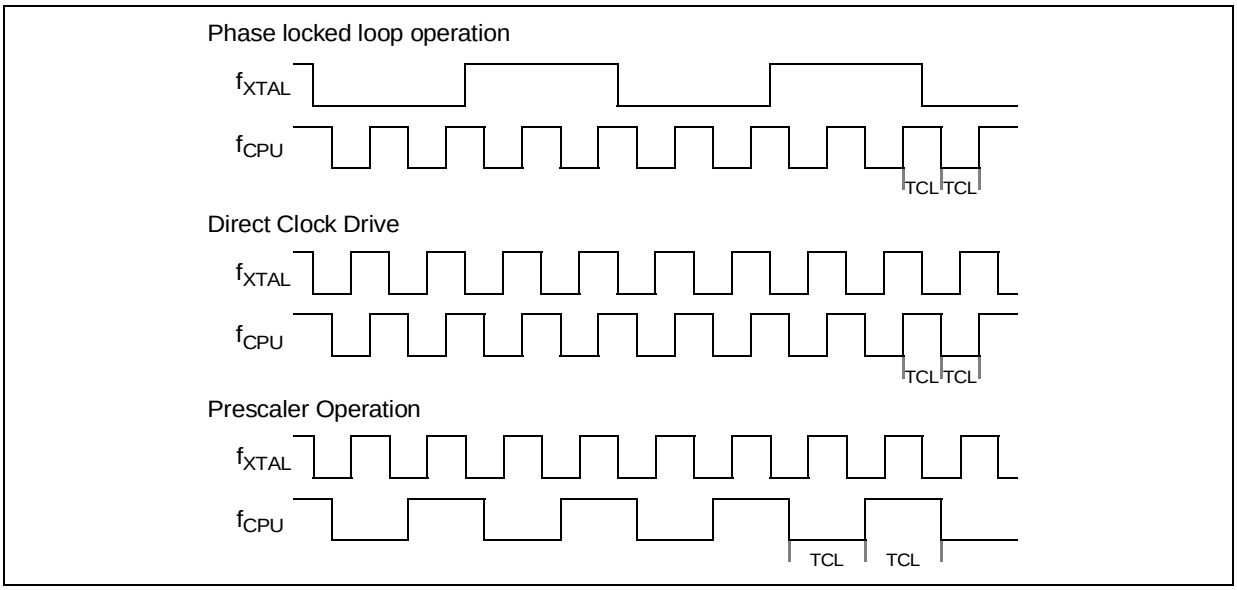


Table 17 : CPU Frequency Generation

P0.15-13 (P0H.7-5)			CPU Frequency $f_{CPU} = f_{XTAL} \times F$	External Clock Input Range [1]	Notes
1	1	1	F_{XTAL} x 4	2.5 to 6.25MHz	Default configuration
1	1	0	F_{XTAL} x 3	3.33 to 8.33MHz	
1	0	1	F_{XTAL} x 2	5 to 12.5MHz	
1	0	0	F_{XTAL} x 5	2 to 5MHz	
0	1	1	F_{XTAL} x 1	1 to 25MHz	Direct drive [2]
0	1	0	F_{XTAL} x 1.5	6.66 to 16.6MHz	
0	0	1	F_{XTAL} / 2	2 to 50MHz	CPU clock via prescaler
0	0	0	F_{XTAL} x 2.5	4 to 10MHz	

Notes 1. The external clock input range refers to a CPU clock range of 10...25MHz.

2. The maximum frequency depends on the duty cycle of the external clock signal.

XX - ELECTRICAL CHARACTERISTICS (continued)

XX.4.3 - Prescaler operation

When pins P0.15-13 (P0H.7-5) equal '001' during reset the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{XTAL} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{XTAL}.

The timings listed in the AC Characteristics that refer to TCLs, therefore, can be calculated using the period of f_{XTAL} for any TCL.

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL is running on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

XX.4.4 - Direct drive

When pins P0.15-13 (P0H.7-5) equal '011' during reset the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL}.

The timings listed below that refer to TCL therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated by the following formula:

$$TCL_{min} = 1/f_{XTAL} * DC_{min}$$

DC= duty cycle

For two consecutive TCLs the deviation caused by the duty cycle of f_{XTAL} is compensated so the duration of 2TCL is always $1/f_{XTAL}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula:

$$2TCL = 1/f_{XTAL}$$

Note The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL ($TCL_{max} = 1/f_{XTAL} \times DC_{max}$) instead of TCL_{min}.

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL is running on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

XX.4.5 - Oscillator watchdog (OWD)

When the clock option selected is direct drive or direct drive with prescaler, in order to provide a fail safe mechanism in case of a loss of the external clock, an oscillator watchdog is implemented as an additional functionality of the PLL circuitry. This oscillator watchdog operates as follows :

After a reset, the Oscillator Watchdog is enabled by default. To disable the OWD, the bit OWDDIS (bit 4 of SYSCON register) must be set.

When the OWD is enabled, the PLL is running on its free-running frequency, and increment the Oscillator Watchdog counter. On each transition of XTAL1 pin, the Oscillator Watchdog is cleared. If an external clock failure occurs, then the Oscillator Watchdog counter overflows (after 16 PLL clock cycles).

The CPU clock signal will be switched to the PLL free-running clock signal, and the Oscillator Watchdog Interrupt Request (XP3INT) is flagged. The CPU clock will not switch back to the external clock even if a valid external clock exits on XTAL1 pin. Only a hardware reset can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always fed from the oscillator input and the PLL is switched off to decrease power supply current.

XX.4.6 - Phase locked loop

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and provides the CPU clock (see table above). The PLL multiplies the input frequency by the factor F which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{XTAL} * F$). With every F'th transition of f_{XTAL} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{XTAL}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCL therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

XX - ELECTRICAL CHARACTERISTICS (continued)

Table 18 : Multiplexed bus characteristics (continued)

Symbol		Parameter	Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			Min.	Max.	Min.	Max.	
t_{10}[1]	**CC**	Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	–	6	–	6	ns
t_{11}[1]	**CC**	Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	–	26	–	TCL + 6	ns
t_{12}	**CC**	$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	30 + t_C	–	2TCL - 10 + t_C	–	ns
t_{13}	**CC**	$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	50 + t_C	–	3TCL - 10 + t_C	–	ns
t_{14}	**SR**	$\overline{RD}$ to valid data in (with RW-delay)	–	20 + t_C	–	2TCL - 20+ t_C	ns
t_{15}	**SR**	$\overline{RD}$ to valid data in (no RW-delay)	–	40 + t_C	–	3TCL - 20+ t_C	ns
t_{16}	**SR**	ALE low to valid data in	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
t_{17}	**SR**	Address/Unlatched $\overline{CS}$ to valid data in	–	50 + 2t_A + t_C	–	4TCL - 30 + 2t_A + t_C	ns
t_{18}	**SR**	Data hold after $\overline{RD}$ rising edge	0	–	0	–	ns
t_{19}[1]	**SR**	Data float after $\overline{RD}$	–	26 + t_F	–	2TCL - 14 + t_F	ns
t_{22}	**CC**	Data valid to $\overline{WR}$	20 + t_C	–	2TCL - 20 + t_C	–	ns
t_{23}	**CC**	Data hold after $\overline{WR}$	26 + t_F	–	2TCL - 14 + t_F	–	ns
t_{25}	**CC**	ALE rising edge after $\overline{RD}$, $\overline{WR}$	26 + t_F	–	2TCL - 14 + t_F	–	ns
t_{27}	**CC**	Address/Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	26 + t_F	–	2TCL - 14 + t_F	–	ns
t_{38}	**CC**	ALE falling edge to Latched $\overline{CS}$	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
t_{39}	**SR**	Latched $\overline{CS}$ low to valid data in	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C + 2t_A	ns
t_{40}	**CC**	Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	46 + t_F	–	3TCL - 14 + t_F	–	ns
t_{42}	**CC**	ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	16 + t_A	–	TCL - 4 + t_A	–	ns
t_{43}	**CC**	ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	-4 + t_A	–	-4 + t_A	–	ns
t_{44}[1]	**CC**	Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	–	0	–	0	ns
t_{45}[1]	**CC**	Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	–	20	–	TCL	ns
t_{46}	**SR**	$\overline{RdCS}$ to Valid Data In (with RW delay)	–	16 + t_C	–	2TCL - 24 + t_C	ns
t_{47}	**SR**	$\overline{RdCS}$ to Valid Data In (no RW delay)	–	36 + t_C	–	3TCL - 24 + t_C	ns

XX - ELECTRICAL CHARACTERISTICS (continued)

Table 18 : Multiplexed bus characteristics (continued)

Symbol		Parameter	Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			Min.	Max.	Min.	Max.	
t_{48}	**CC**	$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	30 + t_C	–	2TCL - 10 + t_C	–	ns
t_{49}	**CC**	$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	50 + t_C	–	3TCL - 10 + t_C	–	ns
t_{50}	**CC**	Data valid to $\overline{WrCS}$	26 + t_C	–	2TCL - 14+ t_C	–	ns
t_{51}	**SR**	Data hold after $\overline{RdCS}$	0	–	0	–	ns
t_{52}[1]	**SR**	Data float after $\overline{RdCS}$	–	20 + t_F	–	2TCL - 20 + t_F	ns
t_{54}	**CC**	Address hold after $\overline{RdCS}$, $\overline{WrCS}$	20 + t_F	–	2TCL - 20 + t_F	–	ns
t_{56}	**CC**	Data hold after $\overline{WrCS}$	20 + t_F	–	2TCL - 20 + t_F	–	ns

Note 1. Guaranteed by design characterization.

XX - ELECTRICAL CHARACTERISTICS (continued)

XX.4.10 - Demultiplexed bus

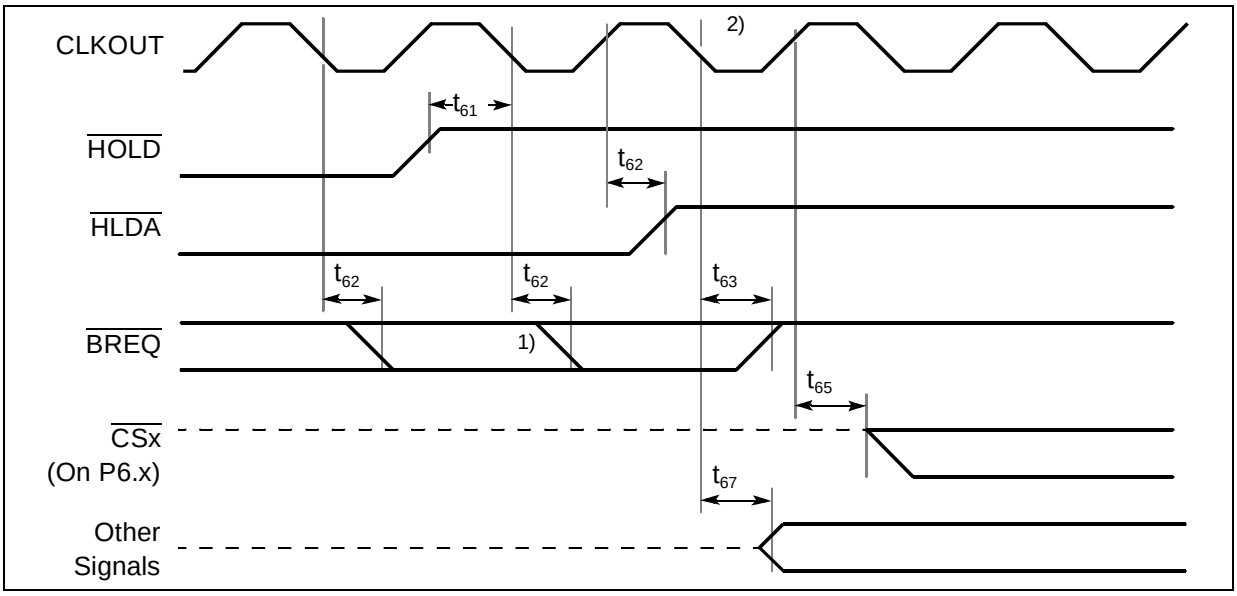
V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40 to +125°C
C_L (for Port0, Port1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100pF,
C_L (for Port 6, $\overline{CS}$) = 100pF
ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80ns at 25MHz CPU clock without wait states)

Table 19 : Demultiplexed bus characteristics

Symbol		Parameter	Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			Min.	Max.	Min.	Max.	
t_5	CC	ALE high time	10 + t_A	–	TCL - 10+ t_A	–	ns
t_6	CC	Address setup to ALE	4 + t_A	–	TCL - 16+ t_A	–	ns
t_8	CC	ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	10 + t_A	–	TCL - 10 + t_A	–	ns
t_9	CC	ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	-10 + t_A	–	-10 + t_A	–	ns
t_{12}	CC	$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	30 + t_C	–	2TCL - 10 + t_C	–	ns
t_{13}	CC	$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	50 + t_C	–	3TCL - 10 + t_C	–	ns
t_{14}	SR	$\overline{RD}$ to valid data in (with RW-delay)	–	20 + t_C	–	2TCL - 20 + t_C	ns
t_{15}	SR	$\overline{RD}$ to valid data in (no RW-delay)	–	40 + t_C	–	3TCL - 20 + t_C	ns
t_{16}	SR	ALE low to valid data in	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
t_{17}	SR	Address/Unlatched $\overline{CS}$ to valid data in	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
t_{18}	SR	Data hold after $\overline{RD}$ rising edge	0	–	0	–	ns
t_{20}[1]	SR	Data float after $\overline{RD}$ rising edge (with RW-delay[1])	–	26 + t_F	–	2TCL - 14 + t_F + $2t_A$[2]	ns
t_{21}[1]	SR	Data float after $\overline{RD}$ rising edge (no RW-delay[1])	–	10 + t_F	–	TCL - 10 + t_F + $2t_A$[2]	ns
t_{22}	CC	Data valid to $\overline{WR}$	20 + t_C	–	2TCL- 20 + t_C	–	ns
t_{24}	CC	Data hold after $\overline{WR}$	10 + t_F	–	TCL - 10+ t_F	–	ns
t_{26}	CC	ALE rising edge after $\overline{RD}$, $\overline{WR}$	-10 + t_F	–	-10 + t_F	–	ns
t_{28}	CC	Address/Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$ [2]	0 + t_F	–	0 + t_F	–	ns
t_{38}	CC	ALE falling edge to Latched $\overline{CS}$	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
t_{39}	SR	Latched $\overline{CS}$ low to Valid Data In	–	40 + t_C+ $2t_A$	–	3TCL - 20 + t_C + $2t_A$	ns
t_{41}	CC	Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	6 + t_F	–	TCL - 14 + t_F	–	ns
t_{42}	CC	ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	16 + t_A	–	TCL - 4 + t_A	–	ns

XX - ELECTRICAL CHARACTERISTICS (continued)

Figure 24 : External bus arbitration, (regaining the bus)



Notes 1. This is the last opportunity for BREQ to trigger the indicated regain-sequence. Even if BREQ is activated earlier, the regain-sequence is initiated by HOLD going high. Please note that HOLD may also be deactivated without the ST10C167 requesting the bus.
2. The next ST10C167 driven bus cycle may start here.