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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	15MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc802m001jdh16fp

Table 4. Pin description

Symbol	TSSOP20-1	TSSOP20-2	TSSOP16	HVQFN33	WLCSP16		Reset state[1]	Type	Description
V_{DD}	15	15	12	20	B4		-	-	If VDDIO is present, VDD is the supply voltage for the I/Os on the right side of the package and the core voltage regulator. If VDDIO is not present, VDD also supplies voltage to the I/Os on the left side of the package.
VDD_{IO}	-	2	-	-	-		-	-	If present, it is the supply voltage for the I/Os on the left side of the package.
V_{SS}	16	16	13	33[8]	C4		-	-	Ground.
VREFP	18	18	15	23	D4			A	**VREFP —** ADC positive reference voltage. Must be equal or lower than V_{DD}.
n.c.	-	-	-	10, 11, 12, 13, 14, 15, 21, 26, 27, 28, 29, 30, 31	-		-	-	no connect.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled; F = floating. For pin states in the different power modes, see Section 15.5 “Pin states in different power modes”. For termination on unused pins, see Section 15.4 “Termination of unused pins”.

[2] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[5] See Figure 16 for the reset pad configuration. This pin includes a 20 ns glitch filter (active in all power modes). $\overline{\text{RESET}}$ functionality is not available in deep power-down mode. Use the WAKEUP pins to reset the chip and wake up from deep power-down mode.

[6] The WKTCLKIN function is enabled in the PINENABLE0 register in the PMU. See the LPC802 user manual.

[7] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

[8] Thermal pad for HVQFN33.

9. Functional description

9.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 15 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

9.2 On-chip flash program memory

The LPC802 contain up to 16 KB of on-chip EEPROM based flash program memory.

9.3 On-chip SRAM

The LPC802 contain a total of 2 KB on-chip static RAM data memory.

9.4 On-chip ROM

The on-chip ROM contains the bootloader:

- Boot loader.
- Supports Flash In-Application Programming (IAP).
- Supports In-System Programming (ISP) through USART.
- On-chip ROM APIs for integer divide.
- Free Running Oscillator (FRO) API.

9.5 Memory map

The LPC802 incorporates several distinct memory regions. Figure 9 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

9.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, CTimer, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 5.

Functions that need specialized pads can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Section 7.2 “Pin description”. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

9.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC802 use accelerated GPIO functions:

- GPIO registers are on the ARM Cortex-M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 7 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and $\overline{\text{RESET}}$/PIO0_5, the switch matrix enables the GPIO port pin function by default.

9.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to GPIO inputs with internal pull-up resistors enabled after reset.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 10).
- Direction (input/output) can be set and cleared individually.
- Pin direction bits can be toggled.

9.11 Pin interrupt

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt. The registers that control the pin interrupt are on the IO+ bus for fast single-cycle access.

- Counter or timer operation.
- Up to three 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins can vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
  - Shadow registers are added for glitch-free PWM output.
- For each timer, up to 4 external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins can vary by device):
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Up to 4 match registers can be configured for PWM operation, allowing up to 3 single edged controlled PWM outputs. (The number of match outputs for each timer that are actually available on device pins can vary by device.)

9.16 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with two channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

9.16.1 Features

- 31-bit interrupt timer
- Two channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

9.17 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to service the watchdog timer periodically within a programmable time window.

9.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.

9.21 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

9.21.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
  - CRC-16: $x^{16} + x^{15} + x^2 + 1$
  - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1’s complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

9.22 Clocking and power control

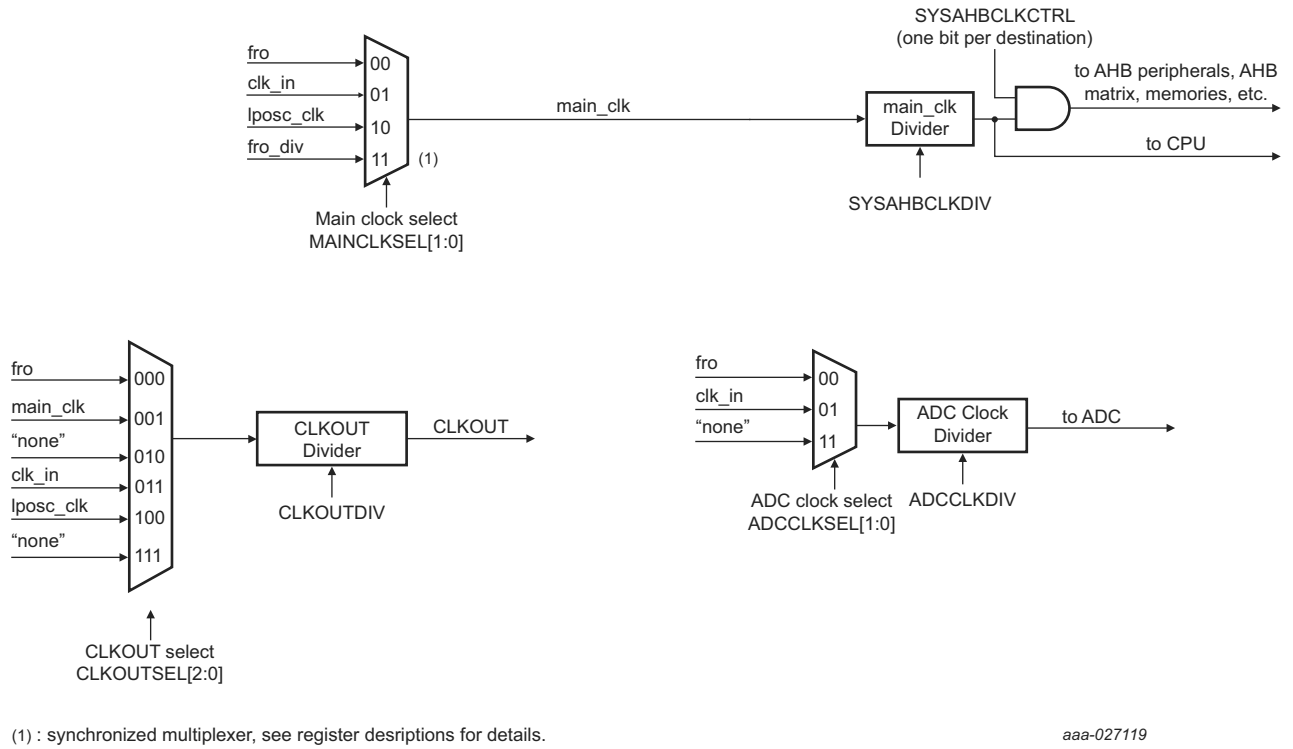


Fig 12. LPC802 clock generation

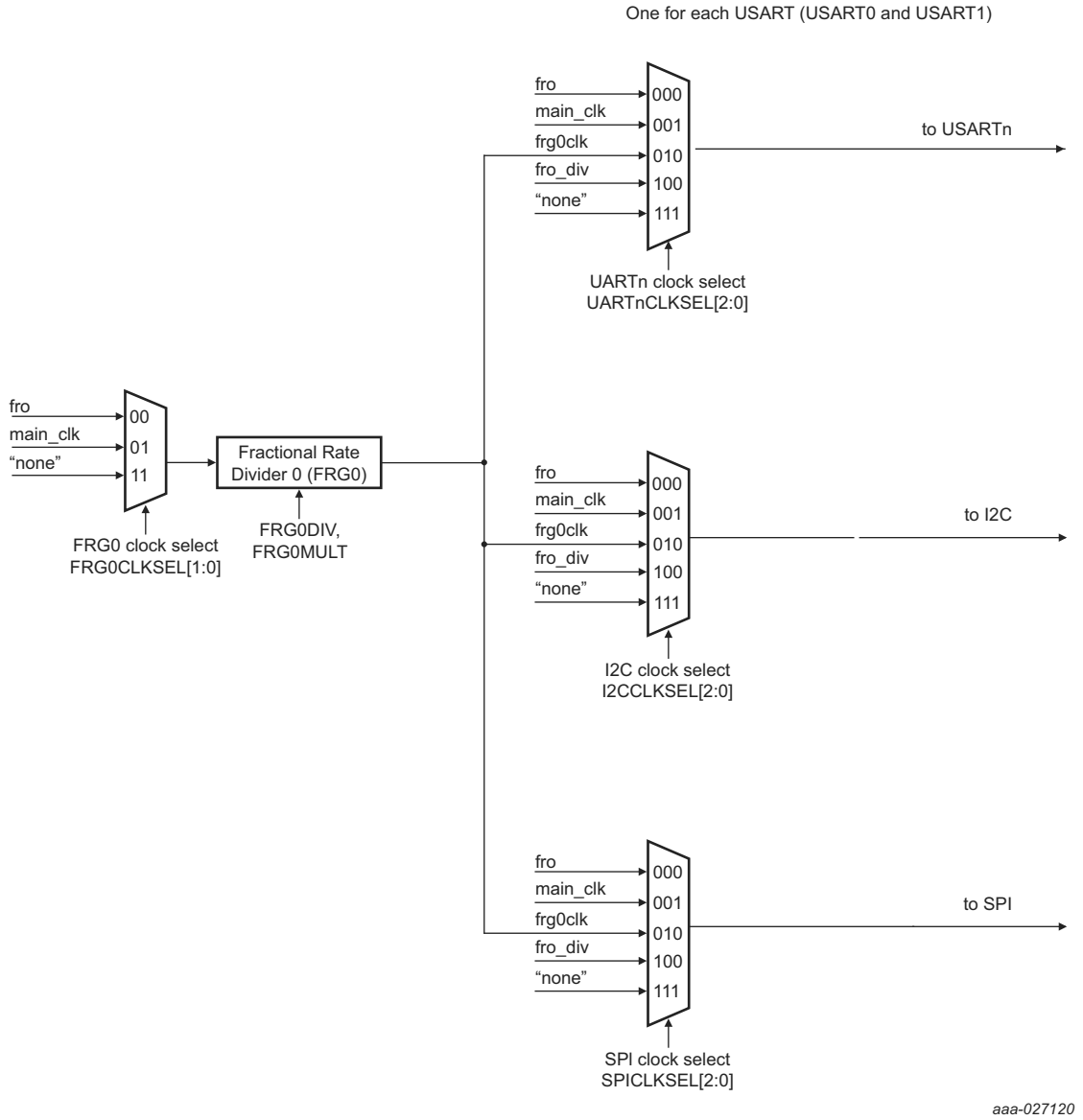


Fig 13. LPC802 clock generation (continued)

Power-down mode reduces power consumption compared to deep-sleep mode at the expense of longer wake-up times.

9.22.4.4 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the WAKEUP pins. The LPC802 can wake up from deep power-down mode via eight WAKEUP pins. See Section 9.18. Five general-purpose registers are available to store information during deep power-down mode.

The LPC802 can be prevented from entering deep power-down mode by setting a lock bit in the PMU block. Locking out deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

When entering deep power-down mode, an external pull-up resistor is required on the WAKEUP pins to hold it HIGH.

Table 7. Peripheral configuration in reduced power modes

Peripheral	Sleep mode	Deep-sleep mode	Power-down mode	Deep power-down mode
FRO	software configurable	on	off	off
FRO output	software configurable	off	off	off
Flash	software configurable	standby	off	off
BOD	software configurable	software configurable	software configurable	off
LPOsc/WWDT	software configurable	software configurable	software configurable	off
Digital peripherals	software configurable	off	off	off
Wake-up buffers	software configurable (cannot be used as wake-up source)	software configurable (cannot be used as wake-up source)	software configurable (cannot be used as wake-up source)	software configurable
ADC	software configurable	off	off	off

Table 12. Static characteristics, supply pins

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[9]	Unit
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash;					
		system clock = 1 MHz V_{DD} = 3.3 V	[3][5][6][10]	-	0.5	-	mA
		system clock = 9 MHz V_{DD} = 3.3 V	[3][4][5][6]	-	0.8	-	mA
		system clock = 12 MHz V_{DD} = 3.3 V	[3][4][5][6]	-	1.0	-	mA
		system clock = 15 MHz V_{DD} = 3.3 V	[3][4][5][6]	-	1.3	-	mA
		Sleep mode					
		system clock = 9 MHz V_{DD} = 3.3 V	[3][4][5][6]	-	0.4	-	mA
		system clock = 12 MHz V_{DD} = 3.3 V	[3][4][5][6]	-	0.5	-	mA
		system clock = 15 MHz V_{DD} = 3.3 V	[3][4][5][6]	-	0.6	-	mA
I_{DD}	supply current	Deep-sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[3][7]	-	100	175	µA
		T_{amb} = 105 °C		-	-	240	µA
I_{DD}	supply current	Power-down mode; V_{DD} = 3.3 V T_{amb} = 25 °C	[3][7]	-	6	14	µA
		T_{amb} = 105 °C		-	-	75	µA
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[8]	-	0.15	0.5	µA
		T_{amb} = 105 °C		-	-	7	µA

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), V_{DD} = 3.3 V.

[2] Characterized through bench measurements using typical samples.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] FRO enabled.

[5] BOD disabled.

[6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks disabled in system configuration block.

[7] All oscillators and analog blocks turned off.

[8] $\overline{\text{WAKEUP}}$ function pin pulled HIGH externally.

[9] Tested in production, VDD = 3.6 V.

[10] LPOsc enabled, FRO disabled.

12.2.1 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG. and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed. Measured on a typical sample at T_{amb} = 25 °C.

The supply currents are shown for system clock frequencies of 12 MHz and 15 MHz.

Table 13. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	15 MHz	
FRO	74	-	-	FRO = 12MHz. FRO output disabled.
BOD	39	-	-	Independent of main clock frequency.
Flash	80	-	-	-
LPOsc	1	-	-	FRO; independent of main clock frequency.
GPIO + pin interrupt	-	40	54	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	24	30	-
IOCON	-	28	36	-
CTimer	-	28	37	-
MRT	-	45	56	-
WWDT	-	31	41	-
I2C0	-	44	58	-
SPI0	-	33	42	-
USART0	-	39	46	-
USART1	-	40	50	-
Comparator ACMP	-	36	46	-
ADC	-	61	78	Digital controller only. Analog portion of the ADC disabled in the PDRUNCFG register.
	-	61	78	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 1 in the ADC CTRL register (ADC in low-power mode).
	-	61	78	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 0 in the ADC CTRL register (ADC powered).
CRC	-	37	50	-

12.3 Pin characteristics

Table 14. Static characteristics, electrical pin characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins configured as digital pins, RESET							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[2]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10[2]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq 1.71$ V; 5 V tolerant pins except PIO0_7		0	-	5.4	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		$V_{DD} - 0.4$	-	-	V
		I_{OH} = 3 mA; 1.71 V <= V_{DD} < 2.5 V		$V_{DD} - 0.5$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		-	-	0.5	V
		I_{OL} = 3 mA; 1.71 V <= V_{DD} < 2.5 V		-	-	0.5	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		$V_{OH} = V_{DD} - 0.5$ V; 1.71 V ≤ V_{DD} ≤ 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.71 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[3]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[3]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[4]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V	[4]	10	50	90	µA
		1.71 V ≤ V_{DD} < 2.0 V		7	50	85	µA
		$V_{DD} < V_I < 5$ V		0	0	0	µA
High-drive output pin configured as digital pin (PIO0_2, PIO0_3, and PIO0_12)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[2]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10[2]	nA

Table 14. Static characteristics, electrical pin characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V		0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 20 mA; 2.5 V <= V_{DD} < 3.6 V		V_{DD} − 0.6	-	-	V
		I_{OH} = 12 mA; 1.71 V <= V_{DD} < 2.5 V		V_{DD} − 0.6	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V I_{OL} = 3 mA; 1.71 V <= V_{DD} < 2.5 V		-	-	0.5	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.6 V; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		V_{OH} = V_{DD} − 0.6 V; 1.71 V <= V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.71 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[3]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[4]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V;	[4]				μA
		2.0 V ≤ V_{DD} ≤ 3.6 V		10	50	90	μA
		1.71 V ≤ V_{DD} < 2.0 V		7	50	85	μA
		V_{DD} < V_I < 5 V		0	0	0	μA

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Based on characterization. Not tested in production.

[3] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[4] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 20.

13. Dynamic characteristics

13.1 Flash memory (EEPROM based)

Table 15. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	200,000	500,000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		not powered		20	-	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors		-	1.03	-	ms
t_{prog}	programming time		[2]	-	2.5	-	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 64 bytes to the flash. T_{amb} <= +85 °C. Flash programming with IAP calls (see *LPC802 user manual*).

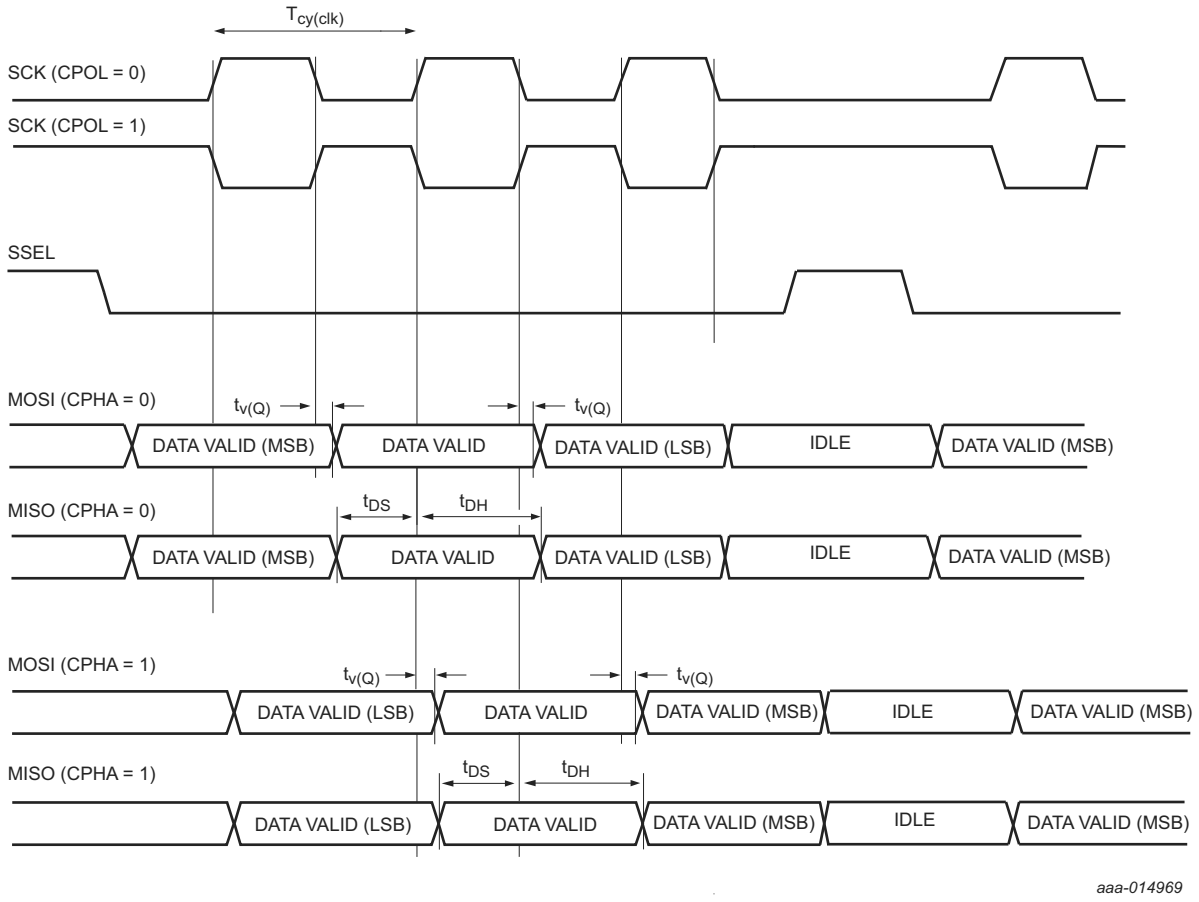
13.2 FRO

Table 16. Dynamic characteristic: FRO

T_{amb} = −40 °C to +105 °C; 1.7 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Min	Typ[1]	Max	Unit
FRO clock frequency; Condition: 0 °C ≤ T_{amb} ≤ 70 °C				
$f_{osc(RC)}$	9 -1 %	9	9 +1 %	MHz
$f_{osc(RC)}$	12 -1 %	12	12 +1 %	MHz
$f_{osc(RC)}$	15 -1 %	15	15 +1 %	MHz
FRO clock frequency; Condition: −20 °C ≤ T_{amb} ≤ 70 °C				
$f_{osc(RC)}$	9 -2 %	9	9 +1 %	MHz
$f_{osc(RC)}$	12 -2 %	12	12 +1 %	MHz
$f_{osc(RC)}$	15 -2 %	15	15 +1 %	MHz
FRO clock frequency; Condition: −40 °C ≤ T_{amb} ≤ 105 °C				
$f_{osc(RC)}$	9 -3.5 %	9	9 +2.5 %	MHz
$f_{osc(RC)}$	12 -3.5 %	12	12 +2.5 %	MHz
$f_{osc(RC)}$	15 -3.5 %	15	15 +2.5 %	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



$T_{cy(clk)}$ = CCLK/DIVVAL with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the LPC802 *User manual*.

Fig 27. SPI master timing

14.2.1 ADC input impedance

Figure 31 shows the ADC input impedance. In this figure:

- ADCx represents ADC input channel 0.
- ADCy represents ADC input channels 1 to 11.
- R_1 and R_{sw} are the switch-on resistance on the ADC input channel.
- If ADC input channel 0 is selected, the ADC input signal goes through $R_1 + R_{sw}$ to the sampling capacitor (C_{ia}).
- If ADC input channels 1 to 11 are selected, the ADC input signal goes through R_{sw} to the sampling capacitor (C_{ia}).
- Typical values, R_1 = 5.6 kΩ, R_{sw} = 6.9 kΩ
- To calculate total resistance, use the following equation:
  - $R_{TOTAL} = R_{external} + R_{internal}$
  - $R_{external}$ = External resistance on the ADC input channel.
  - $R_{internal}$ for channel 0 = $R_1 + R_{SW}$ = 12.5 kΩ.
  - $R_{internal}$ for channels 1 to 11 = 6.9 kΩ.
- See Table 11 for C_{io}.
- See Table 25 for C_{ia}.

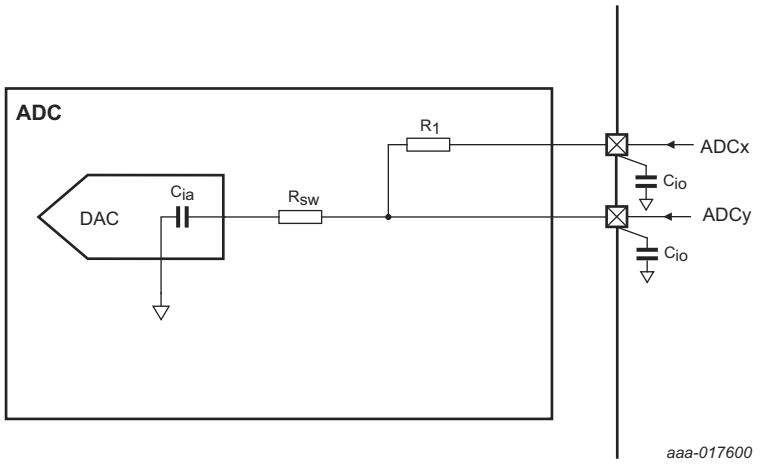
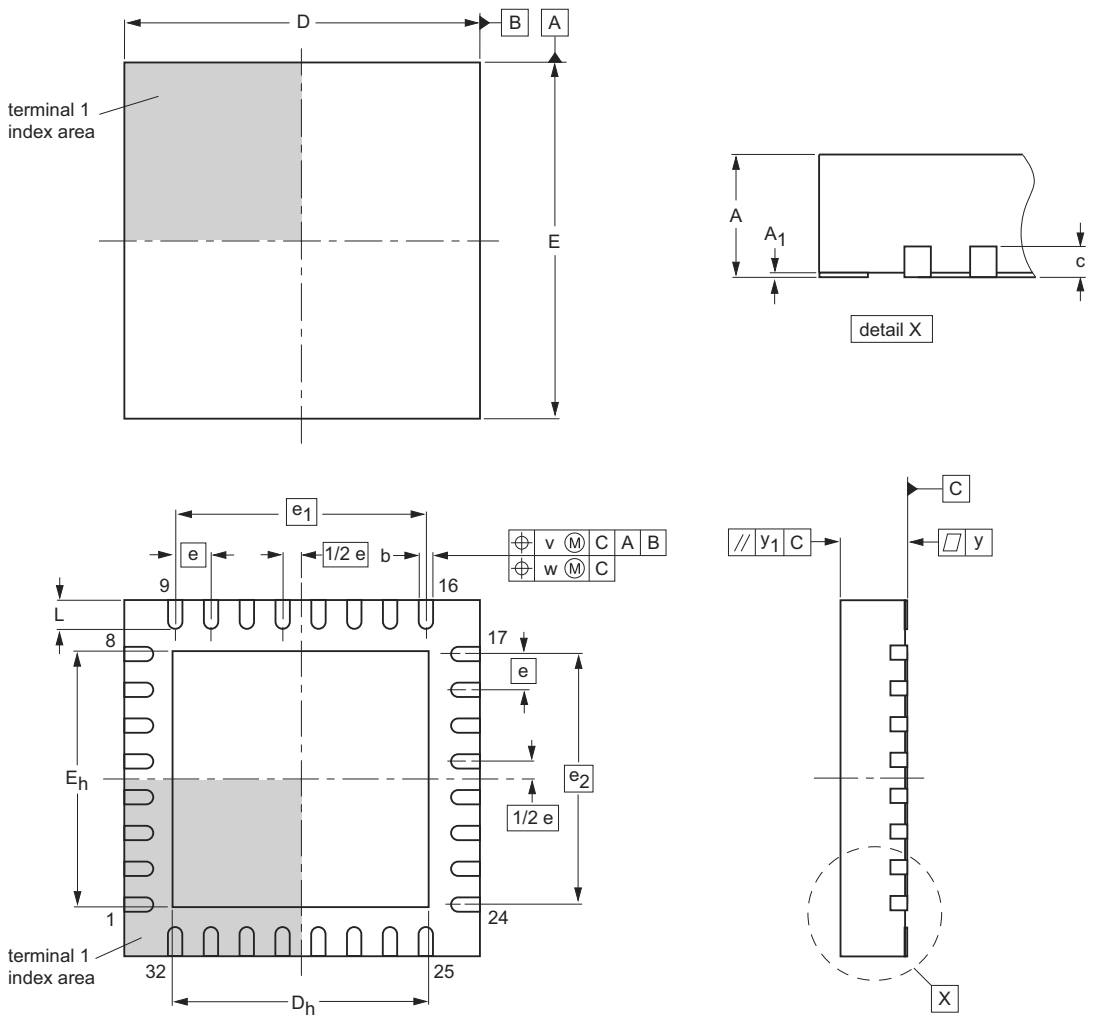


Fig 31. ADC input impedance

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

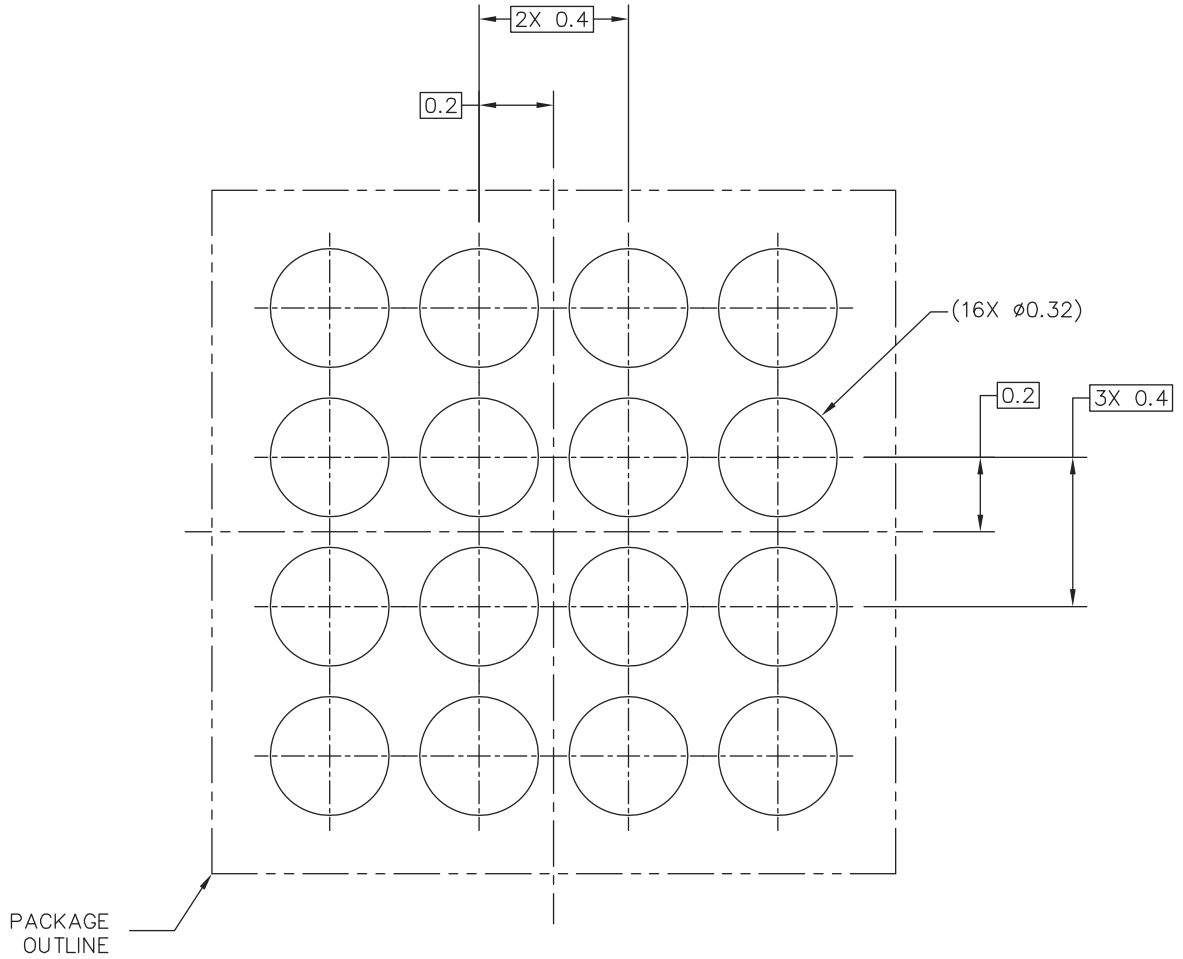
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 37. Package outline HVQFN33 (5 x 5 x 0.85 mm)



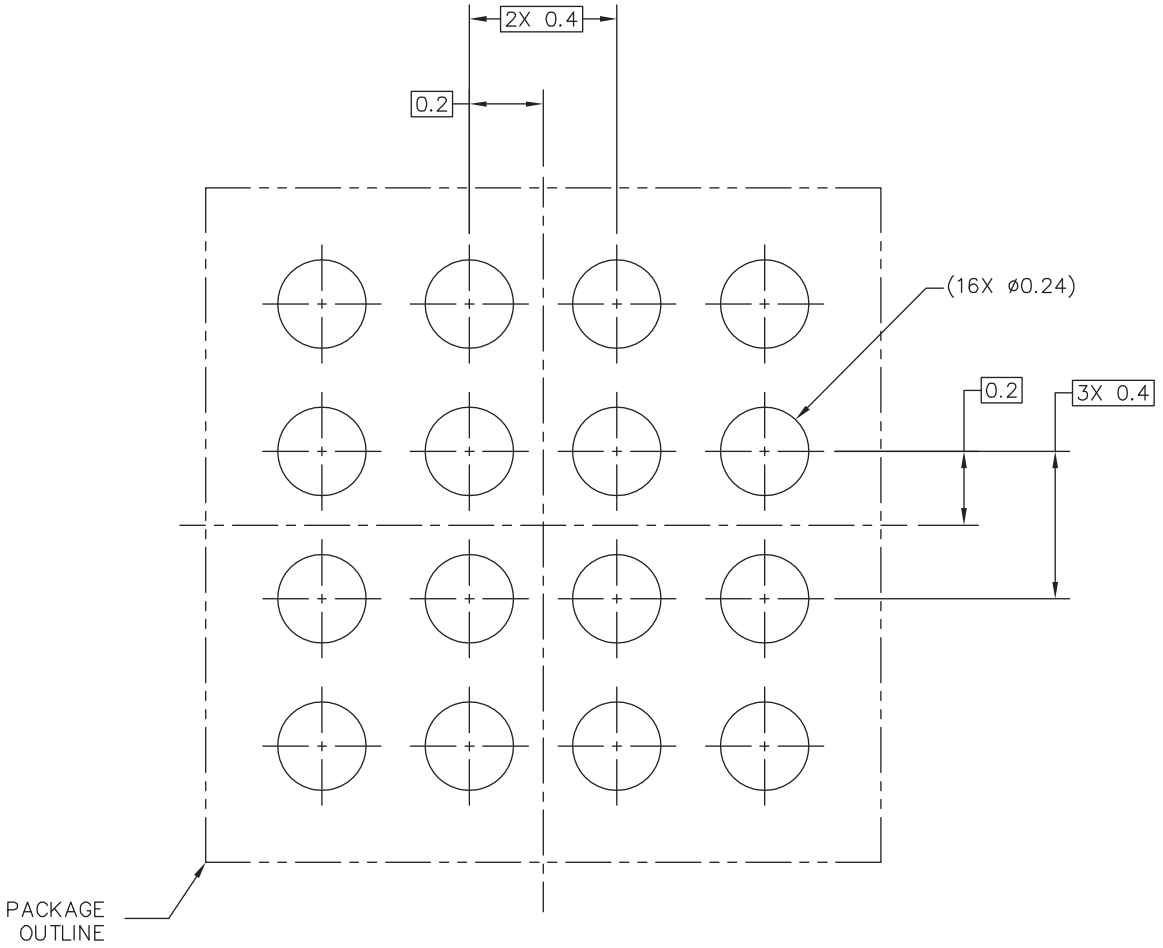
PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

 DATE: 09 FEB 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1393–2	REVISION: O	

Fig 42. Reflow soldering for the WLCSP16 (4x4) package (1 of 3)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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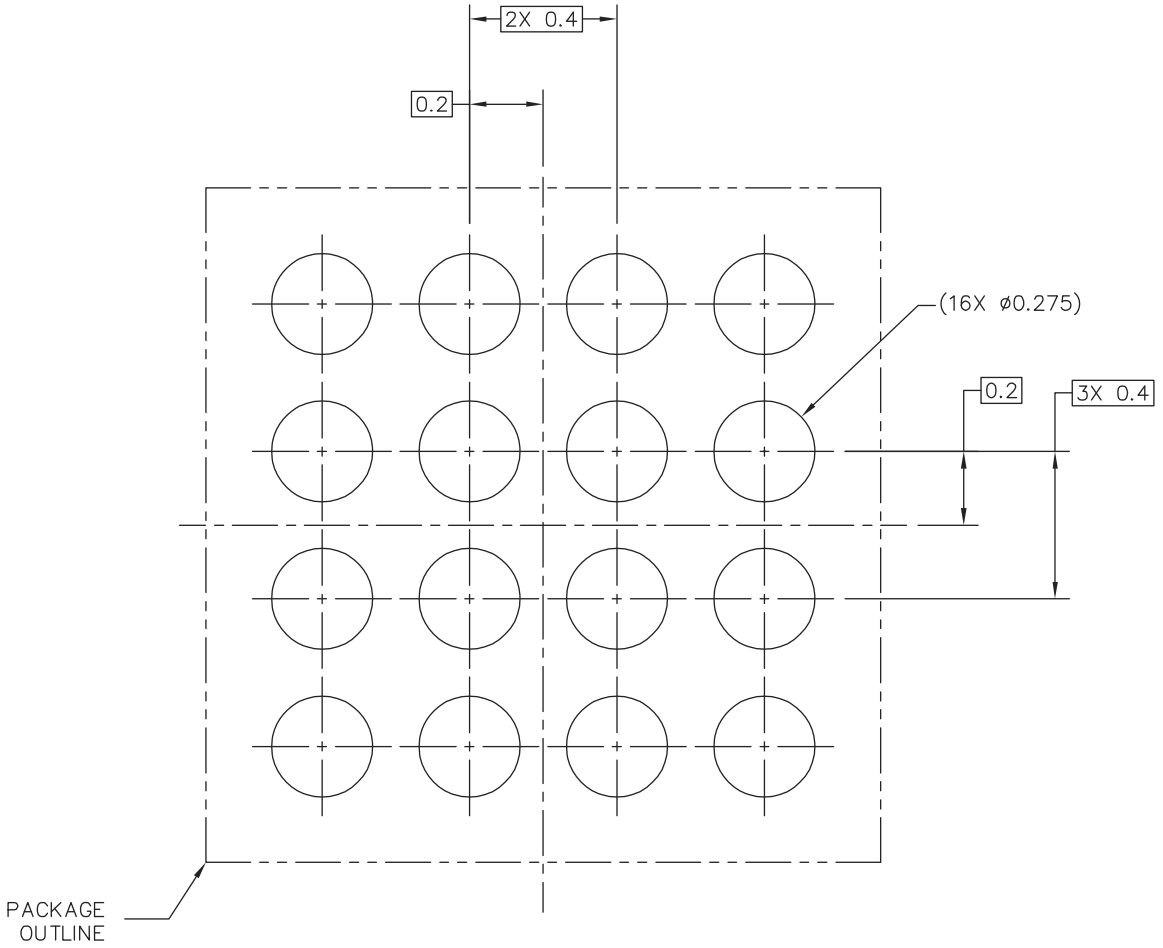
 DATE: 09 FEB 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1393-2	REVISION: O	

Fig 43. Reflow soldering for the WLCSP16 (4x4) package (2 of 3)



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

 DATE: 09 FEB 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1393–2	REVISION: 0	

Fig 44. Reflow soldering for the WLCSP16 (4x4) package (3 of 3)

20. Revision history

Table 34. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC802 v.1.6	20180427	Product data sheet	-	LPC802 v.1.5
Modifications:	• Added LPC802UK part. • Added text to Section 9.22.4.4 “Deep power-down mode”: Five general-purpose registers are available to store information during deep power-down mode. • Updated Section 9.22.1 “Internal oscillators”. Changed heading title. • Updated Section 15.2 “Connecting power, clocks, and debug functions”: removed text: connect the external crystal.			
LPC802 v.1.5	20180312	Product data sheet	-	LPC802 v.1.4
Modifications:	• Updated Table 3 “Device revision table”.			
LPC802 v.1.4	20180227	Product data sheet	-	LPC802 v.1.3
Modifications:	• Added Figure 38 “Package outline WLCSP16 (1.86 ´1.86 ´ 0.3 mm)”. • Added Figure 42 “Reflow soldering for the WLCSP16 (4x4) package (1 of 3)”, Figure 43 “Reflow soldering for the WLCSP16 (4x4) package (2 of 3)”, and Figure 44 “Reflow soldering for the WLCSP16 (4x4) package (3 of 3)”. • Updated title of Section 13.1 “Flash memory (EEPROM based)”. • Updated Table 12 “Static characteristics, supply pins”: Added condition: system clock = 1 MHz, VDD = 3.3 V. • Updated Table 16 “Dynamic characteristic: FRO”: Max values: FRO clock frequency; Condition: −20 °C ≤ T_{amb} ≤ 70 °C and FRO clock frequency; Condition: −40 °C ≤ T_{amb} ≤ 105 °C.			
LPC802 v.1.3	20180209	Product data sheet	-	LPC802 v.1.2
Modifications:	• Updated Section 2 “Features and benefits”. • Updated Table 5 “Movable functions (assign to pins PIO0_0 to PIO0_5, PIO0_7 to PIO0_17 through switch matrix)”. • Added level shifter functionality to Section 9.8 “I/O configuration”. • Updated Table 16 “Dynamic characteristic: FRO”: Changed frequencies to 9 MHz, 12 MHz, and 15 MHz. Added Condition: −20 °C ≤ T_{amb} ≤ 70 °C and Condition: −40 °C ≤ T_{amb} ≤ 70 °C.			
LPC802 v.1.2	20171222	Product data sheet	-	LPC802 v.1.1
Modifications:	• Updated Figure 4 “LPC802 block diagram”. • Updated Figure 12 “LPC802 clock generation”. • Updated Table 7 “Peripheral configuration in reduced power modes”: In deep-sleep mode flash is on standby.			
LPC802 v.1.1	20171222	Product data sheet	-	LPC802 v.1
Modifications:	• Updated Figure 21 “High-drive output: Typical HIGH-level output voltage VOH versus HIGH-level output current IOH” at 1.8 V.			
LPC802 v.1	20171218	Product data sheet	-	-