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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	15MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc802m001jdh20fp

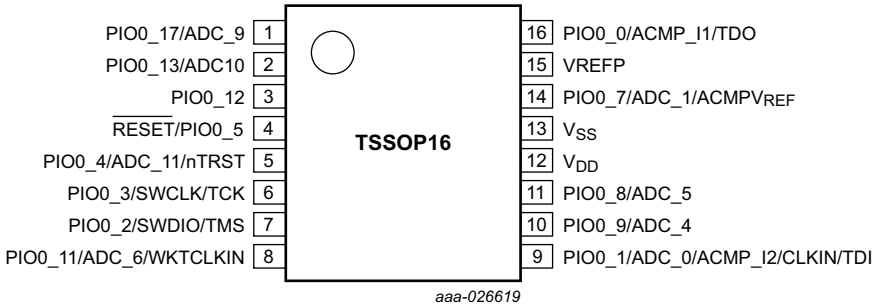


Fig 7. Pin configuration TSSOP16 package

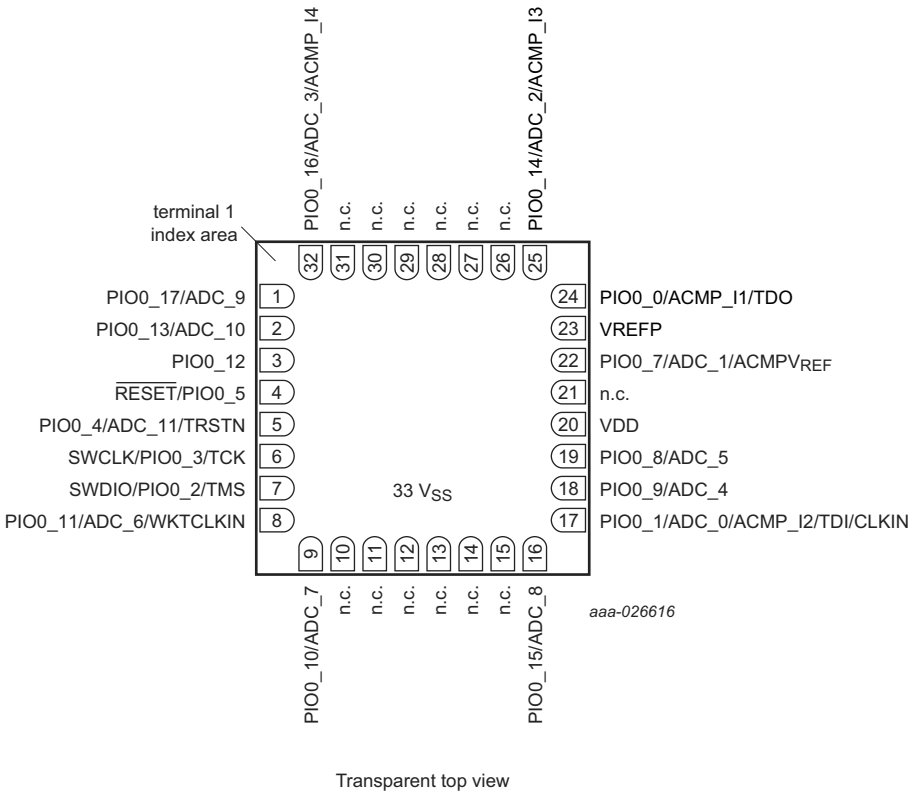


Fig 8. Pin configuration HVQFN33 package

7.2 Pin description

Table 4 shows the pin functions that are fixed to specific pins on each package. These fixed-pin functions are selectable through the switch matrix between GPIO and the comparator, ADC, SWD, and RESET pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable functions for the I2C, USART, SPI, CTimer pins and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, an output and/or one or more inputs can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Eight GPIO pins trigger a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via an external pin, do not assign any movable function to this pin. The GPIO pins should be pulled HIGH externally before entering deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit deep power-down mode and wakes up the part.

The JTAG functions TDO, TDI, TCK, TMS, and TRST are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

PIO0_2, PIO0_3, and PIO0_12 are the high drive output pins. PIO0_4, PIO0_8, PIO0_9, PIO0_10, PIO0_11, PIO0_13, PIO0_15, and PIO0_17 are the WAKEUP pins.

8. Movable functions

Movable functions for the I2C, USART, SPI, CTimer pins and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the fixed functions of the pin.

Table 5. Movable functions (assign to pins PIO0_0 to PIO0_5, PIO0_7 to PIO0_17 through switch matrix)

Function name	Type	Description
Ux_TXD	O	Transmitter output for USART0 to USART1.
Ux_RXD	I	Receiver input for USART0 to USART1.
$\overline{\text{Ux\_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{Ux\_CTS}}$	I	Clear To Send input for USART0.
Ux_SCLK	I/O	Serial clock input/output for USART0 to USART1 in synchronous mode.
SPIx_SCK	I/O	Serial clock for SPI0.
SPIx_MOSI	I/O	Master Out Slave In for SPI0.
SPIx_MISO	I/O	Master In Slave Out for SPI0.
SPIx_SSEL0	I/O	Slave select 0 for SPI0.
SPIx_SSEL1	I/O	Slave select 1 for SPI0.
I2Cx_SDA	I/O	I^2C0 bus data input/output.
I2Cx_SCL	I/O	I^2C0 bus clock input/output.
ACMP_O	O	Analog comparator output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.
T0_MAT0	O	Timer Match channel 0.
T0_MAT1	O	Timer Match channel 1.
T0_MAT2	O	Timer Match channel 2.
T0_MAT3	O	Timer Match channel 3.
T0_CAP0	I	Timer Capture channel 0.
T0_CAP1	I	Timer Capture channel 1.
T0_CAP2	I	Timer Capture channel 2.
LVLSHFT_IN0	I	Level shift input 0.
LVLSHFT_IN1	I	Level shift input 1.
LVLSHFT_OUT0	O	Level shift output 0.
LVLSHFT_OUT1	O	Level shift output 1.

9. Functional description

9.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 15 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

9.2 On-chip flash program memory

The LPC802 contain up to 16 KB of on-chip EEPROM based flash program memory.

9.3 On-chip SRAM

The LPC802 contain a total of 2 KB on-chip static RAM data memory.

9.4 On-chip ROM

The on-chip ROM contains the bootloader:

- Boot loader.
- Supports Flash In-Application Programming (IAP).
- Supports In-System Programming (ISP) through USART.
- On-chip ROM APIs for integer divide.
- Free Running Oscillator (FRO) API.

9.5 Memory map

The LPC802 incorporates several distinct memory regions. Figure 9 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

- Counter or timer operation.
- Up to three 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins can vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
  - Shadow registers are added for glitch-free PWM output.
- For each timer, up to 4 external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins can vary by device):
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Up to 4 match registers can be configured for PWM operation, allowing up to 3 single edged controlled PWM outputs. (The number of match outputs for each timer that are actually available on device pins can vary by device.)

9.16 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with two channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

9.16.1 Features

- 31-bit interrupt timer
- Two channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

9.17 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to service the watchdog timer periodically within a programmable time window.

9.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.

- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) is generated by the dedicated watchdog oscillator (WDOSC).

9.18 Self-Wake-up Timer (WKT)

The self-wake-up timer is a 32-bit, loadable down counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur prior to entering a reduced power mode.

9.18.1 Features

- 32-bit loadable down counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT supports three clock sources: an external clock on the WKTCLKIN pin, the low-power oscillator, and the FRO. The low-power oscillator can be used as the clock source in sleep, deep-sleep, and power-down modes.
- The WKT can be used for waking up the part from any reduced power mode or for general-purpose timing.

9.19 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 27.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled through the switch matrix.

9.22 Clocking and power control

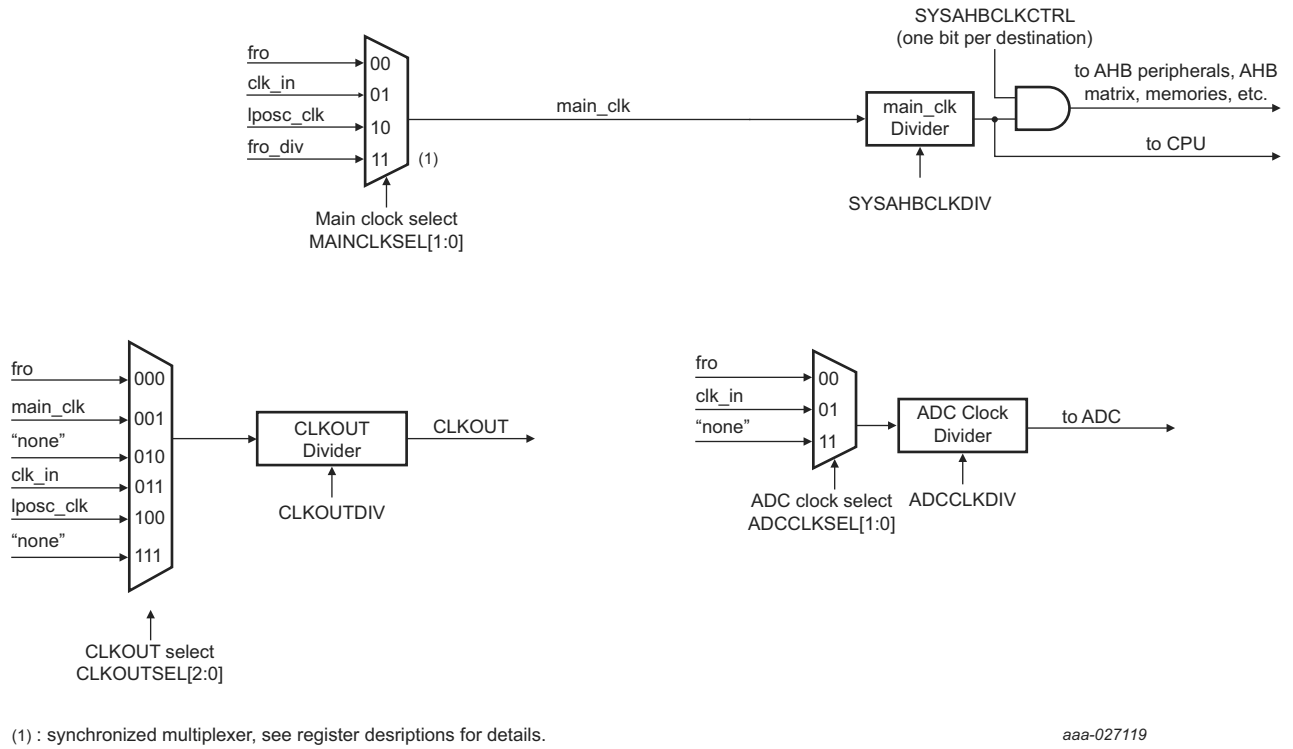


Fig 12. LPC802 clock generation

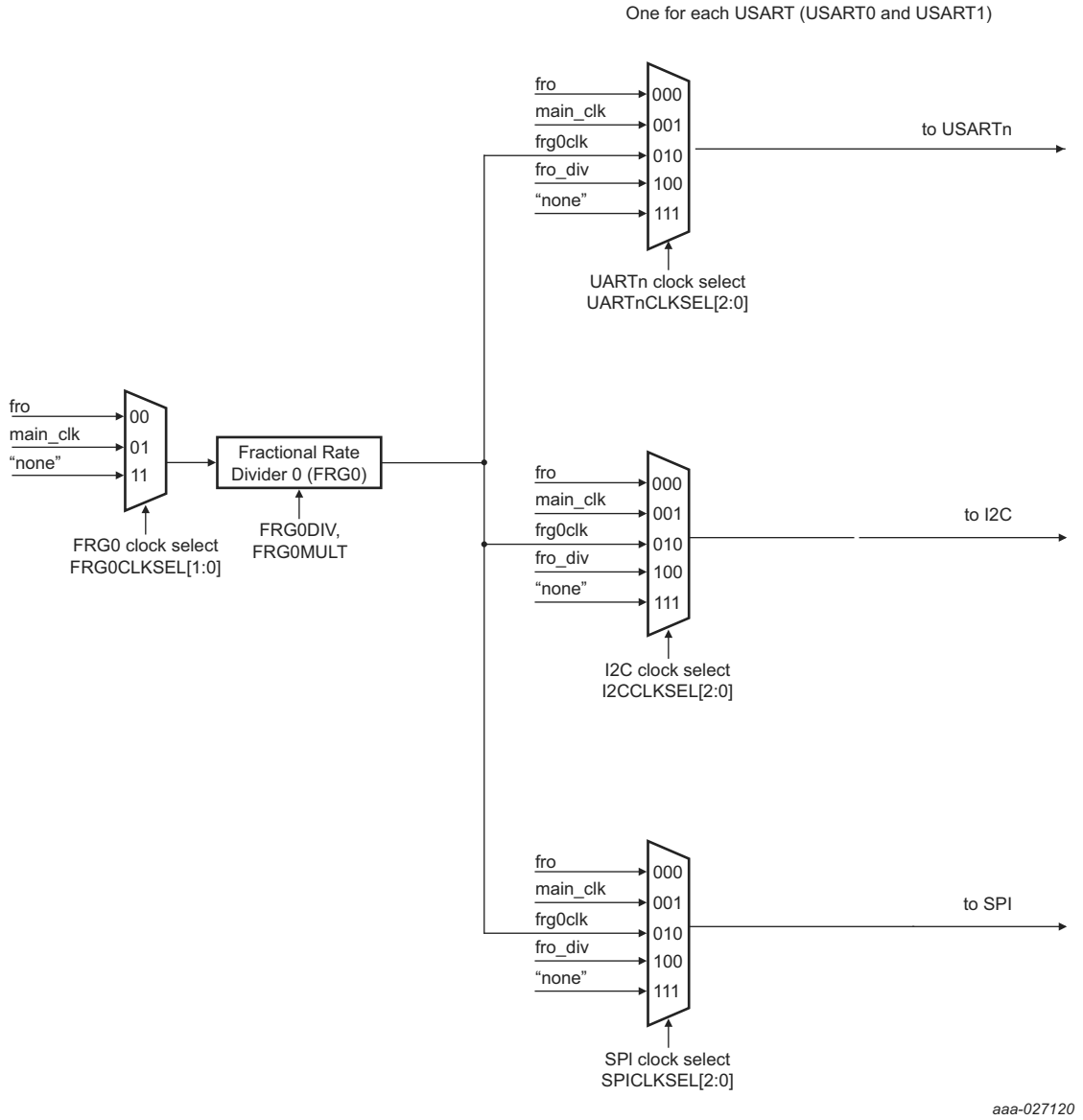


Fig 13. LPC802 clock generation (continued)

9.22.4 Power control

The LPC802 supports the ARM Cortex-M0+ sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing to fine-tune power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

9.22.4.1 Sleep mode

When sleep mode is entered, the clock to the core is stopped. Resumption from the sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

9.22.4.2 Deep-sleep mode

In deep-sleep mode, the LPC802 core is in sleep mode and all peripheral clocks and all clock sources are off except for the FRO or low-power oscillator if selected. The FRO output is disabled. In addition, all analog blocks are shut down and the flash is in standby mode. In deep-sleep mode, the application can keep the low power oscillator and the BOD circuit running for self-timed wakeup and BOD protection.

The LPC802 can wake up from deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI (in slave mode), or the I2C blocks (in slave mode).

Any interrupt used for waking up from deep-sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Deep-sleep mode saves power and allows for short wake-up times.

9.22.4.3 Power-down mode

In power-down mode, the LPC802 is in sleep mode and all peripheral clocks and all clock sources are off except for low-power oscillator if selected. In addition, all analog blocks and the flash are shut down. In power-down mode, the application can keep the low-power oscillator and the BOD circuit running for self-timed wake up and BOD protection.

The LPC802 can wake up from power-down mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI (in slave mode), or the I2C blocks (in slave mode).

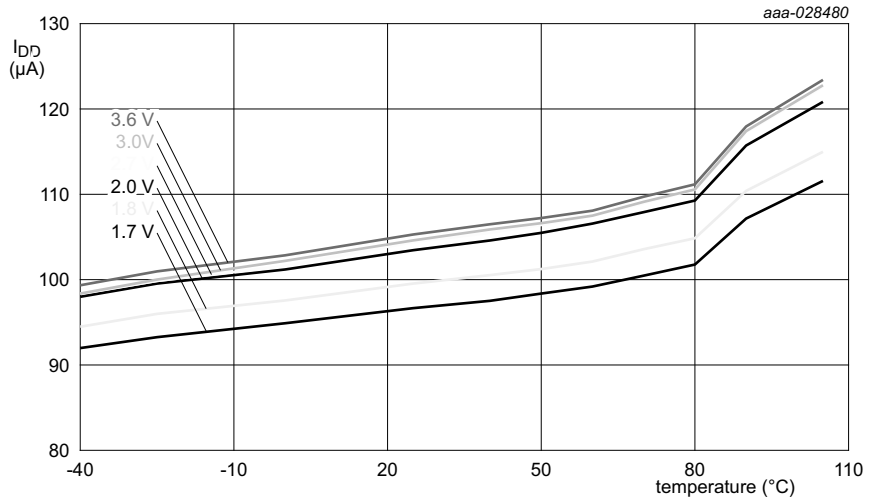
Any interrupt used for waking up from power-down mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

10. Limiting values

Table 9. Limiting values

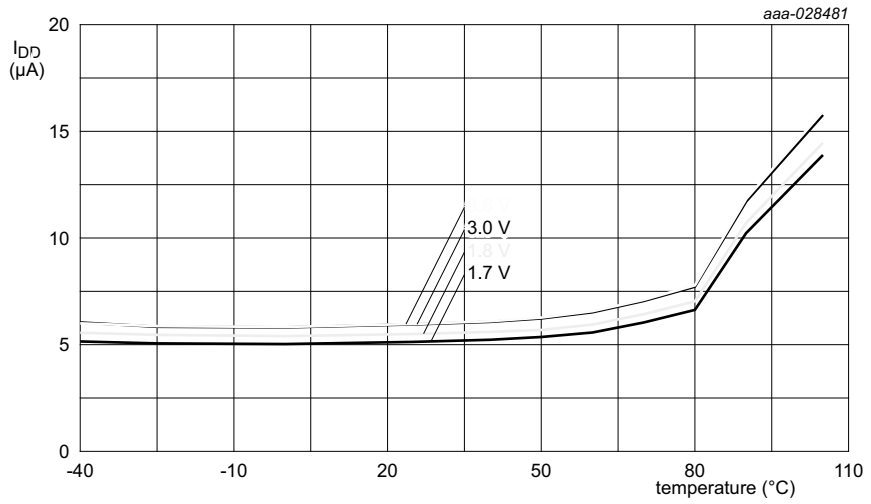
In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	−0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP		−0.5	V_{DD}	V
V_I	input voltage	5 V tolerant I/O pins; $V_{DD} \geq 1.71$ V	[3][4]	−0.5	+5.4	V
		3 V tolerant I/O pin ACMPV_{REF}	[5]	−0.5	+3.6	V
V_{IA}	analog input voltage	on digital pins configured for an analog function	[6][7][8]	−0.5	+4.6	V
I_{DD}	supply current	per supply pin (TSSOP20)		-	40	mA
		per supply pin (TSSOP16)		-	30	
		per supply pin (HVQFN33)		-	50	
		per supply pin (WLCSP16)		-	30	
I_{SS}	ground current	per ground pin (TSSOP20)		-	40	mA
		per ground pin (TSSOP16)		-	30	
		per ground pin (HVQFN33)		-	50	
		per supply pin (WLCSP16)		-	30	
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[9]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register.

Fig 17. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register.

Fig 18. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

12.2.1 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG. and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed. Measured on a typical sample at T_{amb} = 25 °C.

The supply currents are shown for system clock frequencies of 12 MHz and 15 MHz.

Table 13. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	15 MHz	
FRO	74	-	-	FRO = 12MHz. FRO output disabled.
BOD	39	-	-	Independent of main clock frequency.
Flash	80	-	-	-
LPOsc	1	-	-	FRO; independent of main clock frequency.
GPIO + pin interrupt	-	40	54	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	24	30	-
IOCON	-	28	36	-
CTimer	-	28	37	-
MRT	-	45	56	-
WWDT	-	31	41	-
I2C0	-	44	58	-
SPI0	-	33	42	-
USART0	-	39	46	-
USART1	-	40	50	-
Comparator ACMP	-	36	46	-
ADC	-	61	78	Digital controller only. Analog portion of the ADC disabled in the PDRUNCFG register.
	-	61	78	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 1 in the ADC CTRL register (ADC in low-power mode).
	-	61	78	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 0 in the ADC CTRL register (ADC powered).
CRC	-	37	50	-

13.6 SPI interfaces

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 15 Mbit/s, and the maximum supported bit rate for SPI slave mode is 1/(2 x 28 ns) = 17.8 Mbit/s at 3.0v <= VDD <= 3.6v and 1/(2 x 32 ns) = 15.6 Mbit/s at 1.7v <= VDD <= 3.0v.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins.

Table 21. SPI dynamic characteristics

T_{amb} = −40 °C to 105 °C; C_L = 20 pF; input slew = 1 ns. Simulated parameters sampled at the 30 % and 70 % level of the rising or falling edge; values guaranteed by design. Delays introduced by the external trace or external device are not considered.

Symbol	Parameter	Conditions	Min	Max	Unit
SPI master					
t_{DS}	data set-up time	1.71 V <= V_{DD} <= 3.6 V	10	-	ns
t_{DH}	data hold time	1.71 V <= V_{DD} <= 3.6 V	7	-	ns
$t_{v(Q)}$	data output valid time	1.71 V <= V_{DD} <= 3.6 V	0	2	ns
SPI slave					
t_{DS}	data set-up time	1.71 V <= V_{DD} <= 3.6 V	10	-	ns
t_{DH}	data hold time	1.71 V <= V_{DD} <= 3.6 V	7	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	28	ns
		1.71 V <= V_{DD} < 3.0 V	0	32	ns

15. Application information

15.1 Start-up behavior

Figure 33 shows the start-up timing after reset. The FRO 12 MHz oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

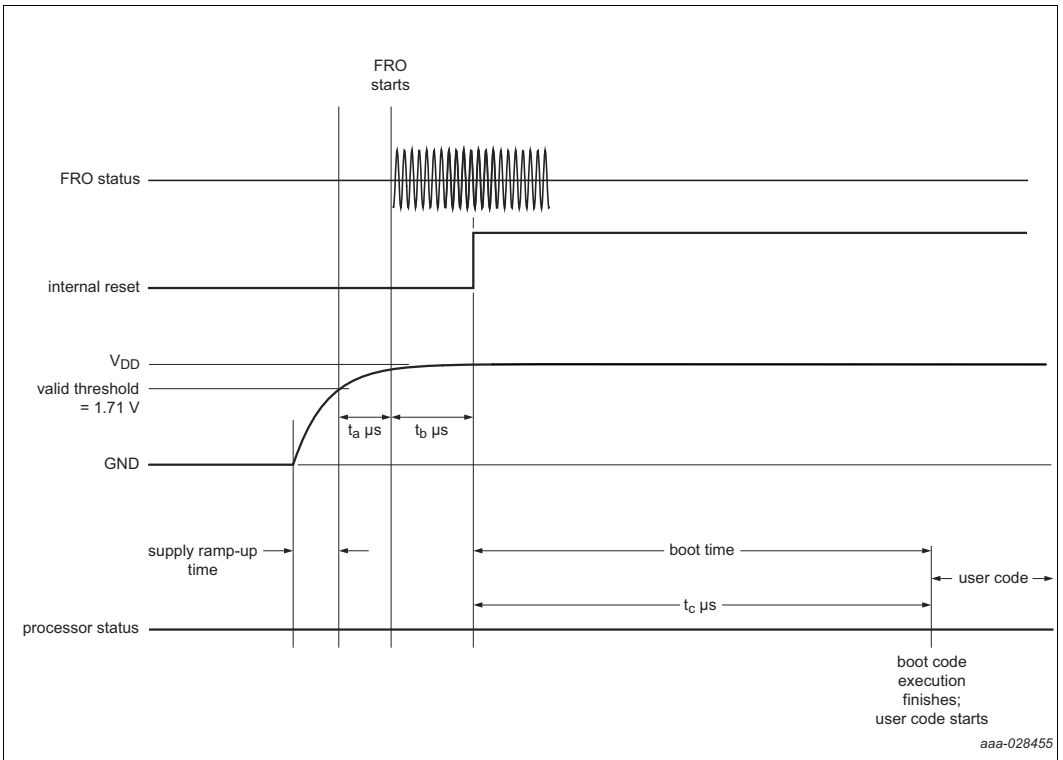


Fig 33. Start-up timing

Table 30. Typical start-up timing parameters

Parameter	Description	Value
t_a	FRO start time	≤ 26 µs
t_b	Internal reset de-asserted	101 µs
t_c	Boot time	36 µs

15.2 Connecting power, clocks, and debug functions

Figure 34 shows the basic board connections used to power the LPC802 and provide debug capabilities via the serial wire port.

15.4 Termination of unused pins

Table 31 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 31. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
all PIOn_m	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
VREFP	-	Tie to VDD.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

15.5 Pin states in different power modes

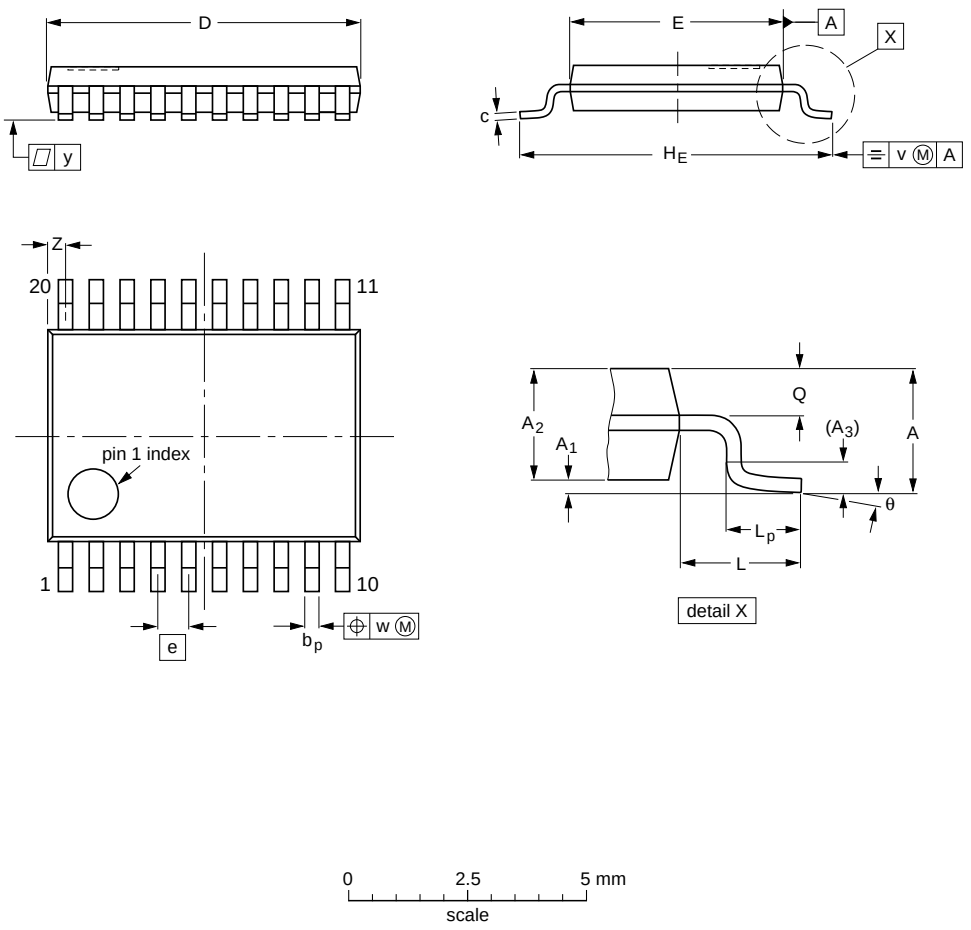
Table 32. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/power-down	Deep power-down
PIOn_m pins	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

16. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

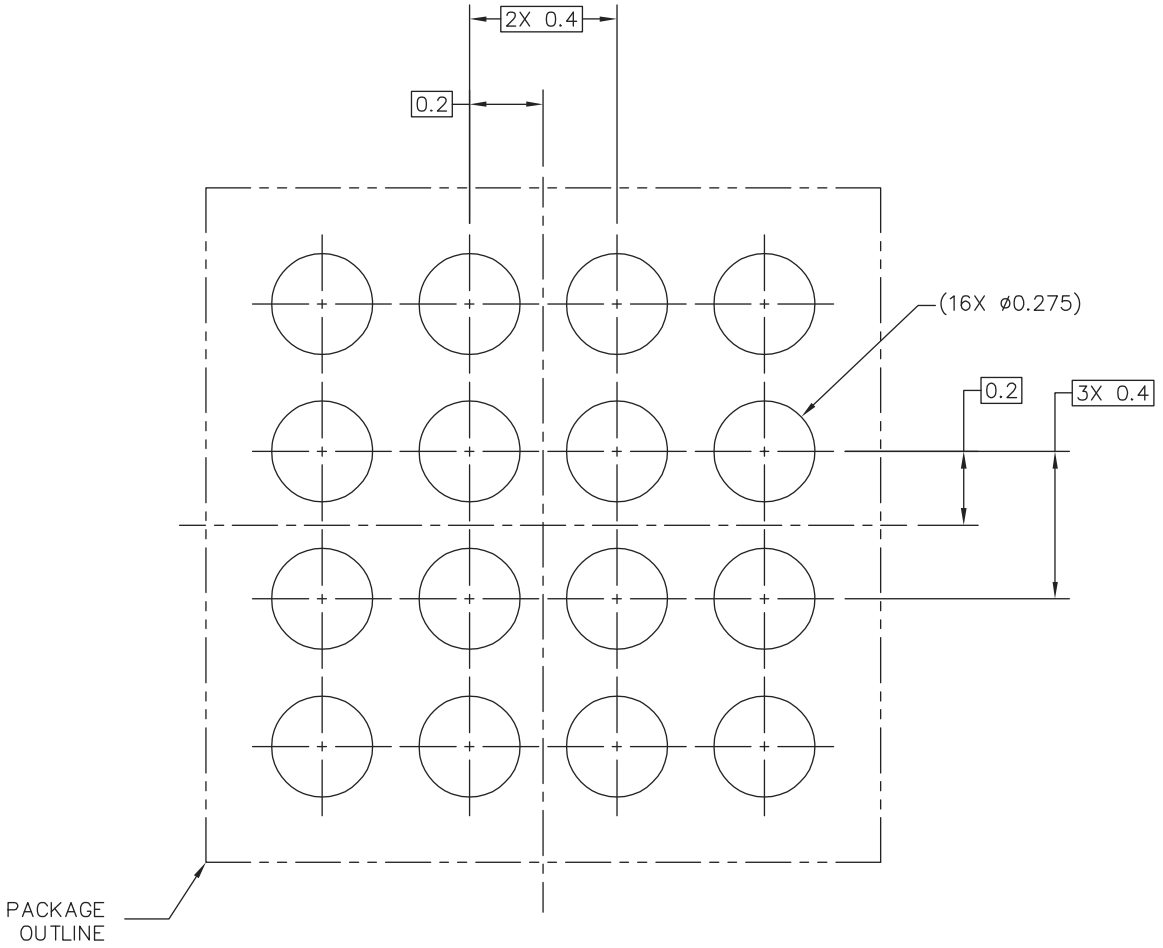
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 35. Package outline SOT360-1 (TSSOP20)



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

 DATE: 09 FEB 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1393–2	REVISION: 0	

Fig 44. Reflow soldering for the WLCSP16 (4x4) package (3 of 3)

20. Revision history

Table 34. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC802 v.1.6	20180427	Product data sheet	-	LPC802 v.1.5
Modifications:	• Added LPC802UK part. • Added text to Section 9.22.4.4 “Deep power-down mode”: Five general-purpose registers are available to store information during deep power-down mode. • Updated Section 9.22.1 “Internal oscillators”. Changed heading title. • Updated Section 15.2 “Connecting power, clocks, and debug functions”: removed text: connect the external crystal.			
LPC802 v.1.5	20180312	Product data sheet	-	LPC802 v.1.4
Modifications:	• Updated Table 3 “Device revision table”.			
LPC802 v.1.4	20180227	Product data sheet	-	LPC802 v.1.3
Modifications:	• Added Figure 38 “Package outline WLCSP16 (1.86 ´1.86 ´ 0.3 mm)”. • Added Figure 42 “Reflow soldering for the WLCSP16 (4x4) package (1 of 3)”, Figure 43 “Reflow soldering for the WLCSP16 (4x4) package (2 of 3)”, and Figure 44 “Reflow soldering for the WLCSP16 (4x4) package (3 of 3)”. • Updated title of Section 13.1 “Flash memory (EEPROM based)”. • Updated Table 12 “Static characteristics, supply pins”: Added condition: system clock = 1 MHz, VDD = 3.3 V. • Updated Table 16 “Dynamic characteristic: FRO”: Max values: FRO clock frequency; Condition: −20 °C ≤ T_{amb} ≤ 70 °C and FRO clock frequency; Condition: −40 °C ≤ T_{amb} ≤ 105 °C.			
LPC802 v.1.3	20180209	Product data sheet	-	LPC802 v.1.2
Modifications:	• Updated Section 2 “Features and benefits”. • Updated Table 5 “Movable functions (assign to pins PIO0_0 to PIO0_5, PIO0_7 to PIO0_17 through switch matrix)”. • Added level shifter functionality to Section 9.8 “I/O configuration”. • Updated Table 16 “Dynamic characteristic: FRO”: Changed frequencies to 9 MHz, 12 MHz, and 15 MHz. Added Condition: −20 °C ≤ T_{amb} ≤ 70 °C and Condition: −40 °C ≤ T_{amb} ≤ 70 °C.			
LPC802 v.1.2	20171222	Product data sheet	-	LPC802 v.1.1
Modifications:	• Updated Figure 4 “LPC802 block diagram”. • Updated Figure 12 “LPC802 clock generation”. • Updated Table 7 “Peripheral configuration in reduced power modes”: In deep-sleep mode flash is on standby.			
LPC802 v.1.1	20171222	Product data sheet	-	LPC802 v.1
Modifications:	• Updated Figure 21 “High-drive output: Typical HIGH-level output voltage VOH versus HIGH-level output current IOH” at 1.8 V.			
LPC802 v.1	20171218	Product data sheet	-	-

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