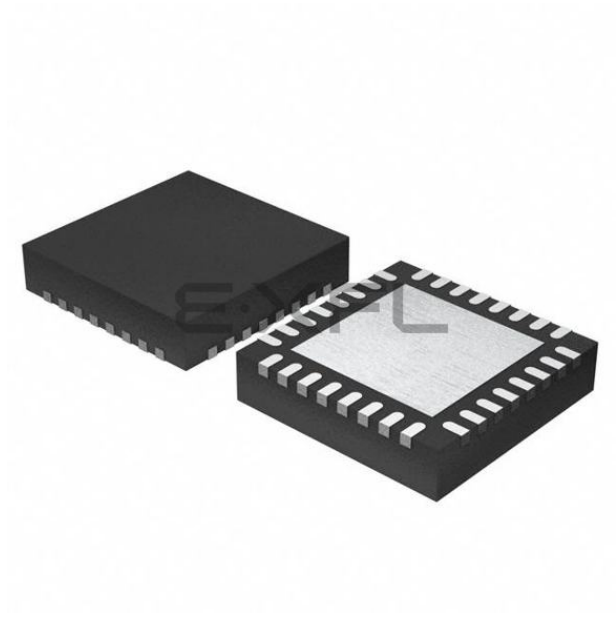

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	15MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc802m001jhi33e

3. Applications

- Sensor gateways
- Industrial
- Gaming controllers
- 8/16-bit applications
- Consumer
- Climate control
- Simple motor control
- Portables and wearables
- Lighting
- Motor control
- Fire and security applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC802M001JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC802M001JDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC802M011JDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC802M001JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC802UK	WLCSP16	wafer level chip-size package; 16 (4 × 4) bumps; 1.86 ×1.86 × 0.3 mm	SOT1393-2

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/KB	SRAM/ KB	USART	I^2C	SPI	GPIO	Dual I/O power supply	Package
LPC802M001JDH16	16	2	2	1	1	13	-	TSSOP16
LPC802M001JDH20	16	2	2	1	1	17	-	TSSOP20
LPC802M011JDH20	16	2	2	1	1	16	yes	TSSOP20
LPC802M001JHI33	16	2	2	1	1	17	-	HVQFN33
LPC802UK	16	2	2	1	1	13	-	WLCSP16

The LPC802 TSSOP16 packages have the following top-side marking:

- First line: LPC802
- Second line: M001J
- Third line: xxxx
- Fourth line: ywwx[R]
  - yww: Date code with y = year and ww = week.
  - xR = Boot code version and device revision.

The LPC802 WLCSP16 packages have the following top-side marking:

- First line: LPC802
- Second line: xxxxx
- Third line: xyywwx[R]
  - yyww: Date code with ww = week and yy = year.
  - xR = Boot code version and device revision.
- Fourth line: xxx - yyy

Table 3. Device revision table

Revision identifier (R)	Revision description
0A	Initial device revision with Boot ROM version 13.0
1A	Initial device revision with Boot ROM version 13.1
1B	Initial device revision with Boot ROM version 13.1

7.2 Pin description

Table 4 shows the pin functions that are fixed to specific pins on each package. These fixed-pin functions are selectable through the switch matrix between GPIO and the comparator, ADC, SWD, and RESET pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable functions for the I2C, USART, SPI, CTimer pins and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, an output and/or one or more inputs can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Eight GPIO pins trigger a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via an external pin, do not assign any movable function to this pin. The GPIO pins should be pulled HIGH externally before entering deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit deep power-down mode and wakes up the part.

The JTAG functions TDO, TDI, TCK, TMS, and TRST are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

PIO0_2, PIO0_3, and PIO0_12 are the high drive output pins. PIO0_4, PIO0_8, PIO0_9, PIO0_10, PIO0_11, PIO0_13, PIO0_15, and PIO0_17 are the WAKEUP pins.

Table 4. Pin description

Symbol	TSSOP20-1	TSSOP20-2	TSSOP16	HVQFN33	WLCSP16		Reset state[1]	Type	Description
PIO0_0/ ACMP_I1/TDO	19	19	16	24	D3	[2]	I; PU	IO	**PIO0_0 —** General-purpose port 0 input/output 0. In ISP mode, this is the U0_RXD pin (for single supply devices). In boundary scan mode: TDO (Test Data Out).
								A	**ACMP_I1 —** Analog comparator input 1.
PIO0_1/ADC_0/ ACMP_I2/CLKIN/TDI/	12	12	9	17	A4	[2]	I; PU	IO	**PIO0_1 —** General-purpose port 0 input/output 1. In boundary scan mode: TDI (Test Data In).
								A	**ACMP_I2 —** Analog comparator input 2.
								I	**CLKIN —** External clock input.
SWDIO/PIO0_2/ TMS	8	8	7	7	A2	[3]	I; PU	IO	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
								I/O	**PIO0_2 —** General-purpose port 0 input/output 2.
SWCLK/PIO0_3/ TCK	7	7	6	6	B1	[3]	I; PU	I	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
								IO	**PIO0_3 —** General-purpose port 0 input/output 3.
PIO0_4/ADC_11/ TRSTN	6	6	5	5	B2	[2]	I; PU	IO	**PIO0_4 —** General-purpose port 0 input/output 4. In ISP mode, this pin is the U0_TXD pin (for single supply devices). In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset).
								A	**ADC_11 —** ADC input 11.
$\overline{\text{RESET}}$/PIO0_5	5	5	4	4	C2	[4][5]	I; PU	IO	**$\overline{\text{RESET}}$ —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{\text{RESET}}$ function is not needed.
								I	**PIO0_5 —** General-purpose port 0 input/output 5.
PIO0_7/ADC_1/ $ACMPV_{REF}$	17	17	14	22	C3	[2]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7.
								A	**ADC_1 —** ADC input 1.
									$ACMPV_{REF}$ — Alternate reference voltage for the analog comparator.

9. Functional description

9.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 15 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

9.2 On-chip flash program memory

The LPC802 contain up to 16 KB of on-chip EEPROM based flash program memory.

9.3 On-chip SRAM

The LPC802 contain a total of 2 KB on-chip static RAM data memory.

9.4 On-chip ROM

The on-chip ROM contains the bootloader:

- Boot loader.
- Supports Flash In-Application Programming (IAP).
- Supports In-System Programming (ISP) through USART.
- On-chip ROM APIs for integer divide.
- Free Running Oscillator (FRO) API.

9.5 Memory map

The LPC802 incorporates several distinct memory regions. Figure 9 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

9.13.1 Features

- Maximum data rates of up to 15 Mbit/s in master mode and up to 18 Mbit/s in slave mode for SPI functions connected to all digital pins.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data, which can be useful while setting up an SPI memory.
- Control information can optionally be written along with data, which allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

9.14 I2C-bus interface (I2C0)

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master.

9.14.1 Features

- I2C0 supports standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.

9.15 CTimer

9.15.1 General-purpose 32-bit timers/external event counter

The LPC802 has one general-purpose 32-bit timer/counter.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. The timer/counter also includes three capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

9.15.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.

- Counter or timer operation.
- Up to three 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins can vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
  - Shadow registers are added for glitch-free PWM output.
- For each timer, up to 4 external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins can vary by device):
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Up to 4 match registers can be configured for PWM operation, allowing up to 3 single edged controlled PWM outputs. (The number of match outputs for each timer that are actually available on device pins can vary by device.)

9.16 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with two channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

9.16.1 Features

- 31-bit interrupt timer
- Two channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

9.17 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to service the watchdog timer periodically within a programmable time window.

9.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.

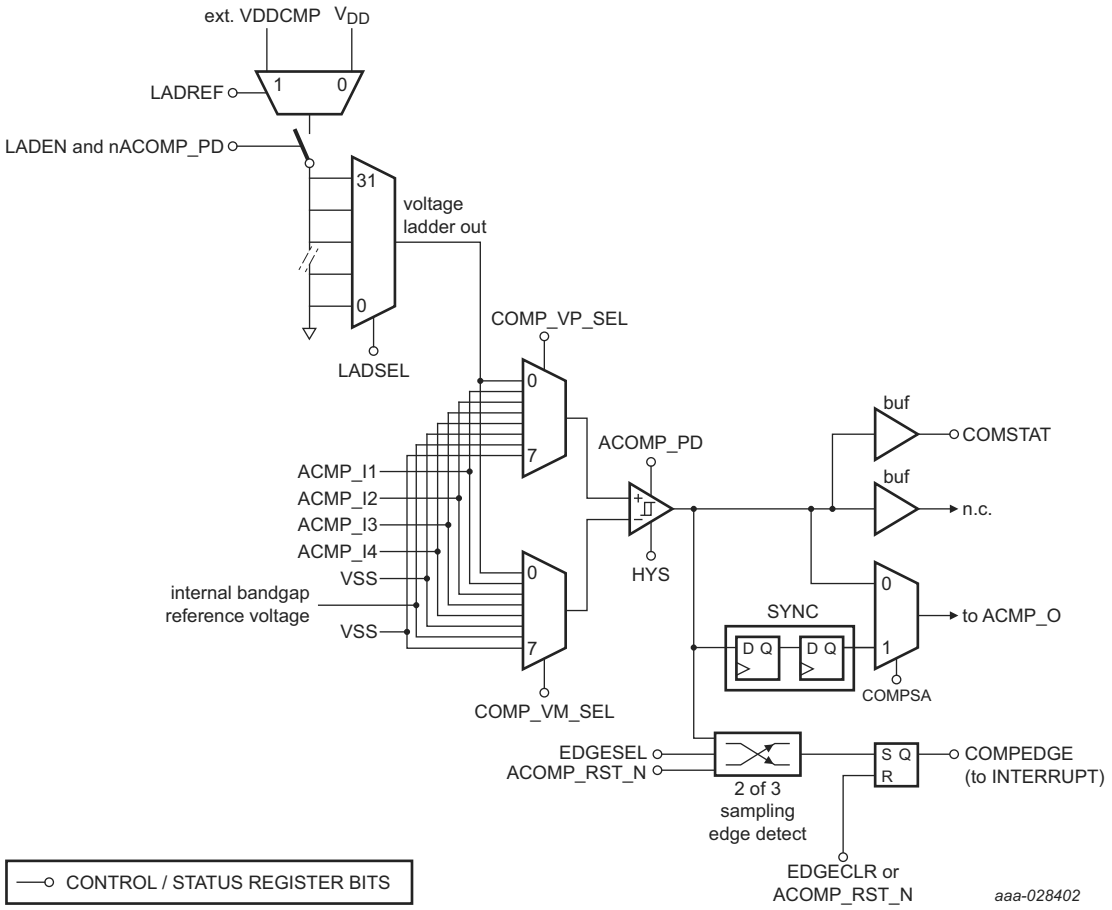


Fig 11. Comparator block diagram

9.19.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or $ACMPV_{REF}$); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- One comparator output is internally collected to the ADC trigger input multiplexer.

9.22 Clocking and power control

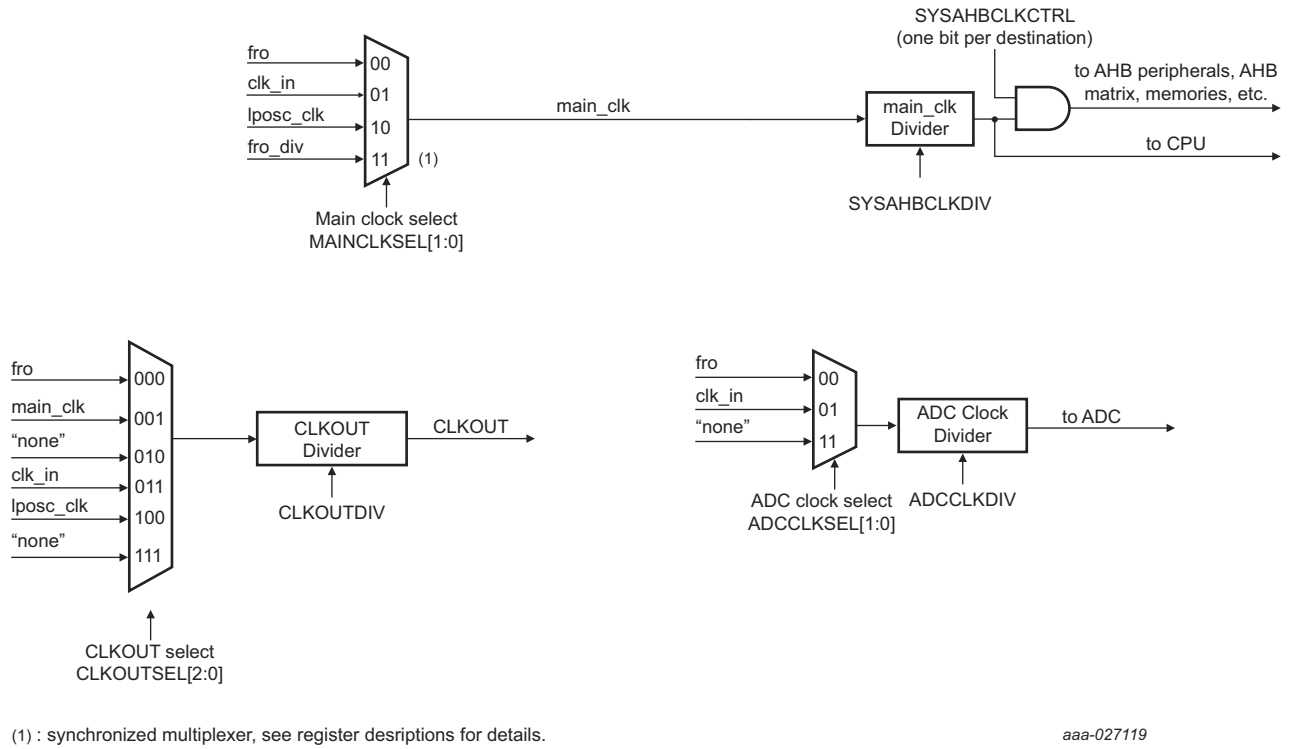


Fig 12. LPC802 clock generation

Power-down mode reduces power consumption compared to deep-sleep mode at the expense of longer wake-up times.

9.22.4.4 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the WAKEUP pins. The LPC802 can wake up from deep power-down mode via eight WAKEUP pins. See Section 9.18. Five general-purpose registers are available to store information during deep power-down mode.

The LPC802 can be prevented from entering deep power-down mode by setting a lock bit in the PMU block. Locking out deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

When entering deep power-down mode, an external pull-up resistor is required on the WAKEUP pins to hold it HIGH.

Table 7. Peripheral configuration in reduced power modes

Peripheral	Sleep mode	Deep-sleep mode	Power-down mode	Deep power-down mode
FRO	software configurable	on	off	off
FRO output	software configurable	off	off	off
Flash	software configurable	standby	off	off
BOD	software configurable	software configurable	software configurable	off
LPOsc/WWDT	software configurable	software configurable	software configurable	off
Digital peripherals	software configurable	off	off	off
Wake-up buffers	software configurable (cannot be used as wake-up source)	software configurable (cannot be used as wake-up source)	software configurable (cannot be used as wake-up source)	software configurable
ADC	software configurable	off	off	off

12. Static characteristics

12.1 General operating conditions

Table 11. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	15	MHz
V_{DD}	supply voltage (core and external rail)			1.71	-	3.6	V
		For ADC operations		2.5	-	3.6	V
V_{DDIO}	I/O rail			1.71	-	3.6	V
		For ADC operations		2.5	-	3.6	V
V_{ref}	ADC positive reference voltage	on pin VREFP		2.5	-	V_{DD}	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[2]	-	-	7.1	pF
		pins with digital functions only	[2]	-	-	2.8	pF

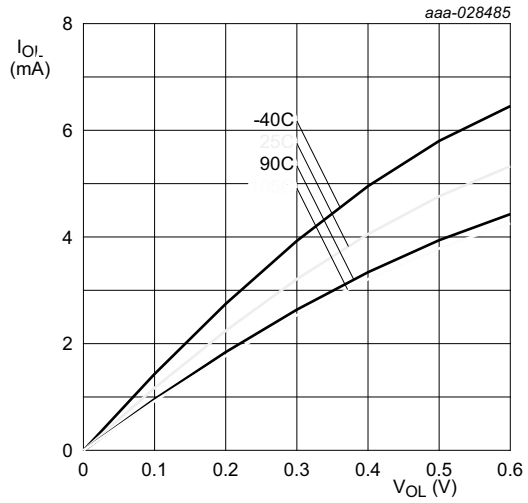
[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Including bonding pad capacitance. Based on simulation, not tested in production.

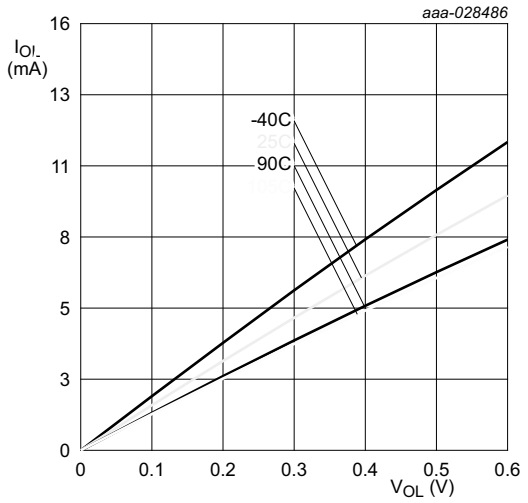
12.2 Power consumption

Power measurements in active, sleep, deep-sleep, and power-down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.

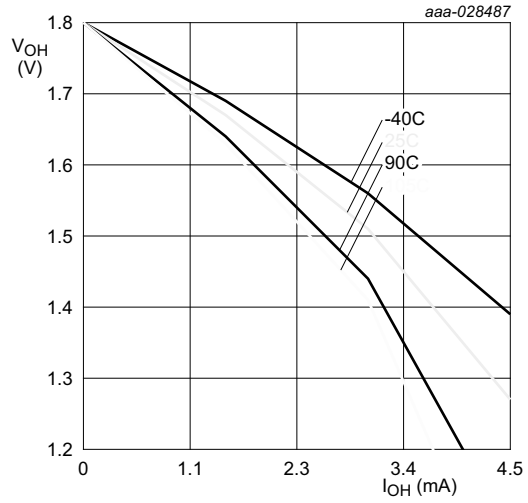


Conditions: V_{DD} = 1.8 V; standard port pins and high-drive pin PIO0_12.

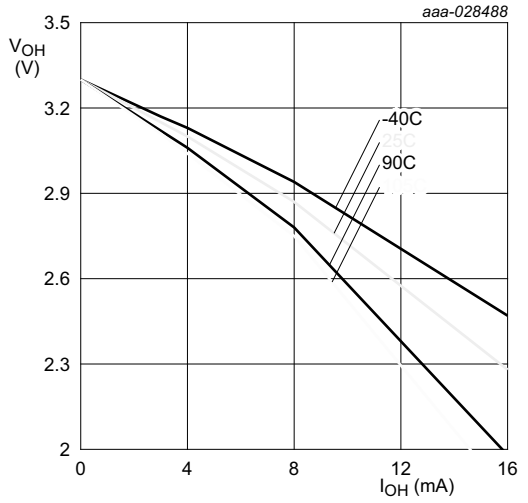


Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_12.

Fig 22. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 23. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

Table 20. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; values guaranteed by design.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
$t_{HD;DAT}$	data hold time	[3][4][7]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
$t_{SU;DAT}$	data set-up time	[8][9]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns

[1] See the I²C-bus specification *UM11045* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[8] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[9] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

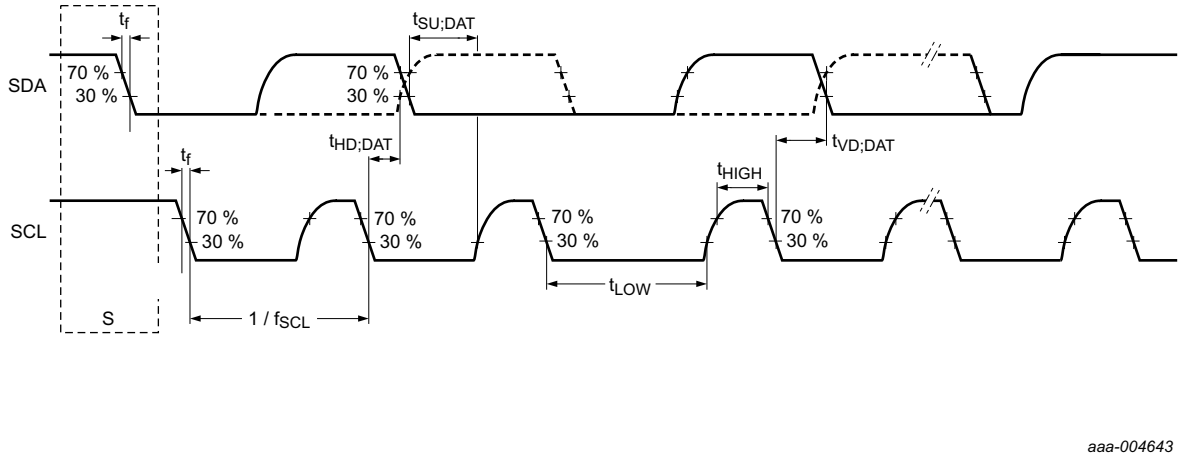


Fig 26. I²C-bus pins clock timing

13.6 SPI interfaces

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 15 Mbit/s, and the maximum supported bit rate for SPI slave mode is 1/(2 x 28 ns) = 17.8 Mbit/s at 3.0v <= VDD <= 3.6v and 1/(2 x 32 ns) = 15.6 Mbit/s at 1.7v <= VDD <= 3.0v.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins.

Table 21. SPI dynamic characteristics

T_{amb} = −40 °C to 105 °C; C_L = 20 pF; input slew = 1 ns. Simulated parameters sampled at the 30 % and 70 % level of the rising or falling edge; values guaranteed by design. Delays introduced by the external trace or external device are not considered.

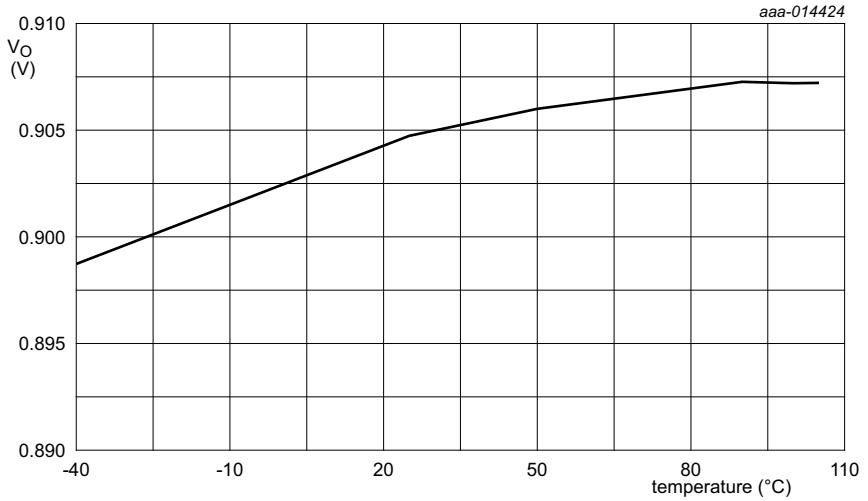
Symbol	Parameter	Conditions	Min	Max	Unit
SPI master					
t_{DS}	data set-up time	1.71 V <= V_{DD} <= 3.6 V	10	-	ns
t_{DH}	data hold time	1.71 V <= V_{DD} <= 3.6 V	7	-	ns
$t_{v(Q)}$	data output valid time	1.71 V <= V_{DD} <= 3.6 V	0	2	ns
SPI slave					
t_{DS}	data set-up time	1.71 V <= V_{DD} <= 3.6 V	10	-	ns
t_{DH}	data hold time	1.71 V <= V_{DD} <= 3.6 V	7	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	28	ns
		1.71 V <= V_{DD} < 3.0 V	0	32	ns

14.3 Comparator and internal voltage reference

Table 26. Internal voltage reference static and dynamic characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 3.3 V; hysteresis disabled in the comparator CTRL register.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = 25 °C to 105°C		860	-	940	mV
		T_{amb} = 25 °C			904		mV



V_{DD} = 3.3 V; characterized through bench measurements on typical samples.

Fig 32. Typical internal voltage reference output voltage

Table 27. Comparator characteristics

T_{amb} = −40 °C to +105 °C unless noted otherwise; V_{DD} = 1.71 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{ref(cmp)}$	comparator reference voltage	pin $ACMPV_{REF}$		1.5	-	3.6	V
I_{DD}	supply current	VP > VM; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	90	-	μA
		VM > VP; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	60	-	μA
V_{IC}	common-mode input voltage			0	-	V_{DD}	V
DV_O	output voltage variation			0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V; V_{DD} = 3.0 V	[2]	-	4	-	mV
		V_{IC} = 1.5 V; V_{DD} = 3.0 V	[2]	-	6	-	mV
		V_{IC} = 2.9 V; V_{DD} = 3.0V	[2]	-	6	-	mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process; V_{DD} = 3.3 V; T_{amb} = 25 °C		-	13	-	μs

Table 27. Comparator characteristics *...continued*

T_{amb} = −40 °C to +105 °C unless noted otherwise; V_{DD} = 1.71 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	HIGH to LOW; V_{DD} = 3.0 V; T_{amb} = 105 °C			320		
		V_{IC} = 0.1 V; 100 mV overdrive input	[1][2][4]	-		-	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1][2]	-	260	-	ns
		V_{IC} = 1.5 V; 100 mV overdrive input	[1][2][4]	-	300	-	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1][2]	-	160	-	ns
		V_{IC} = 2.9 V; 100 mV overdrive input	[1][2][4]	-	400	-	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1][2]	-	80	-	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DD} = 3.0 V; T_{amb} = 105 °C			170		
		V_{IC} = 0.1 V; 100 mV overdrive input	[1][2][4]	-		-	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1][2]	-	80	-	ns
		V_{IC} = 1.5 V; 100 mV overdrive input	[1][2][4]	-	120	-	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1][2]	-	220	-	ns
		V_{IC} = 2.9 V; 100 mV overdrive input	[1][2][4]	-	160	-	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1][2]	-	320	-	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V; T_{amb} = 105 °C; settings:	[3]	-	6	-	
		5 mV					mV
		10 mV		-	11	-	mV
		20 mV		-	21	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V; T_{amb} = 105 °C; settings:	[1][3]		11		
		5 mV		-		-	mV
		10 mV		-	18	-	mV
		20 mV		-	30	-	mV
R_{lad}	ladder resistance	-		-	1	-	MΩ

[1] C_L = 10 pF

[2] Characterized on typical samples, not tested in production.

[3] Input hysteresis is relative to the reference input channel and is software programmable.

[4] 100 mV overdrive corresponds to a square wave from 50 mV below the reference (V_{IC}) to 50 mV above the reference.

Table 28. Comparator voltage ladder dynamic characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	17	-	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1]	-	18	-	µs

[1] Characterized on typical samples, not tested in production.

Table 29. Comparator voltage ladder reference static characteristics

V_{DD} = 1.8 V to 3.6 V. T_{amb} = -40 °C to + 105 °C; external or internal reference.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$E_{V(O)}$	output voltage error	decimal code = 00	[2]	-	±6	-	mV
		decimal code = 08		-	±1	-	%
		decimal code = 16		-	±1	-	%
		decimal code = 24		-	±1	-	%
		decimal code = 30		-	±1	-	%
		decimal code = 31		-	±1	-	%

[1] Characterized though limited samples. Not tested in production.

[2] All peripherals except comparator, temperature sensor, and FRO turned off.

15. Application information

15.1 Start-up behavior

Figure 33 shows the start-up timing after reset. The FRO 12 MHz oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

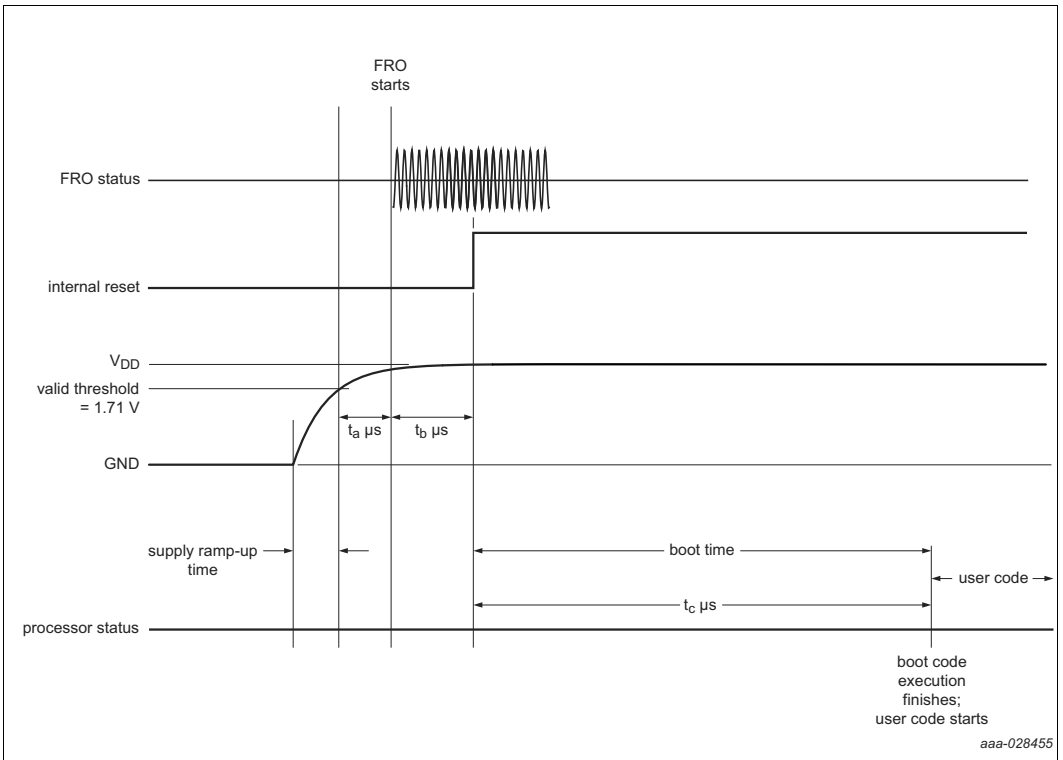


Fig 33. Start-up timing

Table 30. Typical start-up timing parameters

Parameter	Description	Value
t_a	FRO start time	≤ 26 µs
t_b	Internal reset de-asserted	101 µs
t_c	Boot time	36 µs

15.2 Connecting power, clocks, and debug functions

Figure 34 shows the basic board connections used to power the LPC802 and provide debug capabilities via the serial wire port.

15.3 I/O power consumption

I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in Table 14 for a given input voltage V_I. For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in Table 14, but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 14 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

18. Abbreviations

Table 33. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

19. References

[1] LPC802 User manual UM11045.

[2] LPC802 Errata sheet.

[3] I2C-bus specification *UM10204*.

[4] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf