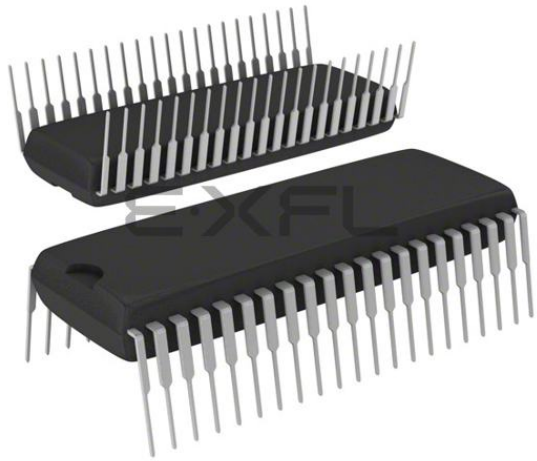

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	42-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f621j4b1

Figure 4. 20-pin SO20 Package Pinout

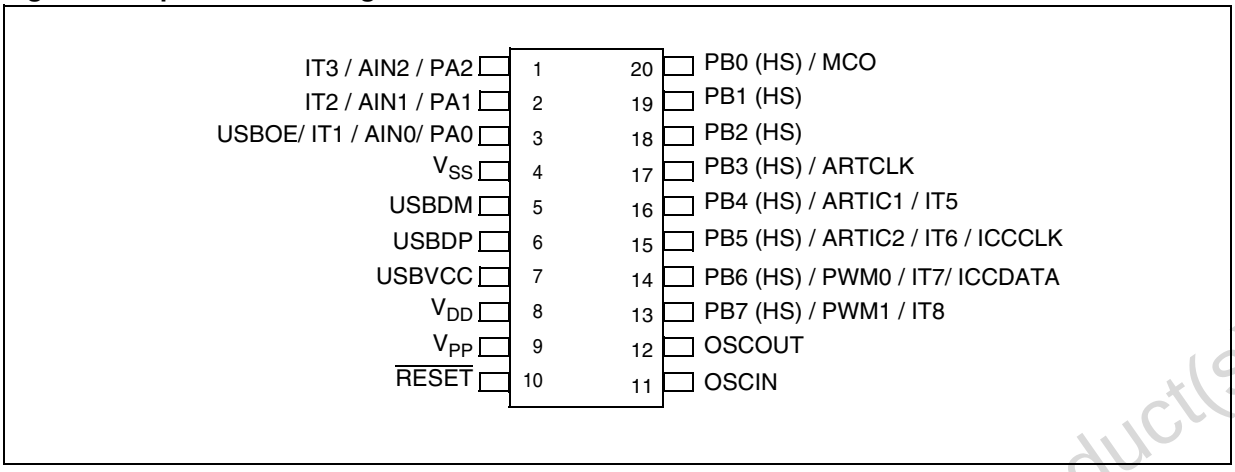
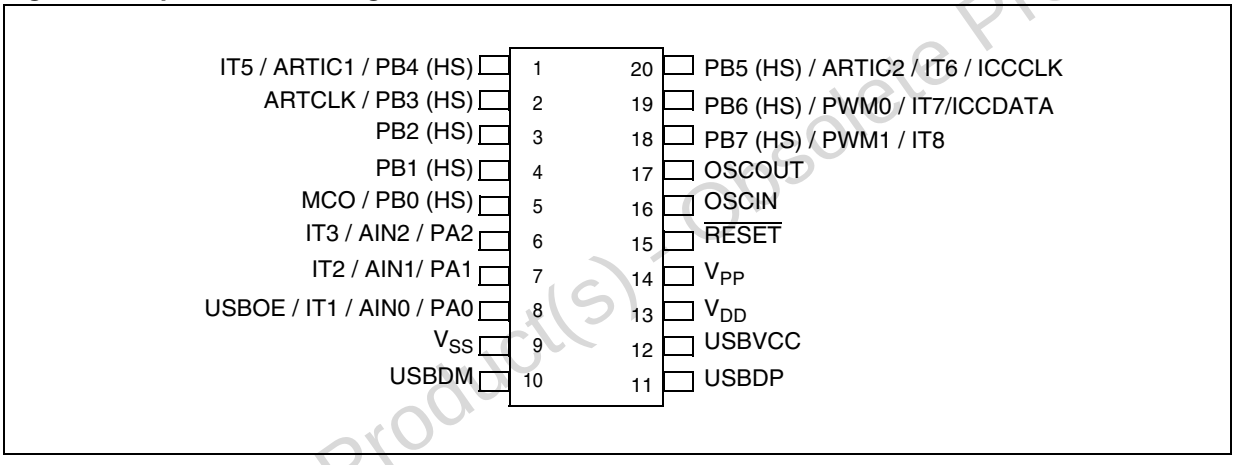


Figure 5. 20-pin DIP20 Package Pinout



Pin n°						Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function
										Input				Output			
LQFP44	DIP42	SO34	DIP32	SO20	DIP20			Input	Output	float	wpu	int	ana	OD	PP		
18	22	9	8	14	19	PB6/PWM0/IT7/ ICCDATA	I/O	C_T	HS	x		\			x	**Port B6**	ART PWM output 0/ Interrupt 7 input/In-Circuit Communication Data
19	23	10	9	15	20	PB5/ARTIC2/IT6/ ICCCLK	I/O	C_T	HS	x		/			x	**Port B5**	ART Input Capture 2/ Interrupt 6 input/ In-Circuit Communication Clock
20	24	11	10	16	1	PB4/ARTIC1/IT5	I/O	C_T	HS	x		/			x	**Port B4**	ART Input Capture 1/Interrupt 5 input
21	25	12	11	17	2	PB3/ARTCLK	I/O	C_T	HS	x					x	**Port B3**	ART Clock input
22	26	13	12	18	3	PB2/TDO	I/O	C_T	HS	x					x	**Port B2**	SCI Transmit Data Output [1]
23	27	14	13	19	4	PB1/RDI	I/O	C_T	HS	x					x	**Port B1**	SCI Receive Data Input [1]
24	28	15	14	20	5	PB0/MCO	I/O	C_T	HS	x					x	**Port B0**	CPU clock output
25	29	16	15	-	-	PA7/AIN7	I/O	C_T		x			x		x	**Port A7**	ADC Analog Input 7
26	30	17	16	-	-	PA6/AIN6	I/O	C_T		x			x		x	**Port A6**	ADC Analog Input 6
27	31	18	17	-	-	PA5/AIN5	I/O	C_T		x			x		x	**Port A5**	ADC Analog Input 5
28	32	19	18	-	-	PA4/AIN4	I/O	C_T		x			x		x	**Port A4**	ADC Analog Input 4
29	33	20	19	-	-	PA3/AIN3/IT4	I/O	C_T		x		\	x		x	**Port A3**	ADC Analog Input 3/ Interrupt 4 input
30	34	21	20	1	6	PA2/AIN2/IT3	I/O	C_T		x		\	x		x	**Port A2**	ADC Analog Input 2/ Interrupt 3 input
31	35	22	21	2	7	PA1/AIN1/IT2	I/O	C_T		x		\	x		x	**Port A1**	ADC Analog Input 1/ Interrupt 2 input
32	36	23	22	3	8	PA0/AIN0/IT1/ USBOE	I/O	C_T		x		\	x		x	**Port A0**	ADC Analog Input 0/ Interrupt 1 input/ USB Output Enable
33	37	30	29	10	15	$\overline{\text{RESET}}$	I/O	C								Top priority non maskable interrupt (active low)	
34	38	24	23	-	-	V_{SSA}	S									Analog Ground Voltage, must be connected externally to V_{SS}.	
35	39	25	24	5	10	USBDM	I/O									USB bidirectional data (data -)	
36	40	26	25	6	11	USBDP	I/O									USB bidirectional data (data +)	
37	41	27	26	7	12	USBVCC	S									USB power supply 3.3V output	
38	42	28	27	-	-	V_{DDA}	S									Analog Power Supply Voltage, must be connected externally to V_{DD}.	
39	-	-	-	-	-	Reserved										Must be left unconnected.	
40	1	-	-	-	-	PD6	I/O	C_T			x				x	**Port D6**	
41	2	-	-	-	-	PD5	I/O	C_T			x				x	**Port D5**	
42	3	-	-	-	-	PD4	I/O	C_T			x				x	**Port D4**	

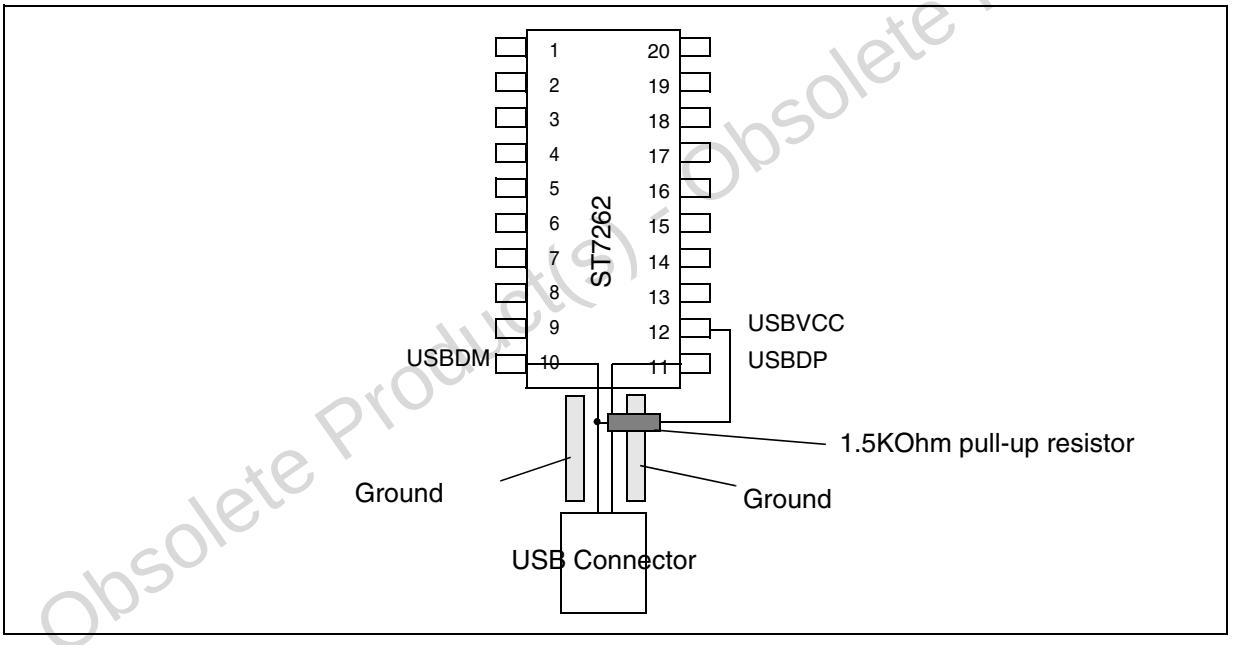
Pin n°						Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function
										Input				Output			
LQFP44	DIP42	SO34	DIP32	SO20	DIP20			Input	Output	float	wpu	int	ana	OD	PP		
43	4	-	-	-	-	PD3	I/O	C_T			x				x	**Port D3**	
44	5	-	-	-	-	PD2	I/O	C_T			x				x	**Port D2**	

Note 1: Peripheral not present on all devices. Refer to "Device Summary" on page 1.

2.1 PCB LAYOUT RECOMMENDATION

In the case of DIP20 devices the user should lay-out the PCB so that the DIP20 ST7262 device and the USB connector are centered on the same axis ensuring that the D- and D+ lines are of equal length. Refer to Figure 6

Figure 6. Recommended PCB Layout for USB Interface with DIP20 package



3 REGISTER & MEMORY MAP

As shown in the Figure 7, the MCU is capable of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 64 bytes of register locations, 768 bytes of RAM and up to 16 Kbytes of user program memory. The RAM space includes up to 128 bytes for the stack from 0100h to 017Fh.

The highest address bytes contain the user reset and interrupt vectors.

IMPORTANT: Memory locations marked as “Reserved” must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 7. Memory Map

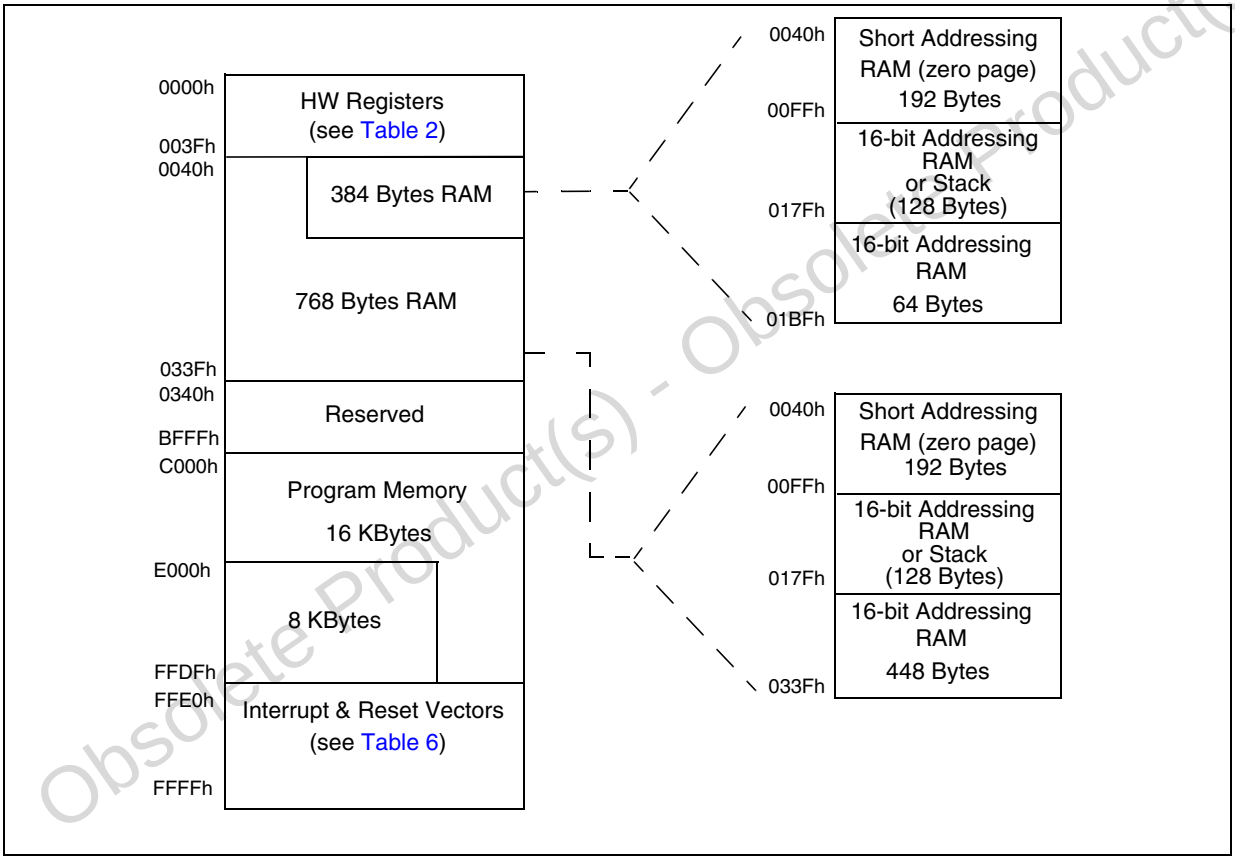
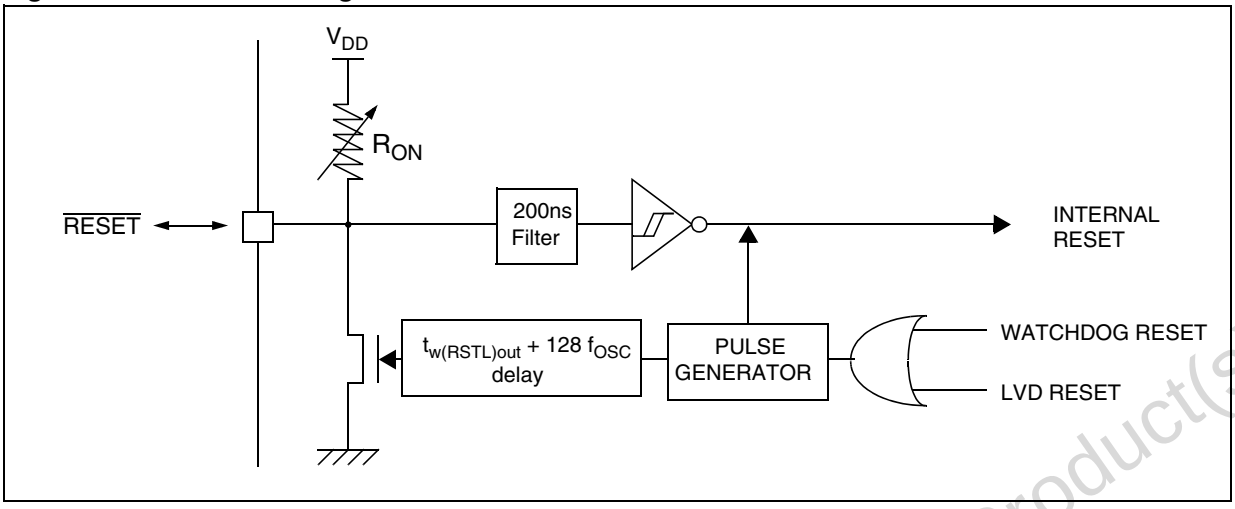


Figure 19. Reset Block Diagram



Note: The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).

PWM AUTO-RELOAD TIMER (Cont'd)

Independent PWM signal generation

This mode allows up to two Pulse Width Modulated signals to be generated on the PWMx output pins with minimum core processing overhead. This function is stopped during HALT mode.

Each PWMx output signal can be selected independently using the corresponding OEx bit in the PWM Control register (PWMCR). When this bit is set, the corresponding I/O pin is configured as output push-pull alternate function.

The PWM signals all have the same frequency which is controlled by the counter period and the ARTARR register value.

$$f_{PWM} = f_{COUNTER} / (256 - ARTARR)$$

When a counter overflow occurs, the PWMx pin level is changed depending on the corresponding OPx (output polarity) bit in the PWMCR register. When the counter reaches the value contained in one of the output compare register (OCRx) the corresponding PWMx pin level is restored.

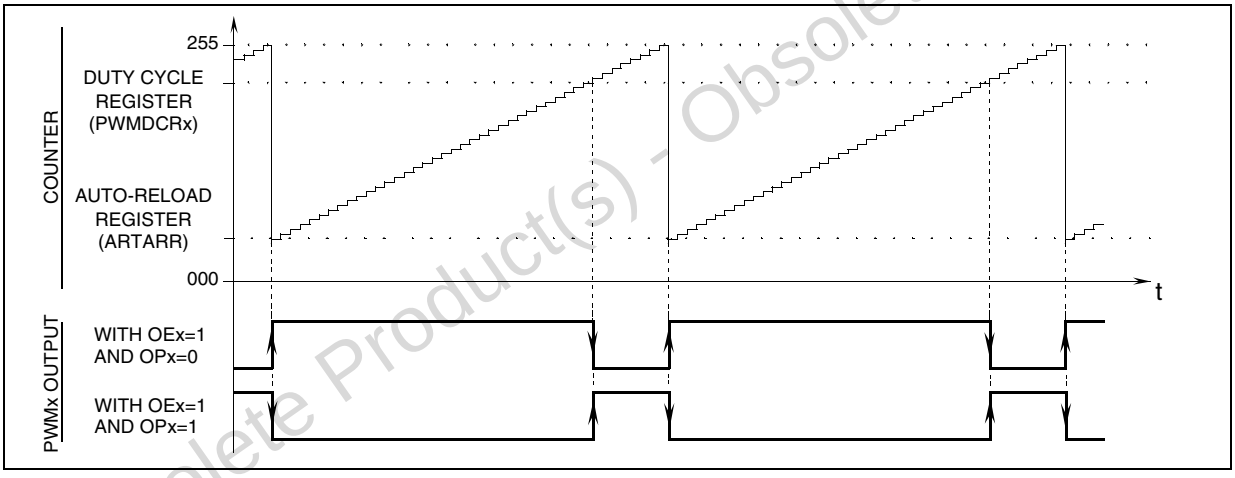
It should be noted that the reload values will also affect the value and the resolution of the duty cycle of the PWM output signal. To obtain a signal on a PWMx pin, the contents of the OCRx register must be greater than the contents of the ARTARR register.

The maximum available resolution for the PWMx duty cycle is:

$$Resolution = 1 / (256 - ARTARR)$$

Note: To get the maximum resolution (1/256), the ARTARR register must be 0. With this maximum resolution, 0% and 100% can be obtained by changing the polarity.

Figure 33. PWM Auto-reload Timer Function



TIMEBASE UNIT (Cont'd)

10.3.5 Low Power Modes

Mode	Description
WAIT	No effect on TBU
HALT	TBU halted.

10.3.6 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
Counter Overflow Event	OVF	ITE	Yes	No

Note: The OVF interrupt event is connected to an interrupt vector (see Interrupts chapter).
It generates an interrupt if the ITE bit is set in the TBUCSR register and the I-bit in the CC register is reset (RIM instruction).

10.3.7 Register Description

TBU COUNTER VALUE REGISTER (TBUCV)
Read/Write
Reset Value: 0000 0000 (00h)

7							0
CV7	CV6	CV5	CV4	CV3	CV2	CV1	CV0

Bit 7:0 = **CV[7:0]** *Counter Value*

This register contains the 8-bit counter value which can be read and written anytime by software. It is continuously incremented by hardware if TCEN=1.

TBU CONTROL/STATUS REGISTER (TBUCSR)
Read/Write
Reset Value: 0000 0000 (00h)

7							0
0	CAS	OVF	ITE	TCEN	PR2	PR1	PR0

Bit 7 = Reserved. Forced by hardware to 0.

Bit 6 = **CAS** *Cascading Enable*
This bit is set and cleared by software. It is used to cascade the TBU and the PWM/ART timers.
0: Cascading disabled
1: Cascading enabled

Bit 5 = **OVF** *Overflow Flag*

This bit is set only by hardware, when the counter value rolls over from FFh to 00h. It is cleared by software reading the TBUCSR register. Writing to this bit does not change the bit value.
0: No overflow
1: Counter overflow

Bit 4 = **ITE** *Interrupt enabled.*

This bit is set and cleared by software.
0: Overflow interrupt disabled
1: Overflow interrupt enabled. An interrupt request is generated when OVF=1.

Bit 3 = **TCEN** *TBU Enable.*

This bit is set and cleared by software.
0: TBU counter is frozen and the prescaler is reset.
1: TBU counter and prescaler running.

Bit 2:0 = **PR[2:0]** *Prescaler Selection*

These bits are set and cleared by software to select the prescaling factor.

PR2	PR1	PR0	Prescaler Division Factor
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

SERIAL PERIPHERAL INTERFACE (Cont'd)

10.4.3.1 Functional Description

A basic example of interconnections between a single master and a single slave is illustrated in Figure 40.

The MOSI pins are connected together and the MISO pins are connected together. In this way data is transferred serially between master and slave (most significant bit first).

The communication is always initiated by the master. When the master device transmits data to a slave device via MOSI pin, the slave device responds by sending data to the master device via the MISO pin. This implies full duplex communication with both data out and data in synchronized with the same clock signal (which is provided by the master device via the SCK pin).

To use a single data line, the MISO and MOSI pins must be connected at each node (in this case only simplex communication is possible).

Four possible data/clock timing relationships may be chosen (see Figure 43) but master and slave must be programmed with the same timing mode.

Figure 40. Single Master/ Single Slave Application

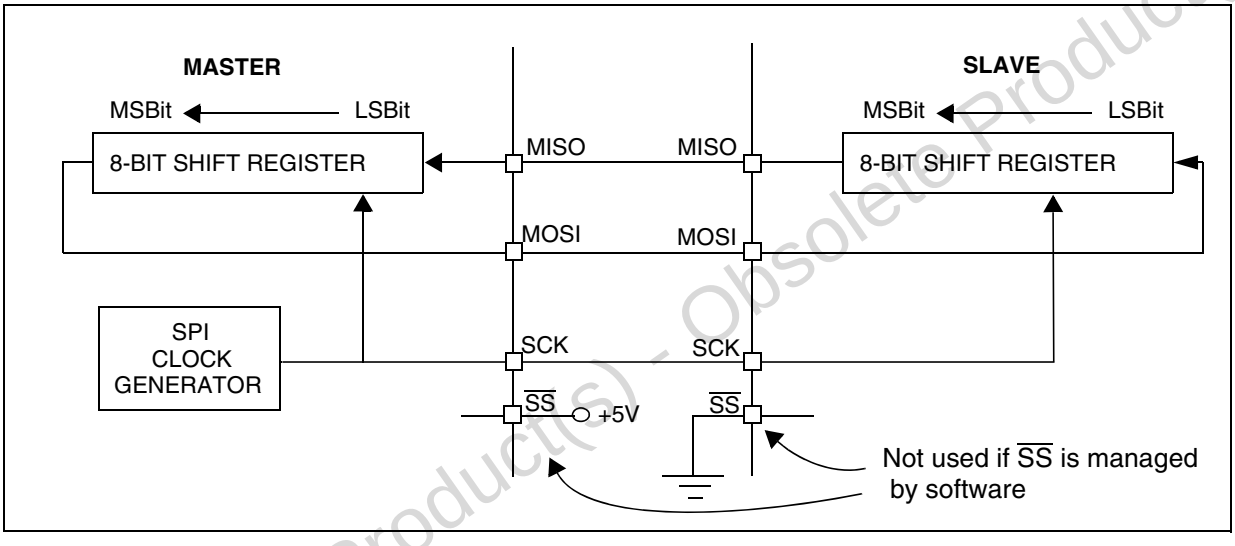


Table 19. SPI Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0011h	**SPIDR** Reset Value	MSB x	x	x	x	x	x	x	LSB x
0012h	**SPICR** Reset Value	SPIE 0	SPE 0	SPR2 0	MSTR 0	CPOL x	CPHA x	SPR1 x	SPR0 x
0013h	**SPICSR** Reset Value	SPIF 0	WCOL 0	OVR 0	MODF 0	0	SOD 0	SSM 0	SSI 0

10.5 SERIAL COMMUNICATIONS INTERFACE (SCI)

10.5.1 Introduction

The Serial Communications Interface (SCI) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The SCI offers a very wide range of baud rates using two baud rate generator systems.

10.5.2 Main Features

- Full duplex, asynchronous communications
- NRZ standard format (Mark/Space)
- Dual baud rate generator systems
- Independently programmable transmit and receive baud rates up to 500K baud
- Programmable data word length (8 or 9 bits)
- Receive buffer full, Transmit buffer empty and End of Transmission flags
- Two receiver wake-up modes:
  - Address bit (MSB)
  - Idle line
- Muting function for multiprocessor configurations
- Separate enable bits for Transmitter and Receiver
- Four error detection flags:
  - Overrun error
  - Noise error
  - Frame error
  - Parity error
- Five interrupt sources with flags:
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Idle line received
  - Overrun error detected
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Reduced power consumption mode

10.5.3 General Description

The interface is externally connected to another device by two pins (see Figure 47):

– TDO: Transmit Data Output. When the transmitter and the receiver are disabled, the output pin returns to its I/O port configuration. When the transmitter and/or the receiver are enabled and nothing is to be transmitted, the TDO pin is at high level.

– RDI: Receive Data Input is the serial data input. Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise.

Through these pins, serial data is transmitted and received as frames comprising:

– An Idle Line prior to transmission or reception

– A start bit

– A data word (8 or 9 bits) least significant bit first

– A Stop bit indicating that the frame is complete

This interface uses two types of baud rate generator:

– A conventional type for commonly-used baud rates

– An extended type with a prescaler offering a very wide range of baud rates even with non-standard oscillator frequencies

SERIAL COMMUNICATIONS INTERFACE (Cont'd)

10.5.4.2 Transmitter

The transmitter can send data words of either 8 or 9 bits depending on the M bit status. When the M bit is set, word length is 9 bits and the 9th bit (the MSB) has to be stored in the T8 bit in the SCICR1 register.

Character Transmission

During an SCI transmission, data shifts out least significant bit first on the TDO pin. In this mode, the SCIDR register consists of a buffer (TDR) between the internal bus and the transmit shift register (see Figure 46).

Procedure

– Select the M bit to define the word length.

– Select the desired baud rate using the SCIBRR and the SCIETPR registers.

– Set the TE bit to assign the TDO pin to the alternate function and to send a idle frame as first transmission.

– Access the SCISR register and write the data to send in the SCIDR register (this sequence clears the TDRE bit). Repeat this sequence for each data to be transmitted.

Clearing the TDRE bit is always performed by the following software sequence:

1. An access to the SCISR register

2. A write to the SCIDR register

The TDRE bit is set by hardware and it indicates:

– The TDR register is empty.

– The data transfer is beginning.

– The next data can be written in the SCIDR register without overwriting the previous data.

This flag generates an interrupt if the TIE bit is set and the I bit is cleared in the CC register.

When a transmission is taking place, a write instruction to the SCIDR register stores the data in the TDR register and which is copied in the shift register at the end of the current transmission.

When no transmission is taking place, a write instruction to the SCIDR register places the data directly in the shift register, the data transmission starts, and the TDRE bit is immediately set.

When a frame transmission is complete (after the stop bit) the TC bit is set and an interrupt is generated if the TCIE is set and the I bit is cleared in the CC register.

Clearing the TC bit is performed by the following software sequence:

1. An access to the SCISR register

2. A write to the SCIDR register

Note: The TDRE and TC bits are cleared by the same software sequence.

Break Characters

Setting the SBK bit loads the shift register with a break character. The break frame length depends on the M bit (see Figure 47).

As long as the SBK bit is set, the SCI send break frames to the TDO pin. After clearing this bit by software the SCI insert a logic 1 bit at the end of the last break frame to guarantee the recognition of the start bit of the next frame.

Idle Characters

Setting the TE bit drives the SCI to send an idle frame before the first data frame.

Clearing and then setting the TE bit during a transmission sends an idle frame after the current word.

Note: Resetting and setting the TE bit causes the data in the TDR register to be lost. Therefore the best time to toggle the TE bit is when the TDRE bit is set, that is, before writing the next byte in the SCIDR.

SERIAL COMMUNICATIONS INTERFACE (Cont'd)

DATA REGISTER (SCIDR)

Read/Write

Reset Value: Undefined

Contains the Received or Transmitted data character, depending on whether it is read from or written to.

7							0
DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0

The Data register performs a double function (read and write) since it is composed of two registers, one for transmission (TDR) and one for reception (RDR).
The TDR register provides the parallel interface between the internal bus and the output shift register (see Figure 46).
The RDR register provides the parallel interface between the input shift register and the internal bus (see Figure 46).

BAUD RATE REGISTER (SCIBRR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
SCP1	SCP0	SCT2	SCT1	SCT0	SCR2	SCR1	SCR0

Bits 7:6 = **SCP[1:0]** *First SCI Prescaler*
These 2 prescaling bits allow several standard clock division ranges:

PR Prescaling factor	SCP1	SCP0
1	0	0
3	0	1
4	1	0
13	1	1

Bits 5:3 = **SCT[2:0]** *SCI Transmitter rate divisor*
These 3 bits, in conjunction with the SCP1 & SCP0 bits define the total division applied to the bus clock to yield the transmit rate clock in conventional Baud Rate Generator mode.

TR dividing factor	SCT2	SCT1	SCT0
1	0	0	0
2	0	0	1
4	0	1	0
8	0	1	1
16	1	0	0
32	1	0	1
64	1	1	0
128	1	1	1

Bits 2:0 = **SCR[2:0]** *SCI Receiver rate divisor.*
These 3 bits, in conjunction with the SCP[1:0] bits define the total division applied to the bus clock to yield the receive rate clock in conventional Baud Rate Generator mode.

RR Dividing factor	SCR2	SCR1	SCR0
1	0	0	0
2	0	0	1
4	0	1	0
8	0	1	1
16	1	0	0
32	1	0	1
64	1	1	0
128	1	1	1

USB INTERFACE (Cont'd)

PID REGISTER (PIDR)

Read only

Reset Value: xx00 0000 (x0h)

7							0
TP3	TP2	0	0	0	RX_ SEZ	RXD	0

Bits 7:6 = **TP[3:2]** *Token PID bits 3 & 2*.
USB token PIDs are encoded in four bits. **TP[3:2]** correspond to the variable token PID bits 3 & 2.
Note: PID bits 1 & 0 have a fixed value of 01.
When a CTR interrupt occurs (see register ISTR) the software should read the TP3 and TP2 bits to retrieve the PID name of the token received.
The USB standard defines TP bits as:

TP3	TP2	PID Name
0	0	OUT
1	0	IN
1	1	SETUP

Bits 5:3 Reserved. Forced by hardware to 0.

Bit 2 = **RX_SEZ** *Received single-ended zero*
This bit indicates the status of the RX_SEZ transceiver output.
0: No SE0 (single-ended zero) state
1: USB lines are in SE0 (single-ended zero) state

Bit 1 = **RXD** *Received data*
0: No K-state
1: USB lines are in K-state

This bit indicates the status of the RXD transceiver output (differential receiver output).

Note: If the environment is noisy, the RX_SEZ and RXD bits can be used to secure the application. By interpreting the status, software can distinguish a valid End Suspend event from a spurious wake-up due to noise on the external USB line. A valid End Suspend is followed by a Resume or Reset sequence. A Resume is indicated by RXD=1, a Reset is indicated by RX_SEZ=1.

Bit 0 = Reserved. Forced by hardware to 0.

INTERRUPT STATUS REGISTER (ISTR)

Read / Write

Reset Value: 0000 0000 (00h)

7							0
SUSP	DOVR	CTR	ERR	IOVR	ESUSP	RESET	SOF

When an interrupt occurs these bits are set by hardware. Software must read them to determine the interrupt type and clear them after servicing.
Note: These bits cannot be set by software.

Bit 7 = **SUSP** *Suspend mode request*.
This bit is set by hardware when a constant idle state is present on the bus line for more than 3 ms, indicating a suspend mode request from the USB bus. The suspend request check is active immediately after each USB reset event and its disabled by hardware when suspend mode is forced (FSUSP bit of CTLR register) until the end of resume sequence.

Bit 6 = **DOVR** *DMA over/underrun*.
This bit is set by hardware if the ST7 processor can't answer a DMA request in time.
0: No over/underrun detected
1: Over/underrun detected

Bit 5 = **CTR** *Correct Transfer.* This bit is set by hardware when a correct transfer operation is performed. The type of transfer can be determined by looking at bits TP3-TP2 in register PIDR. The Endpoint on which the transfer was made is identified by bits EP1-EP0 in register IDR.
0: No Correct Transfer detected
1: Correct Transfer detected

Note: A transfer where the device sent a NAK or STALL handshake is considered not correct (the host only sends ACK handshakes). A transfer is considered correct if there are no errors in the PID and CRC fields, if the DATA0/DATA1 PID is sent as expected, if there were no data overruns, bit stuffing or framing errors.

Bit 4 = **ERR** *Error.*
This bit is set by hardware whenever one of the errors listed below has occurred:
0: No error detected
1: Timeout, CRC, bit stuffing or nonstandard framing error detected

INSTRUCTION SET OVERVIEW (Cont'd)

Mnemo	Description	Function/Example	Dst	Src		I1	H	I0	N	Z	C
JRULE	Jump if (C + Z = 1)	Unsigned <=									
LD	Load	dst <= src	reg, M	M, reg					N	Z	
MUL	Multiply	X,A = X * A	A, X, Y	X, Y, A			0				0
NEG	Negate (2's compl)	neg $10	reg, M						N	Z	C
NOP	No Operation										
OR	OR operation	A = A + M	A	M					N	Z	
POP	Pop from the Stack	pop reg	reg	M							
		pop CC	CC	M		I1	H	I0	N	Z	C
PUSH	Push onto the Stack	push Y	M	reg, CC							
RCF	Reset carry flag	C = 0									0
RET	Subroutine Return										
RIM	Enable Interrupts	I1:0 = 10 (level 0)				1		0			
RLC	Rotate left true C	C <= A <= C	reg, M						N	Z	C
RRC	Rotate right true C	C => A => C	reg, M						N	Z	C
RSP	Reset Stack Pointer	S = Max allowed									
SBC	Substract with Carry	A = A - M - C	A	M					N	Z	C
SCF	Set carry flag	C = 1									1
SIM	Disable Interrupts	I1:0 = 11 (level 3)				1		1			
SLA	Shift left Arithmetic	C <= A <= 0	reg, M						N	Z	C
SLL	Shift left Logic	C <= A <= 0	reg, M						N	Z	C
SRL	Shift right Logic	0 => A => C	reg, M						0	Z	C
SRA	Shift right Arithmetic	A7 => A => C	reg, M						N	Z	C
SUB	Substraction	A = A - M	A	M					N	Z	C
SWAP	SWAP nibbles	A7-A4 <=> A3-A0	reg, M						N	Z	
TNZ	Test for Neg & Zero	tnz lbl1							N	Z	
TRAP	S/W trap	S/W interrupt				1		1			
WFI	Wait for Interrupt					1		0			
XOR	Exclusive OR	A = A XOR M	A	M					N	Z	

12.2.3 Thermal Characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature[1)]	175	°C

Notes:
1. The maximum chip-junction temperature is based on technology characteristics.

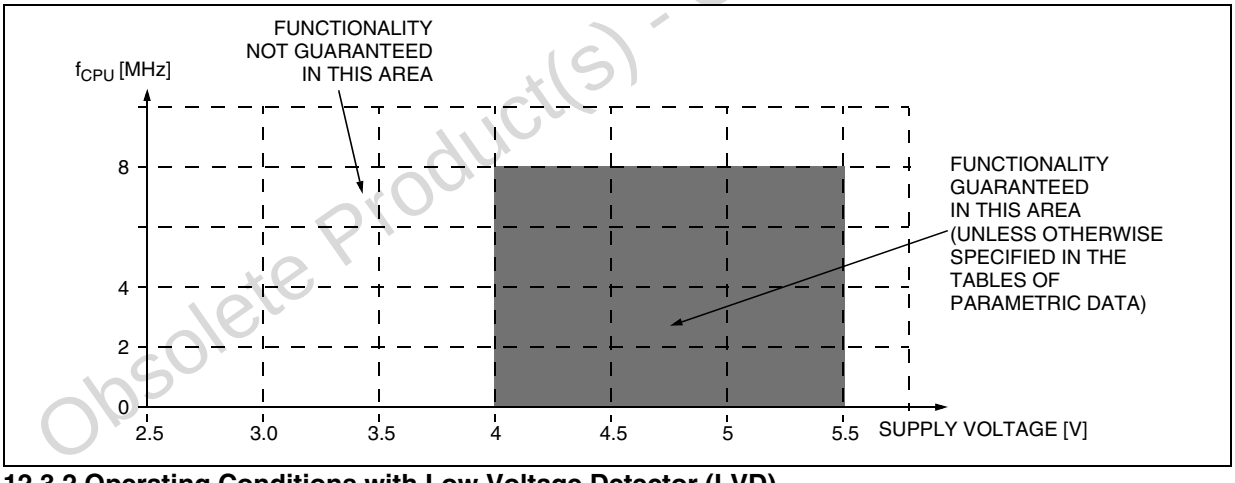
12.3 OPERATING CONDITIONS

12.3.1 General Operating Conditions (standard voltage ROM and Flash devices)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating Supply Voltage	f_{CPU} = 8 MHz	4	5	5.5	
V_{DDA}	Analog reference voltage		V_{DD}		V_{DD}	
V_{SSA}	Analog reference voltage		V_{SS}		V_{SS}	
f_{CPU}	Operating frequency	f_{OSC} = 12MHz			8	MHz
		f_{OSC} = 6MHz			4	
T_A	Ambient temperature range		0		70	°C

.

Figure 55. f_{CPU} Versus V_{DD} for standard voltage devices



12.3.2 Operating Conditions with Low Voltage Detector (LVD)

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A. Refer to Figure 15 on page 21.

Symbol	Parameter	Conditions	Min	Typ [1)]	Max	Unit
V_{IT+}	Low Voltage Reset Threshold (V_{DD} rising)	V_{DD} Max. Variation 50V/ms	3.6	3.8	3.95	V
V_{IT-}	Low Voltage Reset Threshold (V_{DD} falling)	V_{DD} Max. Variation 50V/ms	3.45	3.65	3.8	V
V_{hyst}	Hysteresis (V_{IT+} - V_{IT-})		120 [2)]	150 [2)]	180 [2)]	mV
Vt_{POR}	V_{DD} rise time rate [3)]		0.5		50	V/ms

Notes:
1. Not tested, guaranteed by design.
2. Not tested in production, guaranteed by characterization.
3. The V_{DD} rise time rate condition is needed to insure a correct device power-on and LVD reset. Not tested in production.

Figure 68. Typical V_{OL} vs. V_{DD} (standard port)

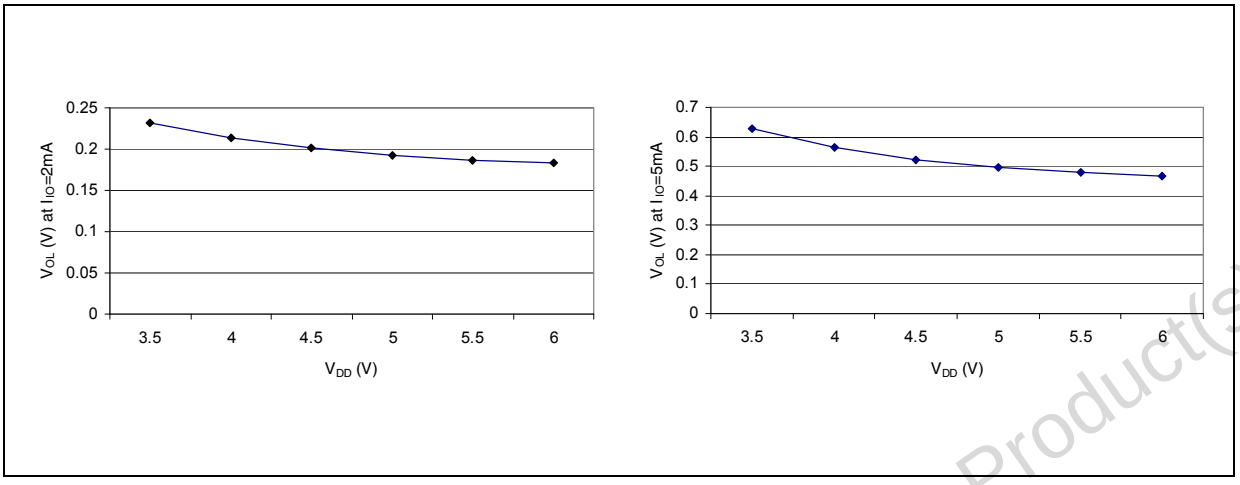


Figure 69. Typical V_{OL} vs. V_{DD} (high-sink port)

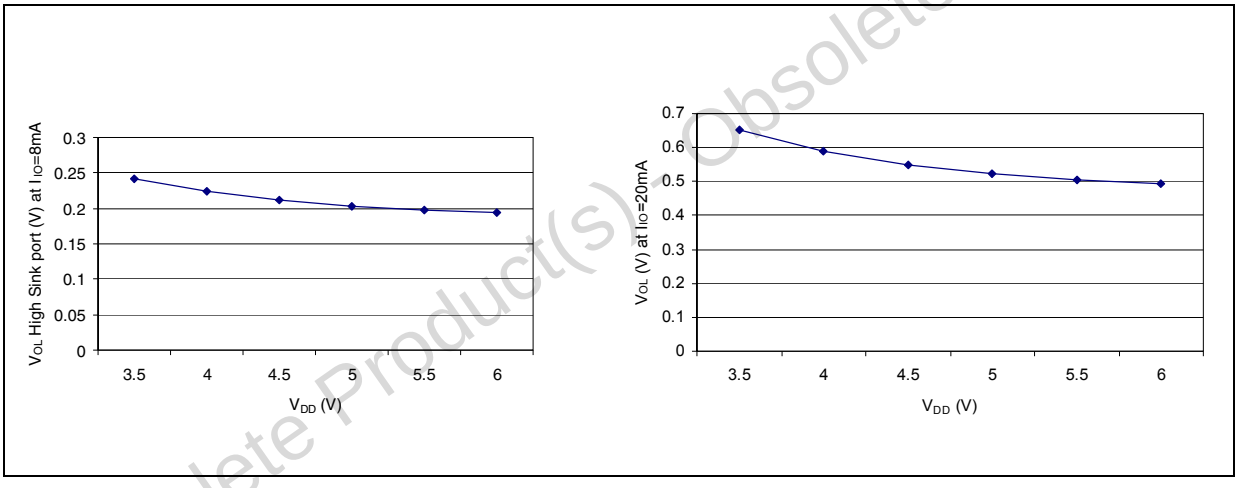


Figure 70. Typical V_{DD}-V_{OH} vs. V_{DD} (standard port)

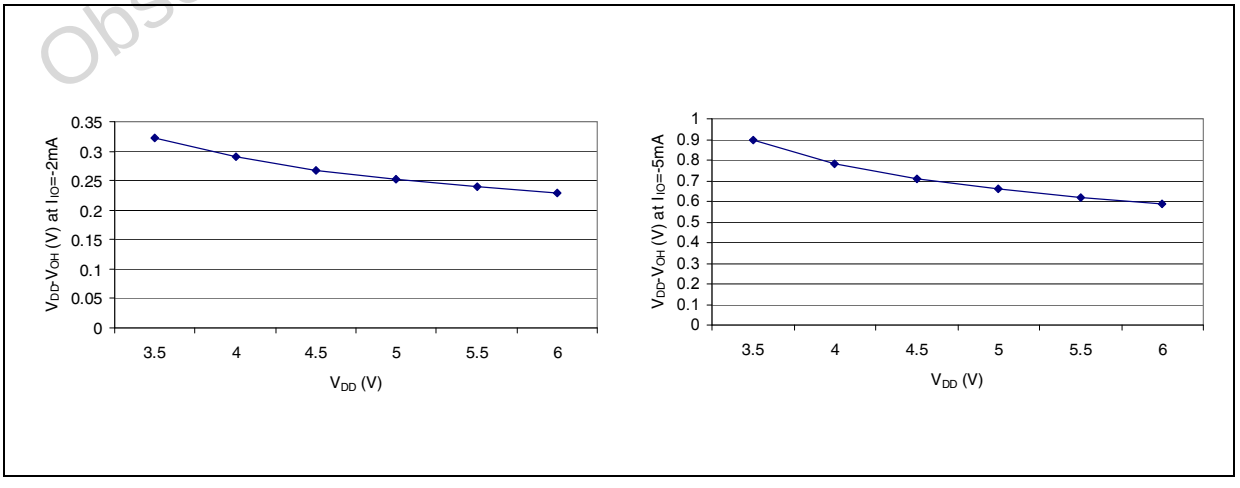
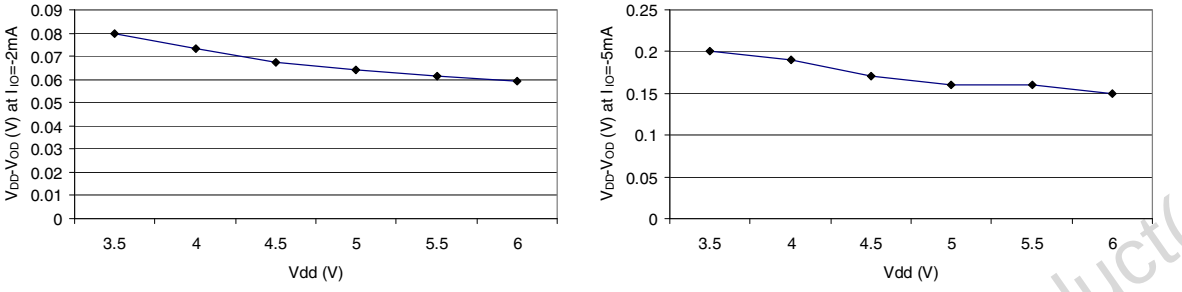


Figure 71. Typical V_{DD}-V_{OH} vs. V_{DD} (high sink port)



12.9 CONTROL PIN CHARACTERISTICS

12.9.1 Asynchronous $\overline{\text{RESET}}$ Pin

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{IH}	Input High Level Voltage			0.7xV_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage			V_{SS}		0.3xV_{DD}	V
V_{hys}	Schmitt trigger voltage hysteresis [3]				400		mV
V_{OL}	Output low level voltage [4] (see Figure 73, Figure 74)	V_{DD}=5V	I_{IO}=5mA			1 [2]	V
			I_{IO}=2mA			0.4 [2]	
R_{ON}	Weak pull-up equivalent resistor [5]	V_{IN}=V_{SS}			60		kΩ
$t_{w(RSTL)out}$	Generated reset pulse duration	External pin or internal reset sources			6 30		$1/f_{SFOSC}$ µs
$t_{h(RSTL)in}$	External reset pulse hold time [6]			10			µs

Notes:

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}=5V, not tested in production.
2. Data guaranteed by design.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The I_{IO} current sunk must always respect the absolute maximum rating specified in Section 12.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
5. The R_{ON} pull-up equivalent resistor is based on a resistive transistor (corresponding I_{ON} current characteristics described in Figure 72). This data is based on characterization results, not tested in production.
6. To guarantee the reset of the device, a minimum pulse has to be applied to $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.

Table 31. ST7 Application Notes

IDENTIFICATION	DESCRIPTION
AN1039	ST7 MATH UTILITY ROUTINES
AN1064	WRITING OPTIMIZED HIWARE C LANGUAGE FOR ST7
AN1071	HALF DUPLEX USB-TO-SERIAL BRIDGE USING THE ST72611 USB MICROCONTROLLER
AN1106	TRANSLATING ASSEMBLY CODE FROM HC05 TO ST7
AN1179	PROGRAMMING ST7 FLASH MICROCONTROLLERS IN REMOTE ISP MODE (IN-SITU PROGRAMMING)
AN1446	USING THE ST72521 EMULATOR TO DEBUG AN ST72324 TARGET APPLICATION
AN1477	EMULATED DATA EEPROM WITH XFLASH MEMORY
AN1478	PORTING AN ST7 PANTA PROJECT TO CODEWARRIOR IDE
AN1527	DEVELOPING A USB SMARTCARD READER WITH ST7SCR
AN1575	ON-BOARD PROGRAMMING METHODS FOR XFLASH AND HDFLASH ST7 MCUS
AN1576	IN-APPLICATION PROGRAMMING (IAP) DRIVERS FOR ST7 HDFLASH OR XFLASH MCUS
AN1577	DEVICE FIRMWARE UPGRADE (DFU) IMPLEMENTATION FOR ST7 USB APPLICATIONS
AN1601	SOFTWARE IMPLEMENTATION FOR ST7DALI-EVAL
AN1603	USING THE ST7 USB DEVICE FIRMWARE UPGRADE DEVELOPMENT KIT (DFU-DK)
AN1635	ST7 CUSTOMER ROM CODE RELEASE INFORMATION
AN1754	DATA LOGGING PROGRAM FOR TESTING ST7 APPLICATIONS VIA ICC
AN1796	FIELD UPDATES FOR FLASH BASED ST7 APPLICATIONS USING A PC COMM PORT
AN1900	HARDWARE IMPLEMENTATION FOR ST7DALI-EVAL
AN1904	ST7MC THREE-PHASE AC INDUCTION MOTOR CONTROL SOFTWARE LIBRARY
AN1905	ST7MC THREE-PHASE BLDC MOTOR CONTROL SOFTWARE LIBRARY
SYSTEM OPTIMIZATION	
AN1711	SOFTWARE TECHNIQUES FOR COMPENSATING ST7 ADC ERRORS
AN1827	IMPLEMENTATION OF SIGMA-DELTA ADC WITH ST7FLITE05/09
AN2009	PWM MANAGEMENT FOR 3-PHASE BLDC MOTOR DRIVES USING THE ST7FMC
AN2030	BACK EMF DETECTION DURING PWM ON TIME BY ST7MC

15.3 SCI WRONG BREAK DURATION

Description

A single break character is sent by setting and resetting the SBK bit in the SCICR2 register. In some cases, the break character may have a longer duration than expected:

– 20 bits instead of 10 bits if M=0

– 22 bits instead of 11 bits if M=1.

In the same way, as long as the SBK bit is set, break characters are sent to the TDO pin. This may lead to generate one break more than expected.

This affects all silicon revisions.

Occurrence

The occurrence of the problem is random and proportional to the baudrate. With a transmit frequency of 19200 baud (f_{CPU}=8MHz and SCIBRR=0xC9), the wrong break duration occurrence is around 1%.

Workaround

If this wrong duration is not compliant with the communication protocol in the application, software can request that an Idle line be generated before the break character. In this case, the break duration is always correct assuming the application is not doing anything between the idle and the break. This can be ensured by temporarily disabling interrupts.

The exact sequence is:

– Disable interrupts

– Reset and Set TE (IDLE request)

– Set and Reset SBK (Break Request)

– Re-enable interrupts

15.4 UNEXPECTED RESET FETCH

If an interrupt request occurs while a "POP CC" instruction is executed, the interrupt controller does not recognise the source of the interrupt and, by default, passes the RESET vector address to the CPU.

This affects all silicon revisions.

Workaround

To solve this issue, a "POP CC" instruction must always be preceded by a "SIM" instruction.

15.5 HALT MODE POWER CONSUMPTION WITH ADC ON

If the A/D converter is being used when Halt mode is entered, the power consumption in Halt Mode may exceed the maximum specified in the datasheet.

This affects all silicon revisions.

Workaround

Switch off the ADC by software (ADON=0) before executing a HALT instruction.

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