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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f621j4t1

3 REGISTER & MEMORY MAP

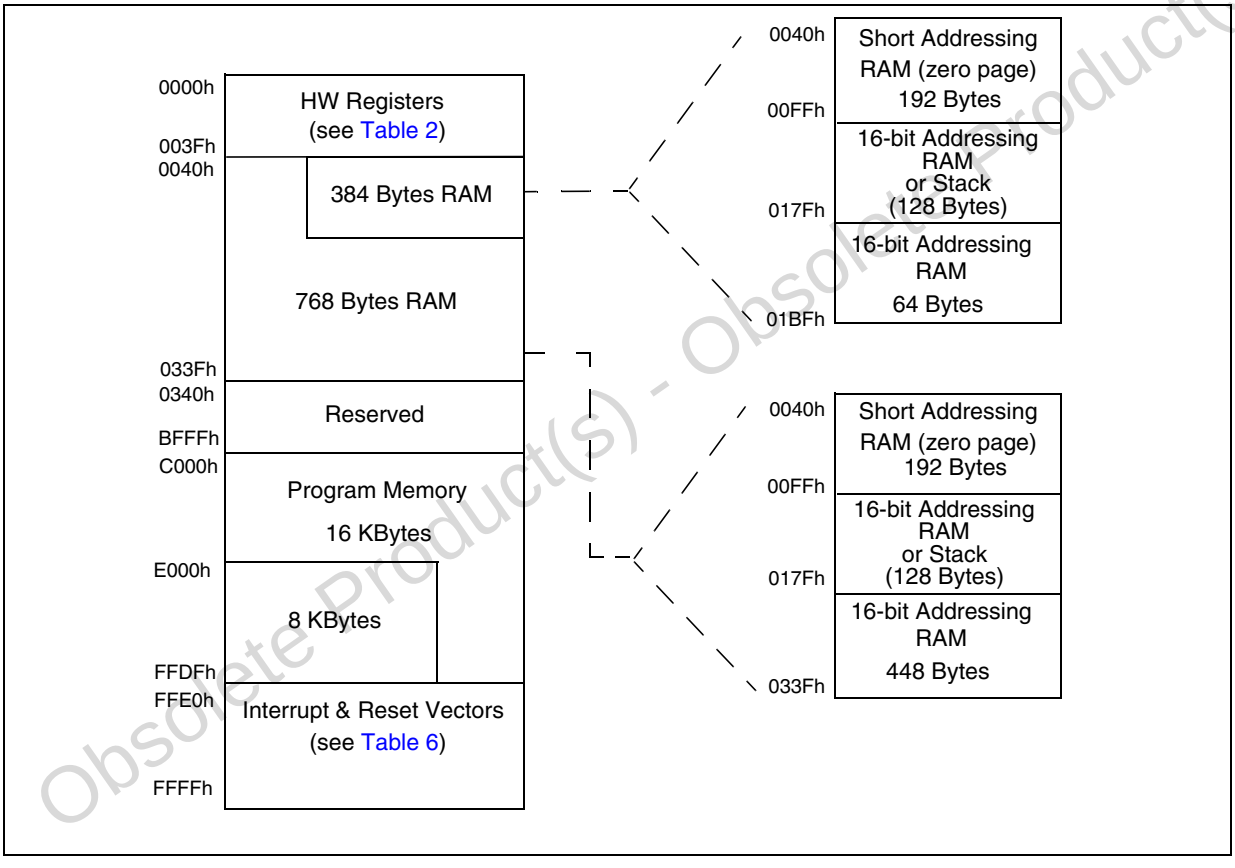
As shown in the Figure 7, the MCU is capable of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 64 bytes of register locations, 768 bytes of RAM and up to 16 Kbytes of user program memory. The RAM space includes up to 128 bytes for the stack from 0100h to 017Fh.

The highest address bytes contain the user reset and interrupt vectors.

IMPORTANT: Memory locations marked as “Reserved” must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 7. Memory Map



4 FLASH PROGRAM MEMORY

4.1 INTRODUCTION

The ST7 dual voltage High Density Flash (HDFlash) is a non-volatile memory that can be electrically erased as a single block or by individual sectors and programmed on a Byte-by-Byte basis using an external V_{PP} supply.

The HDFlash devices can be programmed and erased off-board (plugged in a programming tool) or on-board using ICP (In-Circuit Programming) or IAP (In-Application Programming).

The array matrix organisation allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 MAIN FEATURES

- 3 Flash programming modes:
  - Insertion in a programming tool. In this mode, all sectors including option bytes can be programmed or erased.
  - ICP (In-Circuit Programming). In this mode, all sectors including option bytes can be programmed or erased without removing the device from the application board.
  - IAP (In-Application Programming) In this mode, all sectors except Sector 0, can be programmed or erased without removing the device from the application board and while the application is running.
- ICT (In-Circuit Testing) for downloading and executing user application test patterns in RAM
- Read-out protection
- Register Access Security System (RASS) to prevent accidental programming or erasing

4.3 STRUCTURE

The Flash memory is organised in sectors and can be used for both code and data storage.

Depending on the overall Flash memory size in the microcontroller device, there are up to three user sectors (see Table 3). Each of these sectors can be erased independently to avoid unnecessary erasing of the whole Flash memory when only a partial erasing is required.

The first two sectors have a fixed size of 4 Kbytes (see Figure 8). They are mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

Table 3. Sectors available in Flash devices

Flash Size (bytes)	Available Sectors
4K	Sector 0
8K	Sectors 0,1
> 8K	Sectors 0,1, 2

4.3.1 Read-out Protection

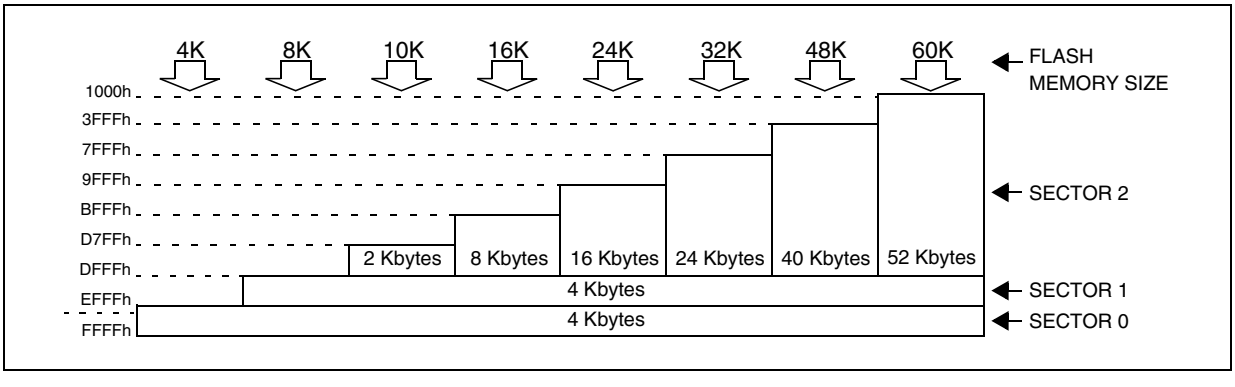
Read-out protection, when selected, provides a protection against Program Memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

In Flash devices, this protection is removed by reprogramming the option. In this case, the entire program memory is first automatically erased and the device can be reprogrammed.

Read-out protection selection depends on the device type:

- In Flash devices it is enabled and removed through the FMP_R bit in the option byte.
- In ROM devices it is enabled by mask option specified in the Option List.

Figure 8. Memory Map and Sector Address



FLASH PROGRAM MEMORY (Cont'd)

4.5 ICP (IN-CIRCUIT PROGRAMMING)

To perform ICP the microcontroller must be switched to ICC (In-Circuit Communication) mode by an external controller or programming tool.

Depending on the ICP code downloaded in RAM, Flash memory programming can be fully customized (number of bytes to program, program locations, or selection serial communication interface for downloading).

When using an STMicroelectronics or third-party programming tool that supports ICP and the specific microcontroller device, the user needs only to implement the ICP hardware interface on the application board (see Figure 9). For more details on the pin locations, refer to the device pinout description.

4.6 IAP (IN-APPLICATION PROGRAMMING)

This mode uses a BootLoader program previously stored in Sector 0 by the user (in ICP mode or by plugging the device in a programming tool).

This mode is fully controlled by user software. This allows it to be adapted to the user application, (user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored, etc.). For example, it is possible to download code from the SPI, SCI or other type of serial interface and program it in the Flash. IAP mode can be used to program any of the Flash sectors except Sector 0, which is write/erase protected to allow recovery in case errors occur during the programming operation.

4.7 RELATED DOCUMENTATION

For details on Flash programming and ICC protocol, refer to the *ST7 Flash Programming Reference Manual* and to the *ST7 ICC Protocol Reference Manual*.

4.8 REGISTER DESCRIPTION

FLASH CONTROL/STATUS REGISTER (FCSR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	0	0

This register is reserved for use by Programming Tool software. It controls the Flash programming and erasing operations.

5 CENTRAL PROCESSING UNIT

5.1 INTRODUCTION

This CPU has a full 8-bit architecture and contains six internal registers allowing efficient 8-bit data manipulation.

5.2 MAIN FEATURES

- Enable executing 63 basic instructions
- Fast 8-bit by 8-bit multiply
- 17 main addressing modes (with indirect addressing mode)
- Two 8-bit index registers
- 16-bit stack pointer
- Low power HALT and WAIT modes
- Priority maskable hardware interrupts
- Non-maskable software/hardware interrupts

5.3 CPU REGISTERS

The 6 CPU registers shown in Figure 10 are not present in the memory mapping and are accessed by specific instructions.

Accumulator (A)

The Accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations and to manipulate data.

Index Registers (X and Y)

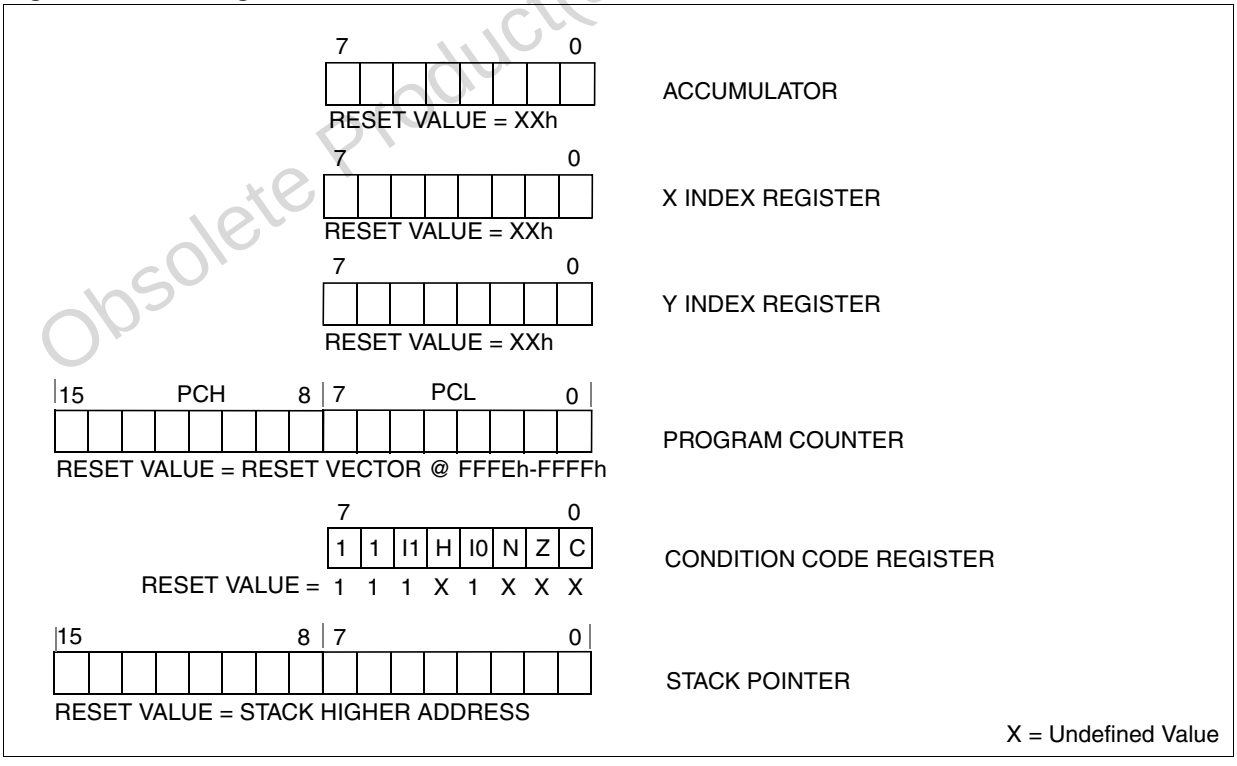
These 8-bit registers are used to create effective addresses or as temporary storage areas for data manipulation. (The Cross-Assembler generates a precede instruction (PRE) to indicate that the following instruction refers to the Y register.)

The Y register is not affected by the interrupt automatic procedures.

Program Counter (PC)

The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. It is made of two 8-bit registers PCL (Program Counter Low which is the LSB) and PCH (Program Counter High which is the MSB).

Figure 10. CPU Registers



9 I/O PORTS

9.1 INTRODUCTION

The I/O ports offer different functional modes:

transfer of data through digital inputs and outputs and for specific pins:

– Analog signal input (ADC)

– Alternate signal input/output for the on-chip peripherals.

– External interrupt generation

An I/O port is composed of up to 8 pins. Each pin can be programmed independently as digital input or digital output.

9.2 FUNCTIONAL DESCRIPTION

Each port is associated with 2 main registers:

– Data Register (DR)

– Data Direction Register (DDR)

Each I/O pin may be programmed using the corresponding register bits in DDR register: bit x corresponding to pin x of the port. The same correspondence is used for the DR register.

Table 8. I/O Pin Functions

DDR	MODE
0	Input
1	Output

9.2.1 Input Modes

The input configuration is selected by clearing the corresponding DDR register bit.

In this case, reading the DR register returns the digital value applied to the external I/O pin.

Notes:

1. All the inputs are triggered by a Schmitt trigger.
2. When switching from input mode to output mode, the DR register should be written first to output the correct value as soon as the port is configured as an output.

Interrupt function

When an external interrupt function of an I/O pin, is enabled using the ITFRE registers, an event on this I/O can generate an external Interrupt request to the CPU. The interrupt sensitivity is programmable, the options are given in the description of the ITRFRE interrupt registers.

Each pin can independently generate an Interrupt request.

Each external interrupt vector is linked to a dedicated group of I/O port pins (see Interrupts section). If more than one input pin is selected simultaneously as interrupt source, this is logically ANDed and inverted. For this reason, if an event occurs on one of the interrupt pins, it masks the other ones.

9.2.2 Output Mode

The pin is configured in output mode by setting the corresponding DDR register bit (see Table 7).

In this mode, writing “0” or “1” to the DR register applies this digital value to the I/O pin through the latch. Then reading the DR register returns the previously stored value.

Note: In this mode, the interrupt function is disabled.

9.2.3 Alternate Functions

Digital Alternate Functions

When an on-chip peripheral is configured to use a pin, the alternate function is automatically selected. This alternate function takes priority over standard I/O programming. When the signal is coming from an on-chip peripheral, the I/O pin is automatically configured in output mode (push-pull or open drain according to the peripheral).

When the signal is going to an on-chip peripheral, the I/O pin has to be configured in input mode. In this case, the pin state is also digitally readable by addressing the DR register.

Notes:

1. Input pull-up configuration can cause an unexpected value at the alternate peripheral input.
2. When the on-chip peripheral uses a pin as input and output, this pin must be configured as an input (DDR = 0).

***Warning*:** Alternate functions of peripherals must must not be activated when the external interrupts are enabled on the same pin, in order to avoid generating spurious interrupts.

I/O PORTS (Cont'd)

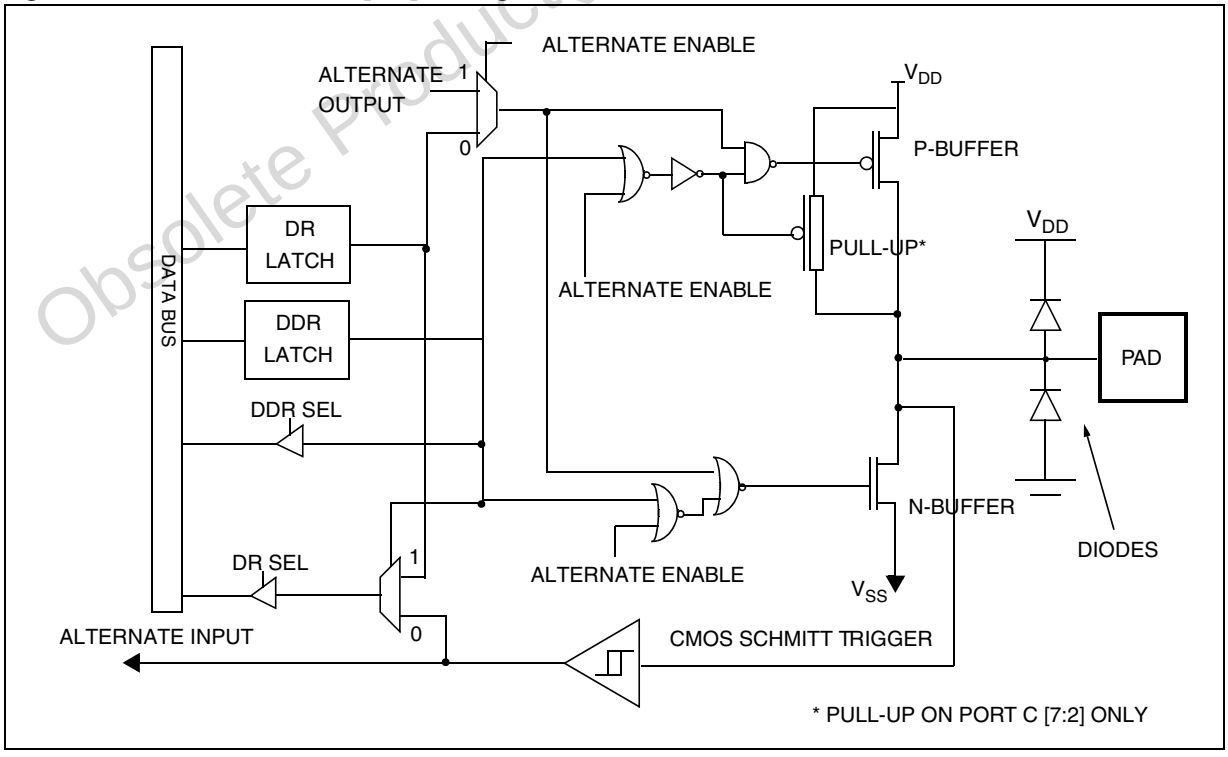
9.2.6 Port B

Table 10. Port B Description

PORT B	I/O		Alternate Function	
	Input*	Output	Signal	Condition
PB0	floating	push-pull (high sink)	MCO (Main Clock Output)	MCO = 1 (MISCR)
PB1	floating	push-pull (high sink)	RDI	SCI enabled
PB2	floating	push-pull (high sink)	TDO	TE = 1 (SCICR2)
PB3	floating	push-pull (high sink)	ARTCLK	EXCL = 1 (ARTCSR)
PB4	floating	push-pull (high sink)	ARTIC1	ART Timer enabled
			IT5 Schmitt triggered input	IT5E = 1 (ITRFRE1)
PB5	floating	push-pull (high sink)	ARTIC2	ART Timer enabled
			IT6 Schmitt triggered input	IT6E = 1 (ITRFRE1)
PB6	floating	push-pull (high sink)	PWM1	OE0 = 1 (PWMCR)
			IT7 Schmitt triggered input	IT7E = 1 (ITRFRE1)
PB7	floating	push-pull (high sink)	PWM2	OE1 = 1 (PWMCR)
			IT8 Schmitt triggered input	IT8E = 1 (ITRFRE1)

*Reset State

Figure 27. Port B and Port C [7:2] Configuration



I/O PORTS (Cont'd)

9.2.9 Register Description

DATA REGISTER (DR)

Port x Data Register
PxDR with x = A, B, C or D.

Read/Write

Reset Value: 0000 0000 (00h)

7							0
D7	D6	D5	D4	D3	D2	D1	D0

Bits 7:0 = **D[7:0]** *Data register 8 bits.*

The DR register has a specific behaviour according to the selected input/output configuration. Writing the DR register is always taken into account even if the pin is configured as an input; this allows to always have the expected level on the pin when toggling to output mode. Reading the DR register returns either the DR register latch content (pin configured as output) or the digital value applied to the I/O pin (pin configured as input).

DATA DIRECTION REGISTER (DDR)

Port x Data Direction Register
PxDDR with x = A, B, C or D.

Read/Write

Reset Value: 0000 0000 (00h)

7							0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

Bits 7:0 = **DD[7:0]** *Data direction register 8 bits.*

The DDR register gives the input/output direction configuration of the pins. Each bit is set and cleared by software.

0: Input mode
1: Output mode

9.3 MISCELLANEOUS REGISTER

MISCELLANEOUS REGISTER
Read Write
Reset Value - 0000 0000 (00h)

7							0
-	-	-	-	SMS1	SMS0	US-BOE	MCO

Bits 7:4 = Reserved

Bits 3:2 = **SMS[1:0]** *Slow Mode Selection*
These bits select the Slow Mode frequency (depending on the oscillator frequency configured by option byte).

OSC12/6	SMS1	SMS0	Slow Mode Frequency (MHz.)
f_{OSC}= 6 MHz.	0	0	4
	0	1	2
	1	0	1
	1	1	0.5
f_{OSC}= 12 MHz.	0	0	8
	0	1	4
	1	0	2
	1	1	1

Bit 1 = **USBOE** *USB Output Enable*
0: PA0 port free for general purpose I/O
1: USBOE alternate function enabled. The USB output enable signal is output on the PA0 port (at “1” when the ST7 USB is transmitting data).

Bit 0 = **MCO** *Main Clock Out*
0: PB0 port free for general purpose I/O
1: MCO alternate function enabled (f_{CPU} output on PB0 I/O port)

10.3 TIMEBASE UNIT (TBU)

10.3.1 Introduction

The Timebase unit (TBU) can be used to generate periodic interrupts.

10.3.2 Main Features

- 8-bit upcounter
- Programmable prescaler
- Period between interrupts: max. 8.1ms (at 8 MHz f_{CPU})
- Maskable interrupt
- Cascadable with PWM/ART TImer

10.3.3 Functional Description

The TBU operates as a free-running upcounter.

When the TCEN bit in the TBUCSR register is set by software, counting starts at the current value of the TBUCV register. The TBUCV register is incremented at the clock rate output from the prescaler selected by programming the PR[2:0] bits in the TBUCSR register.

When the counter rolls over from FFh to 00h, the OVF bit is set and an interrupt request is generated if ITE is set.

The user can write a value at any time in the TBUCV register.

If the cascading option is selected (CAS bit=1 in the TBUCSR register), the TBU and the ART TImer counters act together as a 16-bit counter. In this case, the TBUCV register is the high order byte, the ART counter (ARTCAR register) is the low order byte. Counting is clocked by the ART timer clock (Refer to the description of the ART Timer ARTCSR register).

10.3.4 Programming Example

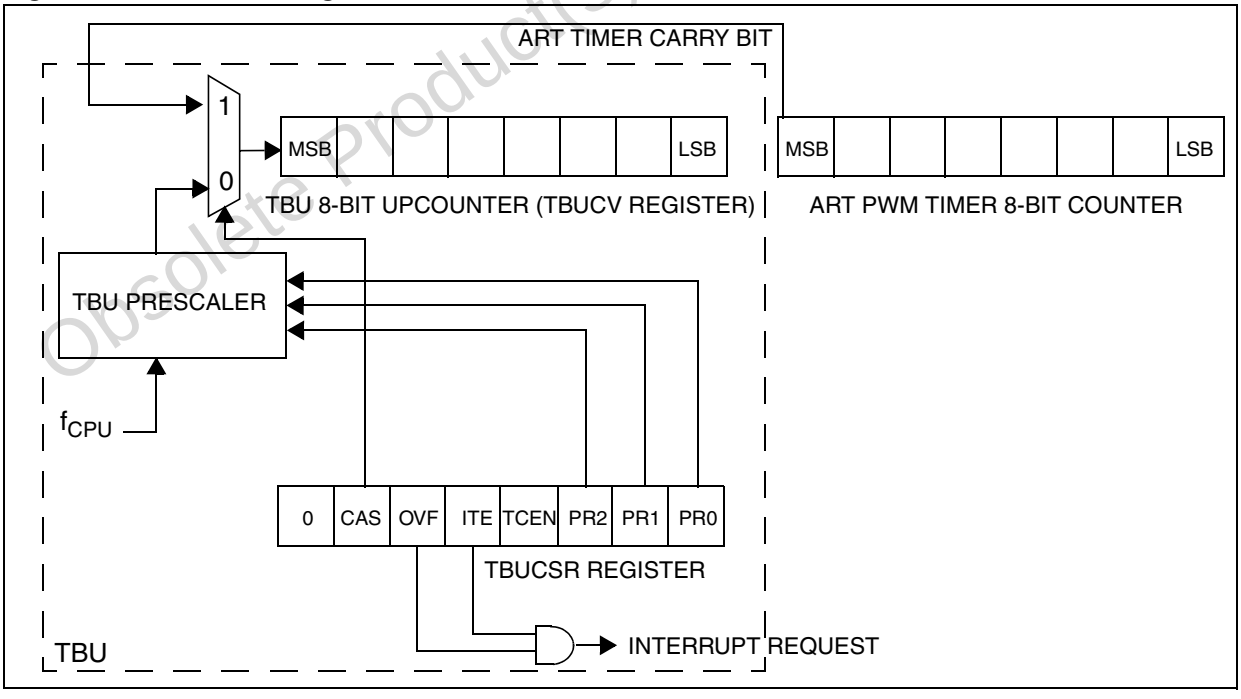
In this example, timer is required to generate an interrupt after a delay of 1 ms.

Assuming that f_{CPU} is 8 MHz and a prescaler division factor of 256 will be programmed using the PR[2:0] bits in the TBUCSR register, 1 ms = 32 TBU timer ticks.

In this case, the initial value to be loaded in the TBUCV must be (256-32) = 224 (E0h).

```
ld A, E0h
ld TBUCV, A   ; Initialize counter value
ld A 1Fh      ;
ld TBUCSR, A  ; Prescaler factor = 256,
              ; interrupt enable,
              ; TBU enable
```

Figure 38. TBU Block Diagram



TIMEBASE UNIT (Cont'd)

Table 17. TBU Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0036h	**TBUCV** Reset Value	CV7 0	CV6 0	CV5 0	CV4 0	CV3 0	CV2 0	CV1 0	CV0 0
0037h	**TBUSR** Reset Value	- 0	CAS 0	OVF 0	ITE 0	TCEN 0	PR2 0	PR1 0	PR0 0

10.5 SERIAL COMMUNICATIONS INTERFACE (SCI)

10.5.1 Introduction

The Serial Communications Interface (SCI) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The SCI offers a very wide range of baud rates using two baud rate generator systems.

10.5.2 Main Features

- Full duplex, asynchronous communications
- NRZ standard format (Mark/Space)
- Dual baud rate generator systems
- Independently programmable transmit and receive baud rates up to 500K baud
- Programmable data word length (8 or 9 bits)
- Receive buffer full, Transmit buffer empty and End of Transmission flags
- Two receiver wake-up modes:
  - Address bit (MSB)
  - Idle line
- Muting function for multiprocessor configurations
- Separate enable bits for Transmitter and Receiver
- Four error detection flags:
  - Overrun error
  - Noise error
  - Frame error
  - Parity error
- Five interrupt sources with flags:
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Idle line received
  - Overrun error detected
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Reduced power consumption mode

10.5.3 General Description

The interface is externally connected to another device by two pins (see Figure 47):

– TDO: Transmit Data Output. When the transmitter and the receiver are disabled, the output pin returns to its I/O port configuration. When the transmitter and/or the receiver are enabled and nothing is to be transmitted, the TDO pin is at high level.

– RDI: Receive Data Input is the serial data input. Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise.

Through these pins, serial data is transmitted and received as frames comprising:

– An Idle Line prior to transmission or reception

– A start bit

– A data word (8 or 9 bits) least significant bit first

– A Stop bit indicating that the frame is complete

This interface uses two types of baud rate generator:

– A conventional type for commonly-used baud rates

– An extended type with a prescaler offering a very wide range of baud rates even with non-standard oscillator frequencies

SERIAL COMMUNICATIONS INTERFACE (Cont'd)

10.5.4.2 Transmitter

The transmitter can send data words of either 8 or 9 bits depending on the M bit status. When the M bit is set, word length is 9 bits and the 9th bit (the MSB) has to be stored in the T8 bit in the SCICR1 register.

Character Transmission

During an SCI transmission, data shifts out least significant bit first on the TDO pin. In this mode, the SCIDR register consists of a buffer (TDR) between the internal bus and the transmit shift register (see Figure 46).

Procedure

– Select the M bit to define the word length.

– Select the desired baud rate using the SCIBRR and the SCIETPR registers.

– Set the TE bit to assign the TDO pin to the alternate function and to send a idle frame as first transmission.

– Access the SCISR register and write the data to send in the SCIDR register (this sequence clears the TDRE bit). Repeat this sequence for each data to be transmitted.

Clearing the TDRE bit is always performed by the following software sequence:

1. An access to the SCISR register

2. A write to the SCIDR register

The TDRE bit is set by hardware and it indicates:

– The TDR register is empty.

– The data transfer is beginning.

– The next data can be written in the SCIDR register without overwriting the previous data.

This flag generates an interrupt if the TIE bit is set and the I bit is cleared in the CC register.

When a transmission is taking place, a write instruction to the SCIDR register stores the data in the TDR register and which is copied in the shift register at the end of the current transmission.

When no transmission is taking place, a write instruction to the SCIDR register places the data directly in the shift register, the data transmission starts, and the TDRE bit is immediately set.

When a frame transmission is complete (after the stop bit) the TC bit is set and an interrupt is generated if the TCIE is set and the I bit is cleared in the CC register.

Clearing the TC bit is performed by the following software sequence:

1. An access to the SCISR register

2. A write to the SCIDR register

Note: The TDRE and TC bits are cleared by the same software sequence.

Break Characters

Setting the SBK bit loads the shift register with a break character. The break frame length depends on the M bit (see Figure 47).

As long as the SBK bit is set, the SCI send break frames to the TDO pin. After clearing this bit by software the SCI insert a logic 1 bit at the end of the last break frame to guarantee the recognition of the start bit of the next frame.

Idle Characters

Setting the TE bit drives the SCI to send an idle frame before the first data frame.

Clearing and then setting the TE bit during a transmission sends an idle frame after the current word.

Note: Resetting and setting the TE bit causes the data in the TDR register to be lost. Therefore the best time to toggle the TE bit is when the TDRE bit is set, that is, before writing the next byte in the SCIDR.

INSTRUCTION SET OVERVIEW (Cont'd)

Mnemo	Description	Function/Example	Dst	Src		I1	H	I0	N	Z	C
ADC	Add with Carry	A = A + M + C	A	M			H		N	Z	C
ADD	Addition	A = A + M	A	M			H		N	Z	C
AND	Logical And	A = A . M	A	M					N	Z	
BCP	Bit compare A, Memory	tst (A . M)	A	M					N	Z	
BRES	Bit Reset	bres Byte, #3	M								
BSET	Bit Set	bset Byte, #3	M								
BTJF	Jump if bit is false (0)	btjf Byte, #3, Jmp1	M								C
BTJT	Jump if bit is true (1)	btjt Byte, #3, Jmp1	M								C
CALL	Call subroutine										
CALLR	Call subroutine relative										
CLR	Clear		reg, M						0	1	
CP	Arithmetic Compare	tst(Reg - M)	reg	M					N	Z	C
CPL	One Complement	A = FFH-A	reg, M						N	Z	1
DEC	Decrement	dec Y	reg, M						N	Z	
HALT	Halt					1		0			
IRET	Interrupt routine return	Pop CC, A, X, PC				I1	H	I0	N	Z	C
INC	Increment	inc X	reg, M						N	Z	
JP	Absolute Jump	jp [TBL.w]									
JRA	Jump relative always										
JRT	Jump relative										
JRF	Never jump	jrf *									
JRIH	Jump if ext. INT pin = 1	(ext. INT pin high)									
JRIL	Jump if ext. INT pin = 0	(ext. INT pin low)									
JRH	Jump if H = 1	H = 1 ?									
JRNH	Jump if H = 0	H = 0 ?									
JRM	Jump if I1:0 = 11	I1:0 = 11 ?									
JRNM	Jump if I1:0 <> 11	I1:0 <> 11 ?									
JRMI	Jump if N = 1 (minus)	N = 1 ?									
JRPL	Jump if N = 0 (plus)	N = 0 ?									
JREQ	Jump if Z = 1 (equal)	Z = 1 ?									
JRNE	Jump if Z = 0 (not equal)	Z = 0 ?									
JRC	Jump if C = 1	C = 1 ?									
JRNC	Jump if C = 0	C = 0 ?									
JRULT	Jump if C = 1	Unsigned <									
JRUGE	Jump if C = 0	Jmp if unsigned >=									
JRUGT	Jump if (C + Z = 0)	Unsigned >									

12.2 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

12.2.1 Voltage Characteristics

Symbol	Ratings	Maximum value	Unit
V_{DD} - V_{SS}	Supply voltage	6.0	V
V_{DDA} - V_{SSA}	Analog Reference Voltage	6.0	
V_{IN} 1) & 2)	Input voltage on true open drain pin	V_{SS}-0.3 to 6.0	
	Input voltage on any other pin	V_{SS}-0.3 to V_{DD}+0.3	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	See “Electrostatic Discharge (ESD)” on page 109.	

12.2.2 Current Characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD}	Total current into V_{DD} power lines (source) 3)	80	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) 3)	80	
I_{IO}	Output current sunk by any standard I/O and control pin	25	
	Output current sunk by any high sink I/O pin	50	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ 2) & 4)	Injected current on V_{PP} pin	75	
	Injected current on $\overline{RESET}$ pin	± 5	
	Injected current on OSCIN and OSCOUT pins	± 5	
	Injected current on PA0 to PA6 pins	± 5	
	Injected current on PA7 pin	+ 5	
	Injected current on any other pin 5) & 6)	± 5	
$\Sigma I_{INJ(PIN)}$ 2)	Total injected current (sum of all I/O and control pins) 5)	± 20	

Notes:

1. Directly connecting the $\overline{RESET}$ and I/O pins to V_{DD} or V_{SS} could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7kΩ for $\overline{RESET}$, 10kΩ for I/Os). Unused I/O pins must be tied in the same way to V_{DD} or V_{SS} according to their reset configuration.

2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

3. All power (V_{DD}) and ground (V_{SS}) lines must always be connected to the external supply.

4. Negative injection disturbs the analog performance of the device. In particular, it induces leakage currents throughout the device including the analog inputs. To avoid undesirable effects on the analog functions, care must be taken:
- Analog input pins must have a negative injection less than 0.8 mA (assuming that the impedance of the analog voltage is lower than the specified limits)
- Pure digital pins must have a negative injection less than 1.6mA. In addition, it is recommended to inject the current as far as possible from the analog input pins.

5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

6. True open drain I/O port pins do not accept positive injection.

Figure 75. $\overline{\text{RESET}}$ pin protection when LVD is enabled.[1)2)3)4)]

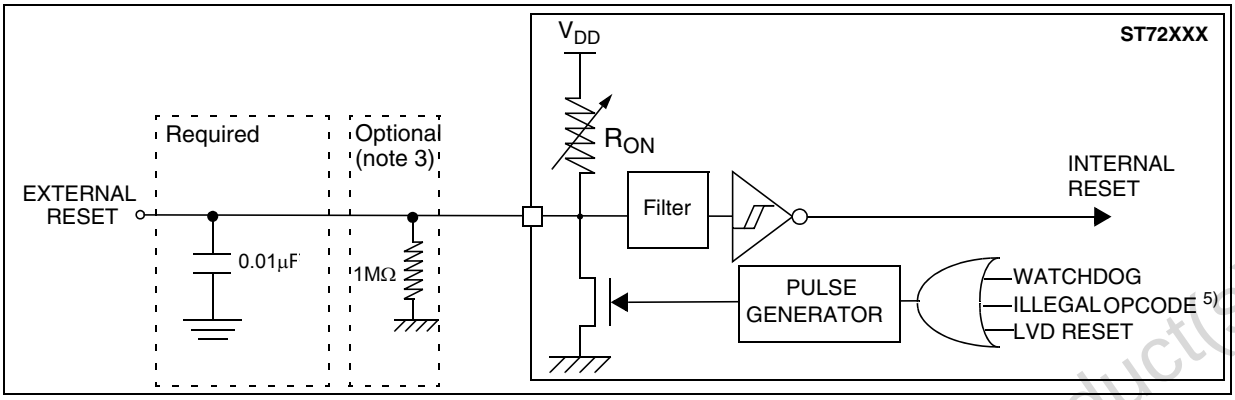
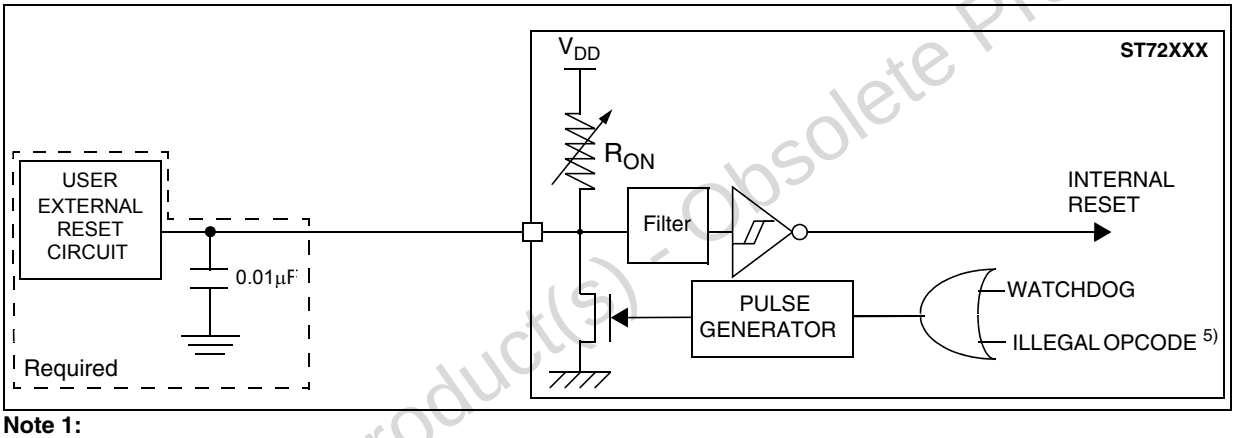


Figure 76. $\overline{\text{RESET}}$ pin protection when LVD is disabled.[1)]



Note 1:

- The reset network protects the device against parasitic resets.
- The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).
- Whatever the reset source is (internal or external), the user must ensure that the level on the $\overline{\text{RESET}}$ pin can go below the V_{IL} max. level specified in section 12.9.1 on page 113. Otherwise the reset will not be taken into account internally.
- Because the reset circuit is designed to allow the internal RESET to be output in the $\overline{\text{RESET}}$ pin, the user must ensure that the current sunk on the $\overline{\text{RESET}}$ pin is less than the absolute maximum value specified for $I_{INJ(RESET)}$ in section 12.2.2 on page 102.

Note 2: When the LVD is enabled, it is recommended not to connect a pull-up resistor or capacitor. A 10nF pull-down capacitor is required to filter noise on the reset line.

Note 3: In case a capacitive power supply is used, it is recommended to connect a 1MΩ pull-down resistor to the $\overline{\text{RESET}}$ pin to discharge any residual voltage induced by the capacitive effect of the power supply (this will add 5µA to the power consumption of the MCU).

Note 4: Tips when using the LVD:

- 1. Check that all recommendations related to the reset circuit have been applied (see notes above).
- 2. Check that the power supply is properly decoupled (100nF + 10µF close to the MCU). Refer to AN1709 and AN2017. If this cannot be done, it is recommended to put a 100nF + 1MΩ pull-down on the $\overline{\text{RESET}}$ pin.
- 3. The capacitors connected on the RESET pin and also the power supply are key to avoid any start-up marginality. In most cases, steps 1 and 2 above are sufficient for a robust solution. Otherwise: replace 10nF pull-down on the $\overline{\text{RESET}}$ pin with a 5µF to 20µF capacitor."

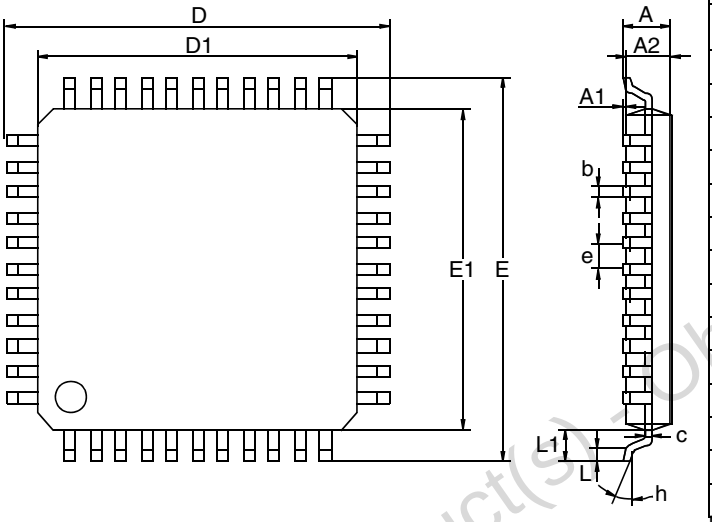
13 PACKAGE CHARACTERISTICS

In order to meet environmental requirements, ST offers this device in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

13.1 PACKAGE MECHANICAL DATA

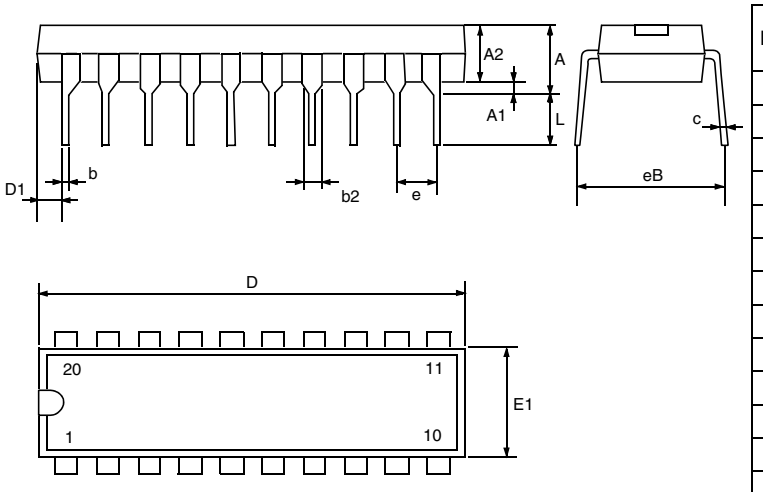
Figure 86. 44-Pin Low Profile Quad Flat Package (10x10)



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.30	0.37	0.45	0.0118	0.0146	0.0177
C	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.80			0.0315	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of Pins					
N	44					

Note 1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 91. 20-Pin Plastic Dual In-Line Package, 300-mil Width



Dim.	mm			inches[1)]		
	Min	Typ	Max	Min	Typ	Max
A			5.33			0.2098
A1	0.38			0.0150		
A2	2.92	3.30	4.95	0.1150	0.1299	0.1949
b	0.36	0.46	0.56	0.0142	0.0181	0.0220
b2	1.14	1.52	1.78	0.0449	0.0598	0.0701
c	0.20	0.25	0.36	0.0079	0.0098	0.0142
D	24.89	26.16	26.92	0.9799	1.0299	1.0598
D1	0.13			0.0051		
e		2.54			0.1000	
eB			10.92			0.4299
E1	6.10	6.35	7.11	0.2402	0.2500	0.2799
L	2.92	3.30	3.81	0.1150	0.1299	0.1500
	Number of Pins					
N	20					

Note 1. Values in inches are converted from mm and rounded to 4 decimal digits.

14 DEVICE CONFIGURATION AND ORDERING INFORMATION

Each device is available for production in user programmable versions (FLASH) as well as in factory coded versions (ROM).

ST7262 devices are ROM versions.

ST72F62 FLASH devices are shipped to customers with a default content (FFh). This implies that FLASH devices have to be configured by the customer using the Option Byte while the ROM devices are factory-configured.

14.1 OPTION BYTE

The Option Byte allows the hardware configuration of the microcontroller to be selected.
The Option Byte has no address in the memory map and can be accessed only in programming mode using a standard ST7 programming tool. The default content of the FLASH is fixed to FFh. This means that all the options have “1” as their default value.

7							0
-	-	WDG SW	NEST	LVD	-	OSC 12/6	FMP_ R

Bits 7:6 = Reserved.

Bit 5 = **WDGSW** *Hardware or software watchdog*
This option bit selects the watchdog type.
0: Hardware enabled
1: Software enabled

Bit 4 = **NEST**
This option bit selects the nested interrupts feature.
0: Nested interrupt feature disabled
1: Nested interrupt feature enabled

Bit 3 = **LVD** *Low Voltage Detector selection*
This option bit selects the LVD.
0: LVD enabled
1: LVD disabled

Bit 2= Reserved.

Bit 1 = **OSC12/6** *Oscillator selection*
This option bit selects the clock divider used to drive the USB interface at 6MHz.
0: 6 MHz oscillator (no divider for USB)
1: 12 Mhz oscillator (2 divider for USB)

Bit 0 = **FMP_R** *Memory Readout Protection*
Readout protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Erasing the option bytes when the FMP_R option is selected will cause the whole memory to be erased first and the device can be reprogrammed. Refer to the ST7 Flash Programming Reference Manual and section 4.3.1 on page 14 for more details.
0: Read-out protection enabled
1: Read-out protection disabled

14.2 DEVICE ORDERING INFORMATION AND TRANSFER OF CUSTOMER CODE

Customer code is made up of the ROM contents and the list of the selected options (if any). The ROM contents are to be sent on diskette, or by electronic means, with the hexadecimal file in .S19 format generated by the development tool. All unused bytes must be set to FFh.

The selected options are communicated to STMicroelectronics using the correctly completed OPTION LIST appended.
Refer to application note AN1635 for information on the counter listing returned by ST after code has been transferred.
The STMicroelectronics Sales Organization will be pleased to provide detailed information on contractual points.

ST7262 MICROCONTROLLER OPTION LIST
(Last update: March 2006)

Customer: . . . . . .
Address: . . . . . .
. . . . . .
Contact: . . . . . .
Phone No: . . . . . .
Reference/ROM Code* : . . . . . .
*The ROM code name is assigned by STMicroelectronics.
ROM code must be sent in .S19 format. .Hex extension cannot be processed.

Device Type/Memory Size/Package (check only one option):

ROM DEVICE:	8K	16K
SDIP20:	[ ] ST72623F2B1	
SO20:	[ ] ST72623F2M1	
SDIP32:		[ ] ST72621K4B1
SO34:	[ ] ST72622L2M1	[ ] ST72621L4M1
SDIP42:		[ ] ST72621J4B1
LQFP44:		[ ] ST72621J4T1

DIE FORM:	8K	16K
20-pin:	[ ]	
32-pin:	[ ]	[ ]
34-pin:	[ ]	[ ]
42-pin:	[ ]	[ ]
44-pin:	[ ]	[ ]

Conditioning (check only one option):

Packaged Product (do not specify for DIP package)		Die Product (dice tested at 25°C only)
[ ] Tape & Reel	[ ] Tray (LQFP package only)	[ ] Tape & Reel
	[ ] Tube (SO package only)	[ ] Inked wafer
		[ ] Sawn wafer on sticky foil

Special Marking: [ ] No [ ] Yes "_ _ _ _ _ _ _ _ _ _ "
Authorized characters are letters, digits, '.', '-', '/' and spaces only.
Max character count: S020 (8 char. max) : _ _ _ _ _ _ _ _ S034 (13 char. max) : _ _ _ _ _ _ _ _ _ _ _ _ _
DIP20/DIP32/LQFP44 (10 char. max) : _ _ _ _ _ _ _ _ _ _ DIP42 (16 char. max) : _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _

Watchdog Selection:	[ ] Software activation	[ ] Hardware activation
Nested Interrupt:	[ ] Enabled	[ ] Disabled
LVD Reset :	[ ] Disabled	[ ] Enabled
Oscillator Selection :	[ ] 6 MHz.	[ ] 12 MHz.
Readout protection:	[ ] Enabled	[ ] Disabled

Date . . . . . Signature . . . . . .

Please download the latest version of this option list from:
http://www.st.com/mcu > downloads > ST7 microcontrollers > Option list

15.3 SCI WRONG BREAK DURATION

Description

A single break character is sent by setting and resetting the SBK bit in the SCICR2 register. In some cases, the break character may have a longer duration than expected:

– 20 bits instead of 10 bits if M=0

– 22 bits instead of 11 bits if M=1.

In the same way, as long as the SBK bit is set, break characters are sent to the TDO pin. This may lead to generate one break more than expected.

This affects all silicon revisions.

Occurrence

The occurrence of the problem is random and proportional to the baudrate. With a transmit frequency of 19200 baud (f_{CPU}=8MHz and SCIBRR=0xC9), the wrong break duration occurrence is around 1%.

Workaround

If this wrong duration is not compliant with the communication protocol in the application, software can request that an Idle line be generated before the break character. In this case, the break duration is always correct assuming the application is not doing anything between the idle and the break. This can be ensured by temporarily disabling interrupts.

The exact sequence is:

– Disable interrupts

– Reset and Set TE (IDLE request)

– Set and Reset SBK (Break Request)

– Re-enable interrupts

15.4 UNEXPECTED RESET FETCH

If an interrupt request occurs while a "POP CC" instruction is executed, the interrupt controller does not recognise the source of the interrupt and, by default, passes the RESET vector address to the CPU.

This affects all silicon revisions.

Workaround

To solve this issue, a "POP CC" instruction must always be preceded by a "SIM" instruction.

15.5 HALT MODE POWER CONSUMPTION WITH ADC ON

If the A/D converter is being used when Halt mode is entered, the power consumption in Halt Mode may exceed the maximum specified in the datasheet.

This affects all silicon revisions.

Workaround

Switch off the ADC by software (ADON=0) before executing a HALT instruction.