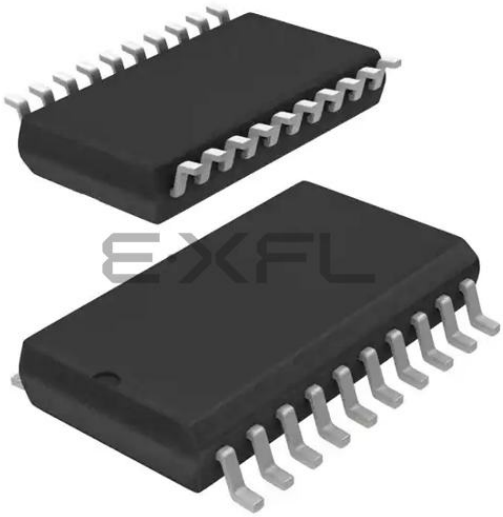

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

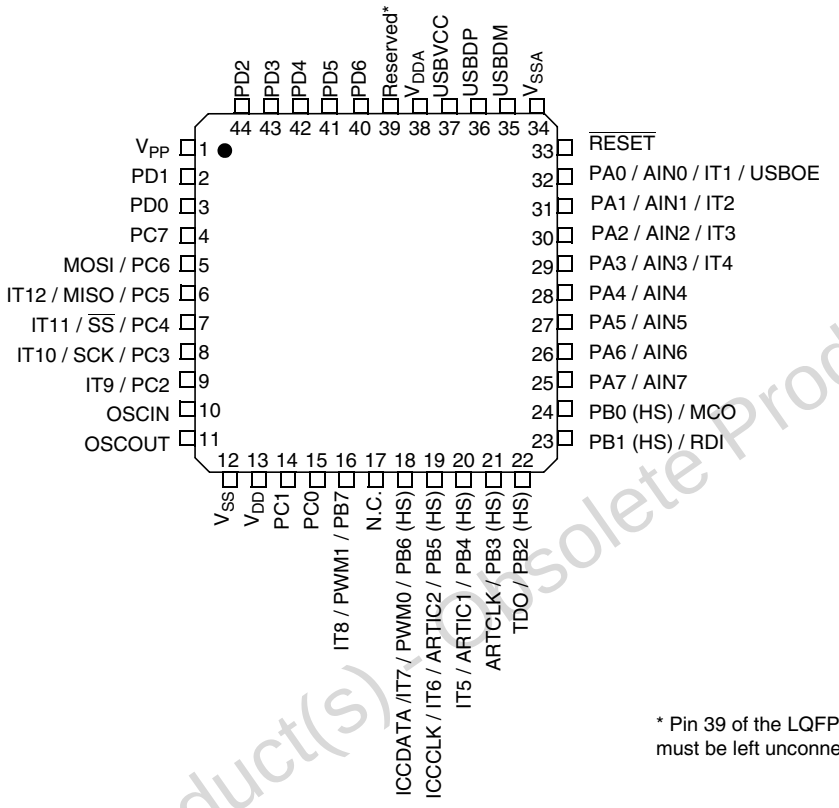
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ST7 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 11 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 384 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 3x10b |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 20-SO |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/st72f623f2m1tr |

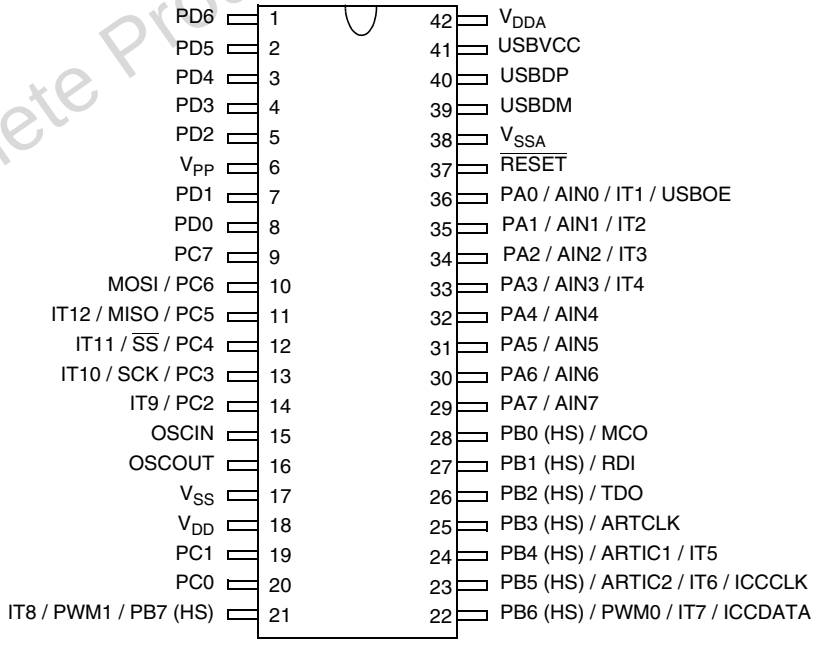
# Table of Contents

# 2 PIN DESCRIPTION

**Figure 2. 44-pin LQFP and 42-Pin SDIP Package Pinouts**




* Pin 39 of the LQFP44 package must be left unconnected.



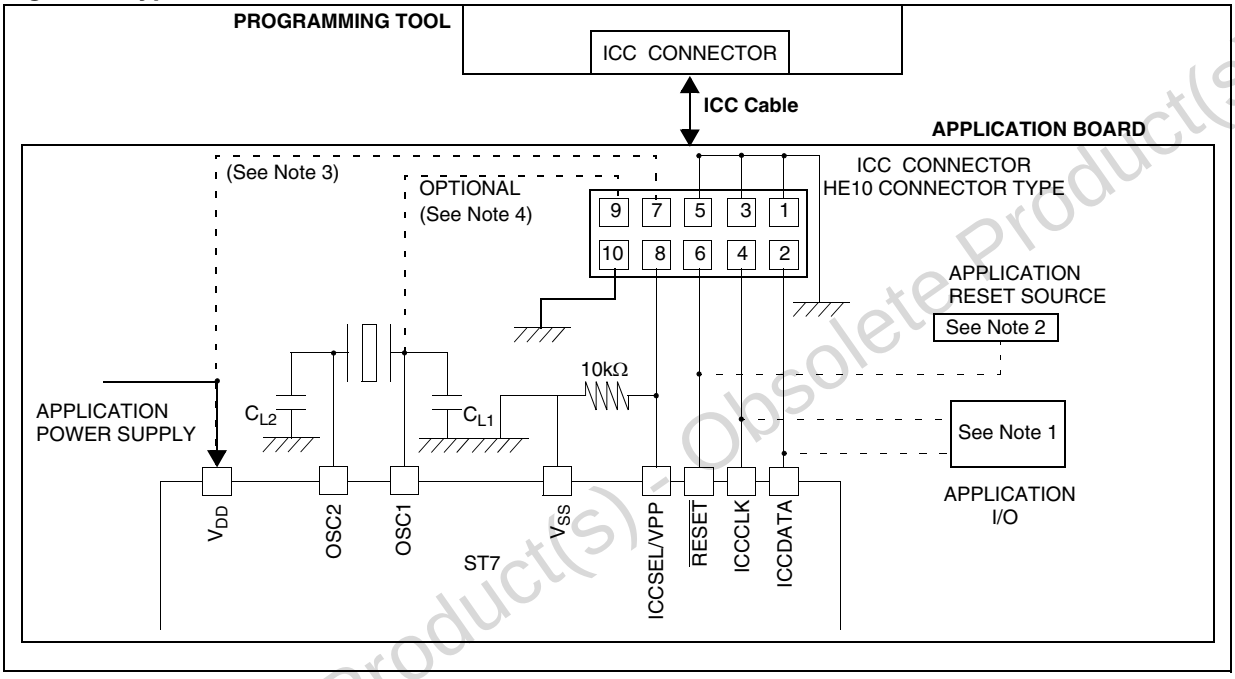
**FLASH PROGRAM MEMORY** (Cont'd)

### 4.4 ICC INTERFACE

ICC (In-Circuit Communication) needs a minimum of four and up to six pins to be connected to the programming tool (see Figure 9). These pins are:

- $\overline{\text{RESET}}$: device reset
- $V_{SS}$: device power supply ground
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input/output serial data pin
- ICCSEL/$V_{PP}$: programming voltage
- OSC1(or OSCIN): main clock input for external source (optional)
- $V_{DD}$: application board power supply (see Figure 9, Note 3)

**Figure 9. Typical ICC Interface**






**Notes:**

1. If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the Programming Tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to implemented in case another device forces the signal. Refer to the Programming Tool documentation for recommended resistor values.

2. During the ICC session, the programming tool must control the $\overline{\text{RESET}}$ pin. This can lead to conflicts between the programming tool and the application reset circuit if it drives more than 5mA at high level (push pull output or pull-up resistor<1K). A schottky diode can be used to isolate the application RESET circuit in this case. When using a classical RC network with R > 1K or a reset management IC with open drain output and pull-up resistor > 1K, no additional components are needed. In all cases the user must ensure that no external reset is generated by the application during the ICC session.

3. The use of Pin 7 of the ICC connector depends on the Programming Tool architecture. This pin must be connected when using most ST Programming Tools (it is used to monitor the application power supply). Please refer to the Programming Tool manual.

4. Pin 9 has to be connected to the OSC1 or OSCIN pin of the ST7 when the clock is not available in the application or if the selected clock option is not programmed in the option byte. ST7 devices with multioscillator capability need to have OSC2 grounded in this case.

**FLASH PROGRAM MEMORY** (Cont'd)

### 4.5 ICP (IN-CIRCUIT PROGRAMMING)

To perform ICP the microcontroller must be switched to ICC (In-Circuit Communication) mode by an external controller or programming tool.

Depending on the ICP code downloaded in RAM, Flash memory programming can be fully customized (number of bytes to program, program locations, or selection serial communication interface for downloading).

When using an STMicroelectronics or third-party programming tool that supports ICP and the specific microcontroller device, the user needs only to implement the ICP hardware interface on the application board (see Figure 9). For more details on the pin locations, refer to the device pinout description.

### 4.6 IAP (IN-APPLICATION PROGRAMMING)

This mode uses a BootLoader program previously stored in Sector 0 by the user (in ICP mode or by plugging the device in a programming tool).

This mode is fully controlled by user software. This allows it to be adapted to the user application, (user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored, etc.). For example, it is possible to download code from the SPI, SCI or other type of serial interface and program it in the Flash. IAP mode can be used to program any of the Flash sectors except Sector 0, which is write/erase protected to allow recovery in case errors occur during the programming operation.

### 4.7 RELATED DOCUMENTATION

For details on Flash programming and ICC protocol, refer to the *ST7 Flash Programming Reference Manual* and to the *ST7 ICC Protocol Reference Manual*.

### 4.8 REGISTER DESCRIPTION

**FLASH CONTROL/STATUS REGISTER (FCSR)**

Read/Write

Reset Value: 0000 0000 (00h)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register is reserved for use by Programming Tool software. It controls the Flash programming and erasing operations.

**CENTRAL PROCESSING UNIT** (Cont'd)

**Condition Code Register (CC)**

Read/Write

Reset Value: 111x1xxx

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | I1 | H | I0 | N | Z | C |

The 8-bit Condition Code register contains the interrupt masks and four flags representative of the result of the instruction just executed. This register can also be handled by the PUSH and POP instructions.

These bits can be individually tested and/or controlled by specific instructions.

**Arithmetic Management Bits**

Bit 4 = **H** *Half carry*.

This bit is set by hardware when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instructions. It is reset by hardware during the same instructions.

0: No half carry has occurred.
1: A half carry has occurred.

This bit is tested using the JRH or JRNH instruction. The H bit is useful in BCD arithmetic subroutines.

Bit 2 = **N** *Negative*.

This bit is set and cleared by hardware. It is representative of the result sign of the last arithmetic, logical or data manipulation. It's a copy of the result $7^{th}$ bit.
0: The result of the last operation is positive or null.
1: The result of the last operation is negative (i.e. the most significant bit is a logic 1).

This bit is accessed by the JRMI and JRPL instructions.

Bit 1 = **Z** *Zero*.

This bit is set and cleared by hardware. This bit indicates that the result of the last arithmetic, logical or data manipulation is zero.
0: The result of the last operation is different from zero.
1: The result of the last operation is zero.

This bit is accessed by the JREQ and JRNE test instructions.

Bit 0 = **C** *Carry/borrow.*

This bit is set and cleared by hardware and software. It indicates an overflow or an underflow has occurred during the last arithmetic operation.
0: No overflow or underflow has occurred.
1: An overflow or underflow has occurred.

This bit is driven by the SCF and RCF instructions and tested by the JRC and JRNC instructions. It is also affected by the "bit test and branch", shift and rotate instructions.

**Interrupt Management Bits**

Bit 5,3 = **I1, I0** *Interrupt*

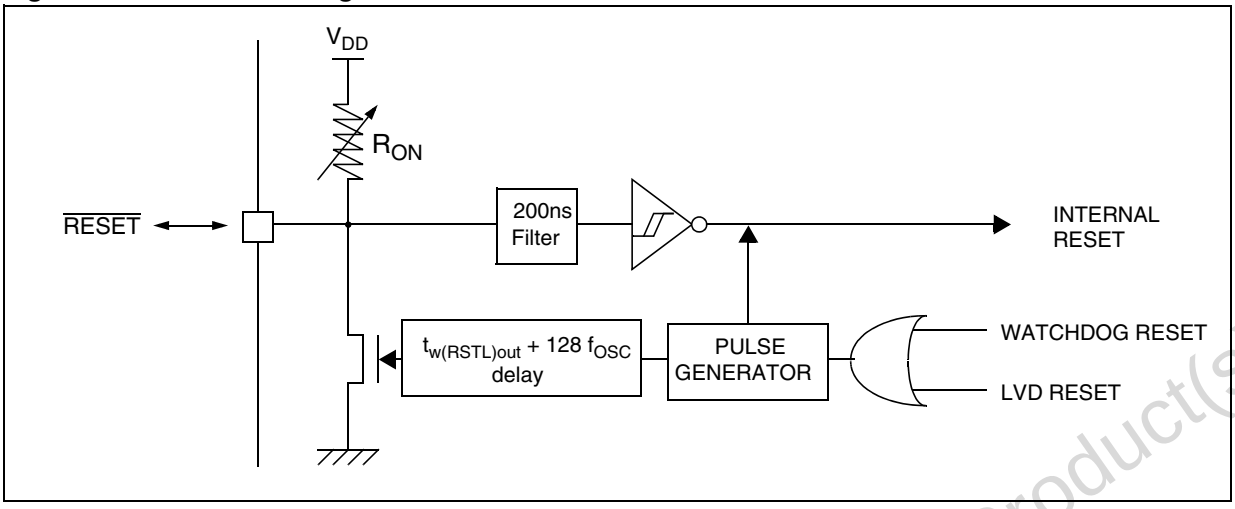
The combination of the I1 and I0 bits gives the current interrupt software priority.

| Interrupt Software Priority | I1 | I0 |
|---|---|---|
| Level 0 (main) | 1 | 0 |
| Level 1 | 0 | 1 |
| Level 2 | 0 | 0 |
| Level 3 (= interrupt disable) | 1 | 1 |

These two bits are set/cleared by hardware when entering in interrupt. The loaded value is given by the corresponding bits in the interrupt software priority registers (IxSPR). They can be also set/cleared by software with the RIM, SIM, IRET, HALT, WFI and PUSH/POP instructions.

See the interrupt management chapter for more details.

**Figure 19. Reset Block Diagram**




**Note:** The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).

**INTERRUPTS** (Cont'd)

**Table 6. Interrupt Mapping**

| N° | Source Block | Description | Register Label | Priority Order | Exit from HALT | Address Vector |
|---|---|---|---|---|---|---|
| | | Reset | | Highest Priority | Yes | FFFEh-FFFFh |
| | | TRAP software interrupt | | | No | FFFCh-FFFDh |
| 0 | ICP | FLASH Start programming NMI interrupt | | | Yes | FFFAh-FFFBh |
| 1 | USB | USB End Suspend interrupt | USBISTR | | Yes | FFF8h-FFF9h |
| 2 | I/O Ports | Port A external interrupts IT[4:1] | ITRFRE1 | | Yes | FFF6h-FFF7h |
| 3 | | Port B external interrupts IT[8:5] | ITRFRE1 | | Yes | FFF4h-FFF5h |
| 4 | | Port C external interrupts IT[12:9] | ITRFRE2 | | Yes | FFF2h-FFF3h |
| 5 | TBU | Timebase Unit interrupt | TBUCSR | | No | FFF0h-FFF1h |
| 6 | ART | ART/PWM Timer interrupt | ICCSR | | Yes | FFEEh-FFEFh |
| 7 | SPI | SPI interrupt vector | SPISR | | Yes | FFECh-FFEDh |
| 8 | SCI | SCI interrupt vector | SCISR | | No | FFEAh-FFEBh |
| 9 | USB | USB interrupt vector | USBISTR | Lowest Priority | No | FFE8h-FFE9h |
| 10 | ADC | A/D End of conversion interrupt | ADCCSR | | No | FFE6h-FFE7h |
| Reserved area | | | | | | FFE0h-FFE5h |

**Table 7. Nested Interrupts Register Map and Reset Values**

| Address (Hex.) | Register Label | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0032h | | Ext. Interrupt Port B | | Ext. Interrupt Port A | | USB END SUSP | | Not Used | |
| | **ISPR0** Reset Value | I1_3 1 | I0_3 1 | I1_2 1 | I0_2 1 | I1_1 1 | I0_1 1 | 1 | 1 |
| 0033h | | SPI | | ART | | TBU | | Ext. Interrupt Port C | |
| | **ISPR1** Reset Value | I1_7 1 | I0_7 1 | I1_6 1 | I0_6 1 | I1_5 1 | I0_5 1 | I1_4 1 | I0_4 1 |
| 0034h | | Not Used | | ADC | | USB | | SCI | |
| | **ISPR2** Reset Value | I1_11 1 | I0_11 1 | I1_10 1 | I0_10 1 | I1_9 1 | I0_9 1 | I1_8 1 | I0_8 1 |
| 0035h | | | | | | Not Used | | Not Used | |
| | **ISPR3** Reset Value | 1 | 1 | 1 | 1 | I1_13 1 | I0_13 1 | I1_12 1 | I0_12 1 |

# 9 I/O PORTS

## 9.1 INTRODUCTION

The I/O ports offer different functional modes:

transfer of data through digital inputs and outputs and for specific pins:

– Analog signal input (ADC)

– Alternate signal input/output for the on-chip peripherals.

– External interrupt generation

An I/O port is composed of up to 8 pins. Each pin can be programmed independently as digital input or digital output.

## 9.2 FUNCTIONAL DESCRIPTION

Each port is associated with 2 main registers:

– Data Register (DR)

– Data Direction Register (DDR)

Each I/O pin may be programmed using the corresponding register bits in DDR register: bit x corresponding to pin x of the port. The same correspondence is used for the DR register.

**Table 8. I/O Pin Functions**

| DDR | MODE |
|---|---|
| 0 | Input |
| 1 | Output |

### 9.2.1 Input Modes

The input configuration is selected by clearing the corresponding DDR register bit.

In this case, reading the DR register returns the digital value applied to the external I/O pin.

**Notes**:

1. All the inputs are triggered by a Schmitt trigger.
2. When switching from input mode to output mode, the DR register should be written first to output the correct value as soon as the port is configured as an output.

**Interrupt function**

When an external interrupt function of an I/O pin, is enabled using the ITFRE registers, an event on this I/O can generate an external Interrupt request to the CPU. The interrupt sensitivity is programmable, the options are given in the description of the ITRFRE interrupt registers.

Each pin can independently generate an Interrupt request.

Each external interrupt vector is linked to a dedicated group of I/O port pins (see Interrupts section). If more than one input pin is selected simultaneously as interrupt source, this is logically ANDed and inverted. For this reason, if an event occurs on one of the interrupt pins, it masks the other ones.

### 9.2.2 Output Mode

The pin is configured in output mode by setting the corresponding DDR register bit (see Table 7).

In this mode, writing “0” or “1” to the DR register applies this digital value to the I/O pin through the latch. Then reading the DR register returns the previously stored value.

**Note**: In this mode, the interrupt function is disabled.

### 9.2.3 Alternate Functions

**Digital Alternate Functions**

When an on-chip peripheral is configured to use a pin, the alternate function is automatically selected. This alternate function takes priority over standard I/O programming. When the signal is coming from an on-chip peripheral, the I/O pin is automatically configured in output mode (push-pull or open drain according to the peripheral).

When the signal is going to an on-chip peripheral, the I/O pin has to be configured in input mode. In this case, the pin state is also digitally readable by addressing the DR register.

**Notes:**

1. Input pull-up configuration can cause an unexpected value at the alternate peripheral input.
2. When the on-chip peripheral uses a pin as input and output, this pin must be configured as an input (DDR = 0).

***Warning*:** Alternate functions of peripherals must must not be activated when the external interrupts are enabled on the same pin, in order to avoid generating spurious interrupts.

**Table 19. SPI Register Map and Reset Values**

| Address (Hex.) | Register Label | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0011h | **SPIDR** Reset Value | MSB x | x | x | x | x | x | x | LSB x |
| 0012h | **SPICR** Reset Value | SPIE 0 | SPE 0 | SPR2 0 | MSTR 0 | CPOL x | CPHA x | SPR1 x | SPR0 x |
| 0013h | **SPICSR** Reset Value | SPIF 0 | WCOL 0 | OVR 0 | MODF 0 | 0 | SOD 0 | SSM 0 | SSI 0 |

**SERIAL COMMUNICATIONS INTERFACE** (Cont'd)

### 10.5.4 Functional Description

The block diagram of the Serial Control Interface, is shown in Figure 46 It contains six dedicated registers:

– Two control registers (SCICR1 & SCICR2)

– A status register (SCISR)

– A baud rate register (SCIBRR)

– An extended prescaler receiver register (SCIERPR)

– An extended prescaler transmitter register (SCIETPR)

Refer to the register descriptions in Section 10.5.7for the definitions of each bit.

#### 10.5.4.1 Serial Data Format

Word length may be selected as being either 8 or 9 bits by programming the M bit in the SCICR1 register (see Figure 46).

The TDO pin is in low state during the start bit.

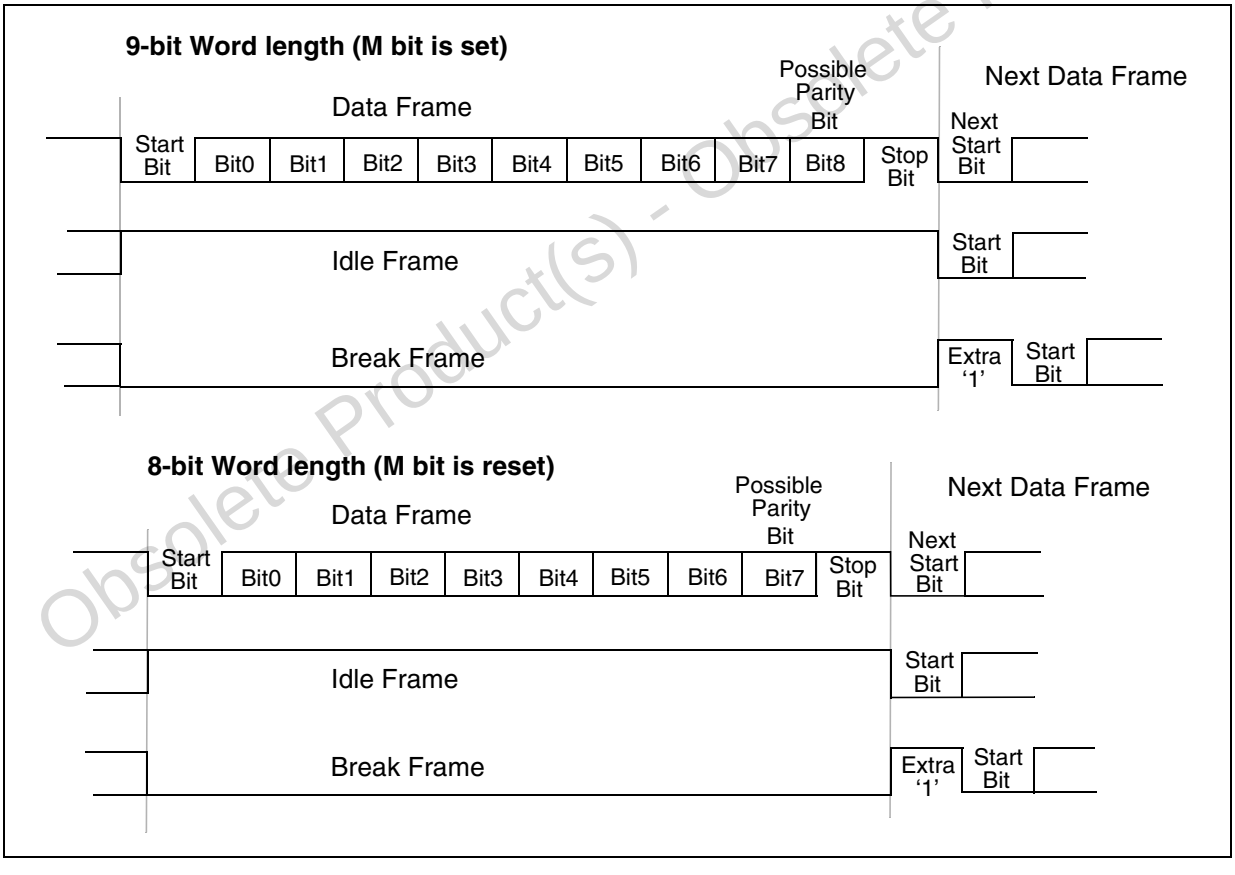
The TDO pin is in high state during the stop bit.

An Idle character is interpreted as an entire frame of "1"s followed by the start bit of the next frame which contains data.

A Break character is interpreted on receiving "0"s for some multiple of the frame period. At the end of the last break frame the transmitter inserts an extra "1" bit to acknowledge the start bit.

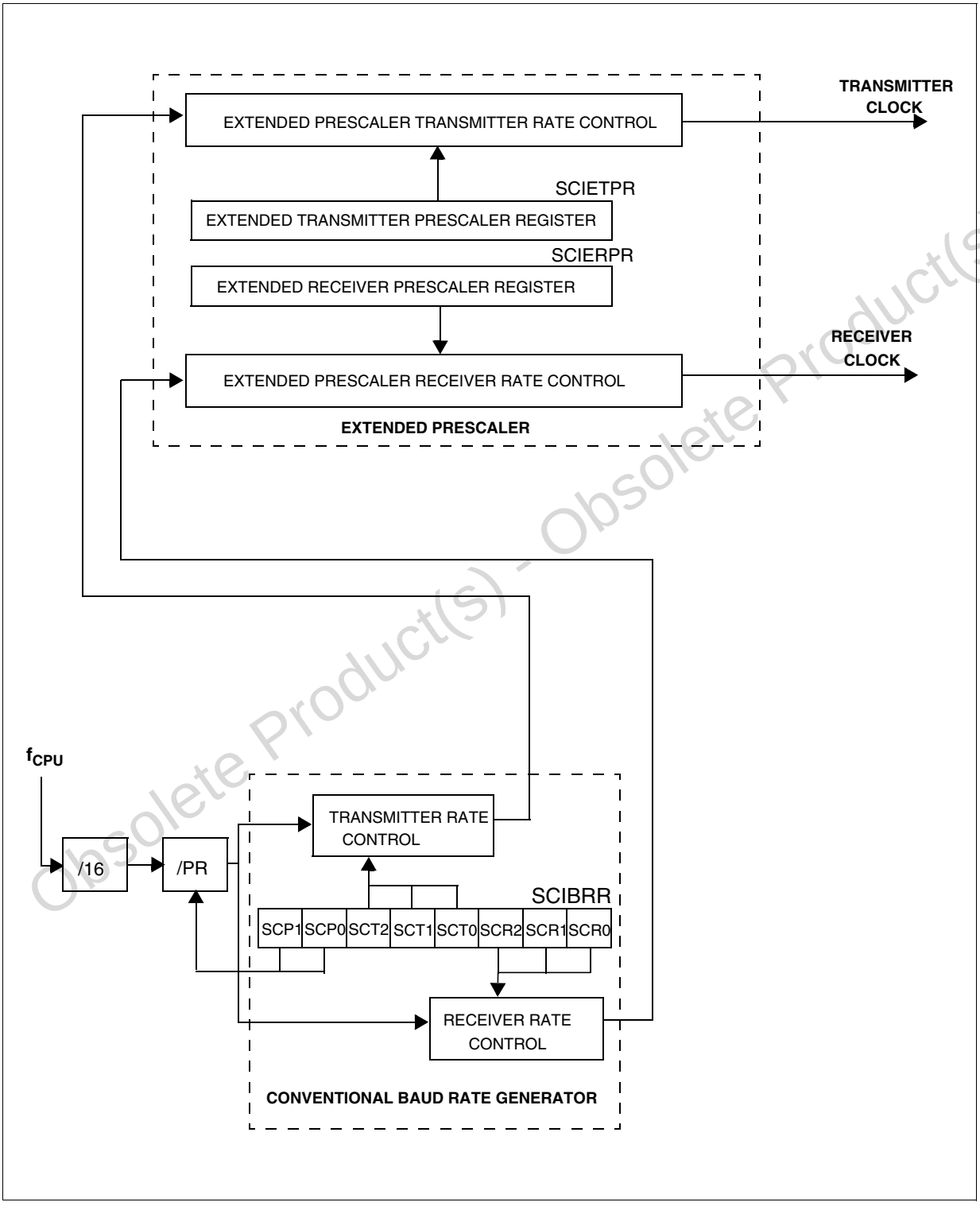
Transmission and reception are driven by their own baud rate generator.

**Figure 47. Word Length Programming**



**SERIAL COMMUNICATIONS INTERFACE** (Cont'd)

**Figure 48. SCI Baud Rate and Extended Prescaler Block Diagram**



**SERIAL COMMUNICATIONS INTERFACE** (Cont'd)

### EXTENDED RECEIVE PRESCALER DIVISION REGISTER (SCIERPR)

Read/Write

Reset Value: 0000 0000 (00h)

Allows setting of the Extended Prescaler rate division factor for the receive circuit.

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| ERPR 7 | ERPR 6 | ERPR 5 | ERPR 4 | ERPR 3 | ERPR 2 | ERPR 1 | ERPR 0 |

Bits 7:0 = **ERPR[7:0]** *8-bit Extended Receive Prescaler Register.*

The extended Baud Rate Generator is activated when a value different from 00h is stored in this register. Therefore the clock frequency issued from the 16 divider (see Figure 48) is divided by the binary factor set in the SCIERPR register (in the range 1 to 255).

The extended baud rate generator is not used after a reset.

### EXTENDED TRANSMIT PRESCALER DIVISION REGISTER (SCIETPR)

Read/Write

Reset Value:0000 0000 (00h)

Allows setting of the External Prescaler rate division factor for the transmit circuit.

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| ETPR 7 | ETPR 6 | ETPR 5 | ETPR 4 | ETPR 3 | ETPR 2 | ETPR 1 | ETPR 0 |

Bits 7:0 = **ETPR[7:0]** *8-bit Extended Transmit Prescaler Register.*

The extended Baud Rate Generator is activated when a value different from 00h is stored in this register. Therefore the clock frequency issued from the 16 divider (see Figure 48) is divided by the binary factor set in the SCIETPR register (in the range 1 to 255).

The extended baud rate generator is not used after a reset.

**Table 21. Baudrate Selection**

| Symbol | Parameter | Conditions | | | Standard | Baud Rate | Unit |
|---|---|---|---|---|---|---|---|
| | | $f_{CPU}$ | Accuracy vs Standard | Prescaler | | | |
| $f_{Tx}$<br>$f_{Rx}$ | Communication frequency | 8 MHz | ~0.16% | Conventional Mode<br>TR (or RR)=128, PR=13<br>TR (or RR)= 32, PR=13<br>TR (or RR)= 16, PR=13<br>TR (or RR)= 8, PR=13<br>TR (or RR)= 4, PR=13<br>TR (or RR)= 16, PR= 3<br>TR (or RR)= 2, PR=13<br>TR (or RR)= 1, PR=13 | <br>300<br>1200<br>2400<br>4800<br>9600<br>10400<br>19200<br>38400 | <br>~300.48<br>~1201.92<br>~2403.84<br>~4807.69<br>~9615.38<br>~10416.67<br>~19230.77<br>~38461.54 | Hz |
| | | | ~0.79% | Extended Mode<br>ETPR (or ERPR) = 35,<br>TR (or RR)= 1, PR=1 | 14400 | ~14285.71 | |

**USB INTERFACE** (Cont'd)

**DEVICE ADDRESS REGISTER (DADDR)**

Read / Write

Reset Value: 0000 0000 (00h)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| 0 | ADD6 | ADD5 | ADD4 | ADD3 | ADD2 | ADD1 | ADD0 |

Bit 7 = Reserved. Forced by hardware to 0.

Bits 6:0 = **ADD[6:0]** *Device address, 7 bits.*

Software must write into this register the address sent by the host during enumeration.

**Note:** This register is also reset when a USB reset is received from the USB bus or forced through bit FRES in the CTLR register.

**ENDPOINT n REGISTER A (EPnRA)**

Read / Write

Reset Value: 0000 xxxx (0xh)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| ST_ OUT | DTOG _TX | STAT _TX1 | STAT _TX0 | TBC 3 | TBC 2 | TBC 1 | TBC 0 |

These registers (**EP0RA**, **EP1RA** and **EP2RA**) are used for controlling data transmission. They are also reset by the USB bus reset.

**Note**: Endpoint 2 and the EP2RA register are not available on some devices (see device feature list and register map).

Bit 7 = **ST_OUT** *Status out.*
This bit is set by software to indicate that a status out packet is expected: in this case, all nonzero OUT data transfers on the endpoint are STALLed instead of being ACKed. When ST_OUT is reset, OUT transactions can have any number of bytes, as needed.

Bit 6 = **DTOG_TX** *Data Toggle, for transmission transfers.*
It contains the required value of the toggle bit (0=DATA0, 1=DATA1) for the next transmitted data packet. This bit is set by hardware at the reception of a SETUP PID. DTOG_TX toggles only when the transmitter has received the ACK signal from the USB host. DTOG_TX and also DTOG_RX (see EPnRB) are normally updated by hardware, at the receipt of a relevant PID. They can be also written by software.

Bits 5:4 = **STAT_TX[1:0]** *Status bits, for transmission transfers.*
These bits contain the information about the endpoint status, which are listed below:

| STAT_TX1 | STAT_TX0 | Meaning |
|---|---|---|
| 0 | 0 | **DISABLED:** transmission transfers cannot be executed. |
| 0 | 1 | **STALL**: the endpoint is stalled and all transmission requests result in a STALL handshake. |
| 1 | 0 | **NAK**: the endpoint is naked and all transmission requests result in a NAK handshake. |
| 1 | 1 | **VALID**: this endpoint is enabled for transmission. |

These bits are written by software. Hardware sets the STAT_TX bits to NAK when a correct transfer has occurred (CTR=1) related to a IN or SETUP transaction addressed to this endpoint; this allows the software to prepare the next set of data to be transmitted.

Bits 3:0 = **TBC[3:0]** *Transmit byte count for Endpoint n.*
Before transmission, after filling the transmit buffer, software must write in the TBC field the transmit packet size expressed in bytes (in the range 0-8).

**Warning:** Any value outside the range 0-8 will induce undesired effects (such as continuous data transmission).

## 11.2 INSTRUCTION GROUPS

The ST7 family devices use an Instruction Set consisting of 63 instructions. The instructions may be subdivided into 13 main groups as illustrated in the following table:

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Load and Transfer | LD | CLR | | | | | | |
| Stack operation | PUSH | POP | RSP | | | | | |
| Increment/Decrement | INC | DEC | | | | | | |
| Compare and Tests | CP | TNZ | BCP | | | | | |
| Logical operations | AND | OR | XOR | CPL | NEG | | | |
| Bit Operation | BSET | BRES | | | | | | |
| Conditional Bit Test and Branch | BTJT | BTJF | | | | | | |
| Arithmetic operations | ADC | ADD | SUB | SBC | MUL | | | |
| Shift and Rotates | SLL | SRL | SRA | RLC | RRC | SWAP | SLA | |
| Unconditional Jump or Call | JRA | JRT | JRF | JP | CALL | CALLR | NOP | RET |
| Conditional Branch | JRxx | | | | | | | |
| Interruption management | TRAP | WFI | HALT | IRET | | | | |
| Condition Code Flag modification | SIM | RIM | SCF | RCF | | | | |

### Using a prebyte

The instructions are described with one to four opcodes.

In order to extend the number of available opcodes for an 8-bit CPU (256 opcodes), three different prebyte opcodes are defined. These prebytes modify the meaning of the instruction they precede.

The whole instruction becomes:

PC-2 End of previous instruction

PC-1 Prebyte

PC Opcode

PC+1 Additional word (0 to 2) according to the number of bytes required to compute the effective address

These prebytes enable instruction in Y as well as indirect addressing modes to be implemented. They precede the opcode of the instruction in X or the instruction using direct addressing mode. The prebytes are:

PDY 90 Replace an X based instruction using immediate, direct, indexed, or inherent addressing mode by a Y one.

PIX 92 Replace an instruction using direct, direct bit, or direct relative addressing mode to an instruction using the corresponding indirect addressing mode.
It also changes an instruction using X indexed addressing mode to an instruction using indirect X indexed addressing mode.

PIY 91 Replace an instruction using X indirect indexed addressing mode by a Y one.

## 12.2 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### 12.2.1 Voltage Characteristics

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| $V_{DD}$ - $V_{SS}$ | Supply voltage | 6.0 | V |
| $V_{DDA}$ - $V_{SSA}$ | Analog Reference Voltage | 6.0 | |
| $V_{IN}$ 1) & 2) | Input voltage on true open drain pin | $V_{SS}$-0.3 to 6.0 | |
| | Input voltage on any other pin | $V_{SS}$-0.3 to $V_{DD}$+0.3 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (Human Body Model) | See “Electrostatic Discharge (ESD)” on page 109. | |

### 12.2.2 Current Characteristics

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}$ power lines (source) 3) | 80 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground lines (sink) 3) | 80 | |
| $I_{IO}$ | Output current sunk by any standard I/O and control pin | 25 | |
| | Output current sunk by any high sink I/O pin | 50 | |
| | Output current source by any I/Os and control pin | - 25 | |
| $I_{INJ(PIN)}$ 2) & 4) | Injected current on $V_{PP}$ pin | 75 | |
| | Injected current on $\overline{RESET}$ pin | ± 5 | |
| | Injected current on OSCIN and OSCOUT pins | ± 5 | |
| | Injected current on PA0 to PA6 pins | ± 5 | |
| | Injected current on PA7 pin | + 5 | |
| | Injected current on any other pin 5) & 6) | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ 2) | Total injected current (sum of all I/O and control pins) 5) | ± 20 | |

**Notes:**

1. Directly connecting the $\overline{RESET}$ and I/O pins to $V_{DD}$ or $V_{SS}$ could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7kΩ for $\overline{RESET}$, 10kΩ for I/Os). Unused I/O pins must be tied in the same way to $V_{DD}$ or $V_{SS}$ according to their reset configuration.

2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding $V_{IN}$ maximum must always be respected

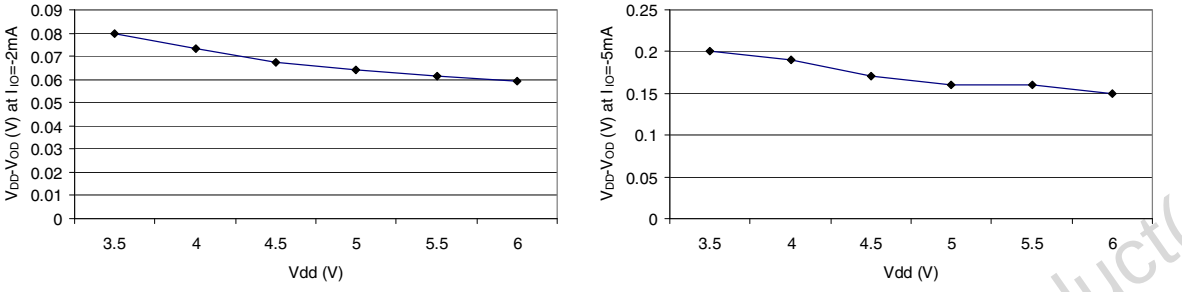
3. All power ($V_{DD}$) and ground ($V_{SS}$) lines must always be connected to the external supply.

4. Negative injection disturbs the analog performance of the device. In particular, it induces leakage currents throughout the device including the analog inputs. To avoid undesirable effects on the analog functions, care must be taken:
- Analog input pins must have a negative injection less than 0.8 mA (assuming that the impedance of the analog voltage is lower than the specified limits)
- Pure digital pins must have a negative injection less than 1.6mA. In addition, it is recommended to inject the current as far as possible from the analog input pins.

5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

6. True open drain I/O port pins do not accept positive injection.

**Figure 71. Typical $V_{DD}$-$V_{OH}$ vs. $V_{DD}$ (high sink port)**




## 12.9 CONTROL PIN CHARACTERISTICS

### 12.9.1 Asynchronous $\overline{\text{RESET}}$ Pin

Subject to general operating conditions for $V_{DD}$, $f_{CPU}$, and $T_A$ unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ [1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Level Voltage | | | 0.7x$V_{DD}$ | | $V_{DD}$ | V |
| $V_{IL}$ | Input Low Voltage | | | $V_{SS}$ | | 0.3x$V_{DD}$ | V |
| $V_{hys}$ | Schmitt trigger voltage hysteresis [3] | | | | 400 | | mV |
| $V_{OL}$ | Output low level voltage [4] (see Figure 73, Figure 74) | $V_{DD}$=5V | $I_{IO}$=5mA | | | 1 [2] | V |
| | | | $I_{IO}$=2mA | | | 0.4 [2] | |
| $R_{ON}$ | Weak pull-up equivalent resistor [5] | $V_{IN}$=$V_{SS}$ | | | 60 | | kΩ |
| $t_{w(RSTL)out}$ | Generated reset pulse duration | External pin or internal reset sources | | | 6<br>30 | | $1/f_{SFOSC}$<br>µs |
| $t_{h(RSTL)in}$ | External reset pulse hold time [6] | | | 10 | | | µs |

**Notes:**

1. Unless otherwise specified, typical data are based on $T_A$=25°C and $V_{DD}$=5V, not tested in production.
2. Data guaranteed by design.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in Section 12.2 and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
5. The $R_{ON}$ pull-up equivalent resistor is based on a resistive transistor (corresponding $I_{ON}$ current characteristics described in Figure 72). This data is based on characterization results, not tested in production.
6. To guarantee the reset of the device, a minimum pulse has to be applied to $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.

**Figure 75. $\overline{\text{RESET}}$ pin protection when LVD is enabled.**[1)2)3)4)]

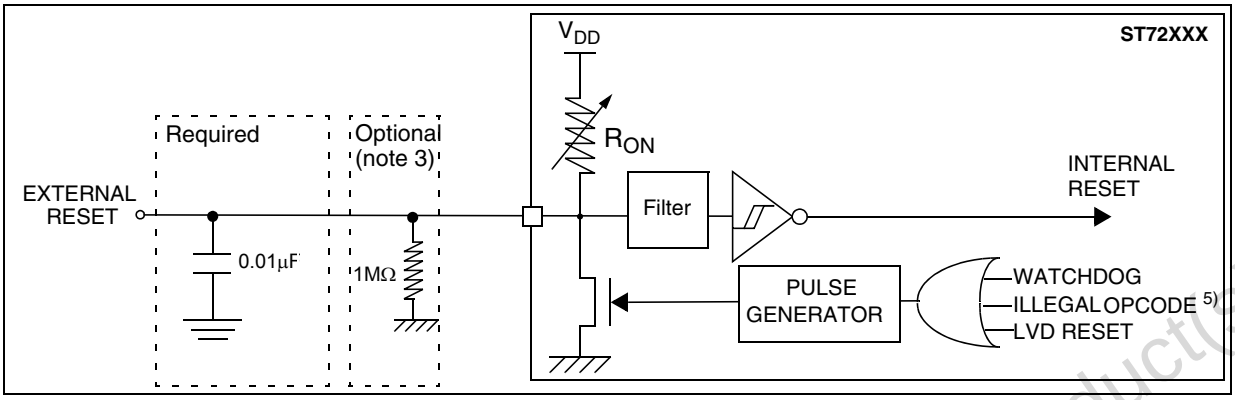
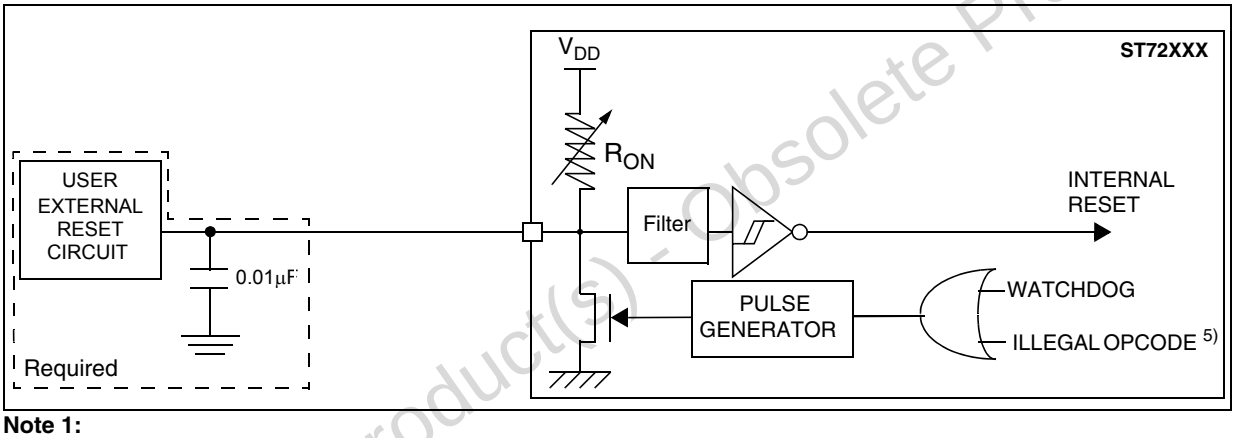



**Figure 76. $\overline{\text{RESET}}$ pin protection when LVD is disabled.**[1)]






**Note 1:**

- The reset network protects the device against parasitic resets.
- The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).
- Whatever the reset source is (internal or external), the user must ensure that the level on the $\overline{\text{RESET}}$ pin can go below the $V_{IL}$ max. level specified in section 12.9.1 on page 113. Otherwise the reset will not be taken into account internally.
- Because the reset circuit is designed to allow the internal RESET to be output in the $\overline{\text{RESET}}$ pin, the user must ensure that the current sunk on the $\overline{\text{RESET}}$ pin is less than the absolute maximum value specified for $I_{INJ(RESET)}$ in section 12.2.2 on page 102.

**Note 2:** When the LVD is enabled, it is recommended not to connect a pull-up resistor or capacitor. A 10nF pull-down capacitor is required to filter noise on the reset line.

**Note 3:** In case a capacitive power supply is used, it is recommended to connect a 1MΩ pull-down resistor to the $\overline{\text{RESET}}$ pin to discharge any residual voltage induced by the capacitive effect of the power supply (this will add 5µA to the power consumption of the MCU).

**Note 4:** Tips when using the LVD:

- 1. Check that all recommendations related to the reset circuit have been applied (see notes above).
- 2. Check that the power supply is properly decoupled (100nF + 10µF close to the MCU). Refer to AN1709 and AN2017. If this cannot be done, it is recommended to put a 100nF + 1MΩ pull-down on the $\overline{\text{RESET}}$ pin.
- 3. The capacitors connected on the RESET pin and also the power supply are key to avoid any start-up marginality. In most cases, steps 1 and 2 above are sufficient for a robust solution. Otherwise: replace 10nF pull-down on the $\overline{\text{RESET}}$ pin with a 5µF to 20µF capacitor."

### 12.12.1 ADC Accuracy

**Table 27. $f_{CPU}$=8 MHz, $f_{ADC}$=4 MHz $R_{AIN}$< 10kΩ 2)**

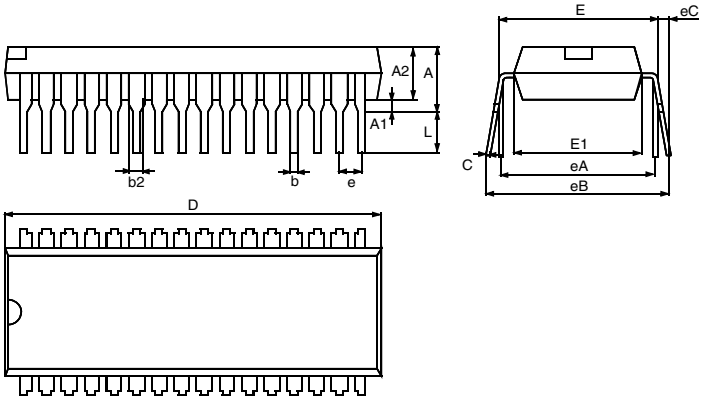
| Symbol | Parameter | Conditions | Typ | Max 1) | Unit |
|---|---|---|---|---|---|
| $\|E_T\|$ | Total unadjusted error | $V_{DD}$= 4V-5.5V | 3 | | LSB |
| $\|E_O\|$ | Offset error | | 1 | 2 | |
| $\|E_G\|$ | Gain Error | | 0.7 | 2 | |
| $\|E_D\|$ | Differential linearity error | | 1.3 | 2 | |
| $\|E_L\|$ | Integral linearity error | | 2.9 | 5 | |

**Notes:**

1. Not tested in production, guaranteed by characterization. All accuracy measurements are taken with the MCU in WAIT mode (no I/O switching) and when adequate low-pass filtering is present (0.1 µF capacitor between $V_{DD}$/$V_{DDA}$ and $V_{SS}$/$V_{SSA}$). Outside these conditions, a degree of microcontroller noise may result, causing accuracy errors which will vary based on board layout and the type of CPU activity.

2. ADC Accuracy vs. Negative Injection Current:
Injecting negative current on any of the analog input pins significantly reduces the accuracy of the conversion being performed on another analog input.
For $I_{INJ-}$=0.8mA, the typical leakage induced inside the die is 1.6µA and the effect on the ADC accuracy is a loss of 4 LSB for each 10KΩ increase of the external analog source impedance. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 12.8 does not affect the ADC accuracy.

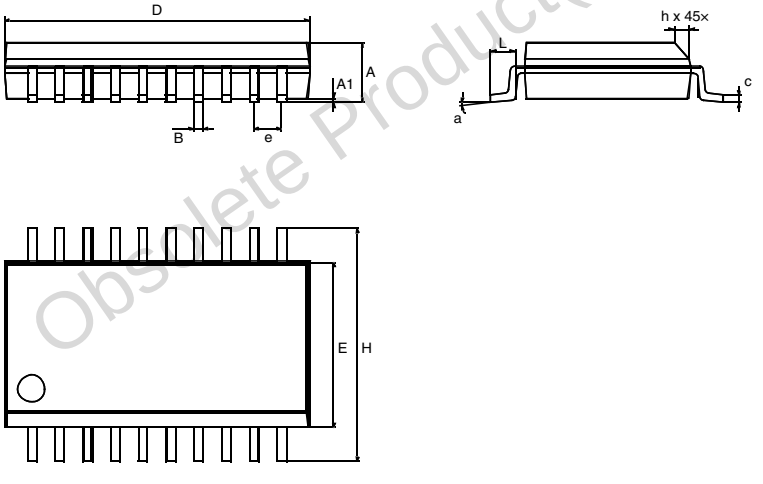
**Figure 89. 32-Pin Plastic Dual In-Line Package, Shrink 400-mil Width**




| Dim. | mm | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 3.56 | 3.76 | 5.08 | 0.1402 | 0.1480 | 0.2000 |
| A1 | 0.51 | | | 0.0201 | | |
| A2 | 3.05 | 3.56 | 4.57 | 0.1201 | 0.1402 | 0.1799 |
| b | 0.36 | 0.46 | 0.58 | 0.0142 | 0.0181 | 0.0228 |
| b1 | 0.76 | 1.02 | 1.40 | 0.0299 | 0.0402 | 0.0551 |
| C | 0.20 | 0.25 | 0.36 | 0.0079 | 0.0098 | 0.0142 |
| D | 27.43 | | 28.45 | 1.0799 | | 1.1201 |
| E | 9.91 | 10.41 | 11.05 | 0.3902 | 0.4098 | 0.4350 |
| E1 | 7.62 | 8.89 | 9.40 | 0.3000 | 0.3500 | 0.3701 |
| e | | 1.78 | | | 0.0701 | |
| eA | | 10.16 | | | 0.4000 | |
| eB | | | 12.70 | | | 0.5000 |
| eC | | | 1.40 | | | 0.0551 |
| L | 2.54 | 3.05 | 3.81 | 0.1000 | 0.1201 | 0.1500 |
| | Number of Pins | | | | | |
| N | 32 | | | | | |

Note 1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 90. 20-Pin Plastic Small Outline Package, 300-mil Width**




| Dim. | mm | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 2.35 | | 2.65 | 0.0925 | | 0.1043 |
| A1 | 0.10 | | 0.30 | 0.0039 | | 0.0118 |
| B | 0.33 | | 0.51 | 0.0130 | | 0.0201 |
| C | 0.23 | | 0.32 | 0.0091 | | 0.0126 |
| D | 12.60 | | 13.00 | 0.4961 | | 0.5118 |
| E | 7.40 | | 7.60 | 0.2913 | | 0.2992 |
| e | | 1.27 | | | 0.0500 | |
| H | 10.00 | | 10.65 | 0.3937 | | 0.4193 |
| h | 0.25 | | 0.75 | 0.0098 | | 0.0295 |
| α | 0° | | 8° | 0° | | 8° |
| L | 0.40 | | 1.27 | 0.0157 | | 0.0500 |
| | Number of Pins | | | | | |
| N | 20 | | | | | |

Note 1. Values in inches are converted from mm and rounded to 4 decimal digits.

# 14 DEVICE CONFIGURATION AND ORDERING INFORMATION

Each device is available for production in user programmable versions (FLASH) as well as in factory coded versions (ROM).

ST7262 devices are ROM versions.

ST72F62 FLASH devices are shipped to customers with a default content (FFh). This implies that FLASH devices have to be configured by the customer using the Option Byte while the ROM devices are factory-configured.

## 14.1 OPTION BYTE

The Option Byte allows the hardware configuration of the microcontroller to be selected.
The Option Byte has no address in the memory map and can be accessed only in programming mode using a standard ST7 programming tool. The default content of the FLASH is fixed to FFh. This means that all the options have “1” as their default value.

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| - | - | WDG SW | NEST | LVD | - | OSC 12/6 | FMP_ R |

Bits 7:6 = Reserved.

Bit 5 = **WDGSW** *Hardware or software watchdog*
This option bit selects the watchdog type.
0: Hardware enabled
1: Software enabled

Bit 4 = **NEST**
This option bit selects the nested interrupts feature.
0: Nested interrupt feature disabled
1: Nested interrupt feature enabled

Bit 3 = **LVD** *Low Voltage Detector selection*
This option bit selects the LVD.
0: LVD enabled
1: LVD disabled

Bit 2= Reserved.

Bit 1 = **OSC12/6** *Oscillator selection*
This option bit selects the clock divider used to drive the USB interface at 6MHz.
0: 6 MHz oscillator (no divider for USB)
1: 12 Mhz oscillator (2 divider for USB)

Bit 0 = **FMP_R** *Memory Readout Protection*
Readout protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Erasing the option bytes when the FMP_R option is selected will cause the whole memory to be erased first and the device can be reprogrammed. Refer to the ST7 Flash Programming Reference Manual and section 4.3.1 on page 14 for more details.
0: Read-out protection enabled
1: Read-out protection disabled



## 14.2 DEVICE ORDERING INFORMATION AND TRANSFER OF CUSTOMER CODE

Customer code is made up of the ROM contents and the list of the selected options (if any). The ROM contents are to be sent on diskette, or by electronic means, with the hexadecimal file in .S19 format generated by the development tool. All unused bytes must be set to FFh.

The selected options are communicated to STMicroelectronics using the correctly completed OPTION LIST appended.
Refer to application note AN1635 for information on the counter listing returned by ST after code has been transferred.
The STMicroelectronics Sales Organization will be pleased to provide detailed information on contractual points.