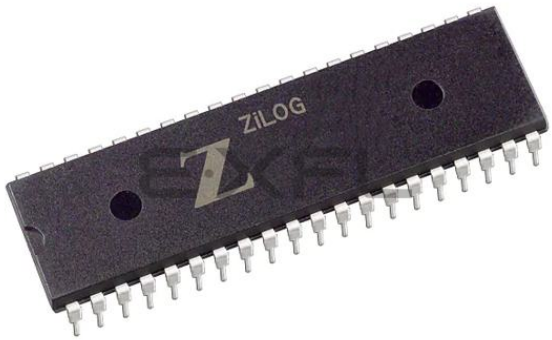

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	TV Controller
Core Processor	Z8
Program Memory Type	OTP (24kB)
Controller Series	Digital Television Controller (DTC)
RAM Size	640 x 16
Interface	-
Number of I/O	19
Voltage - Supply	4.5V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8930012psc

DEVICE IDENTIFICATION AND SUMMARY

Zilog's Z893xx family of television controller products combine On-Screen Display and VBI data capture functions to provide a highly integrated solution for TV, VCR and set-top applications. Family members serve as either stand-alone controllers providing the most cost effective central processing facility or as add-on controllers where time-to-market is a key factor. Common to all devices is a high-speed 16-bit RISC controller that provides ultimate OSD flexibility and allows for digital VBI data capture. The power of the Z893xx family architecture is evident by it's ability to support a variety of OSD applications including Line 21 closed-caption, EDS and Starsight. Table 1 summarizes the features of the devices in the family.

In Circuit Emulation is facilitated by the Z89309 124-pin PGA device. The Z89332/6 are 24K/12K ROM variants in 42-pin SDIP package.

One Time Programmable versions of the parts Z89300/ Z89331, are offered for development and small scale production.

The Z89302, Z89303, Z89304, Z89305, Z89306 and Z89307/8/13/14 are mask ROM devices intended for high volume TV chassis production applications. They offer 40-pin, DIP and 52-pins DIP package configurations with 10K, 12K word, 16K word, and 24K word program memory sizes.

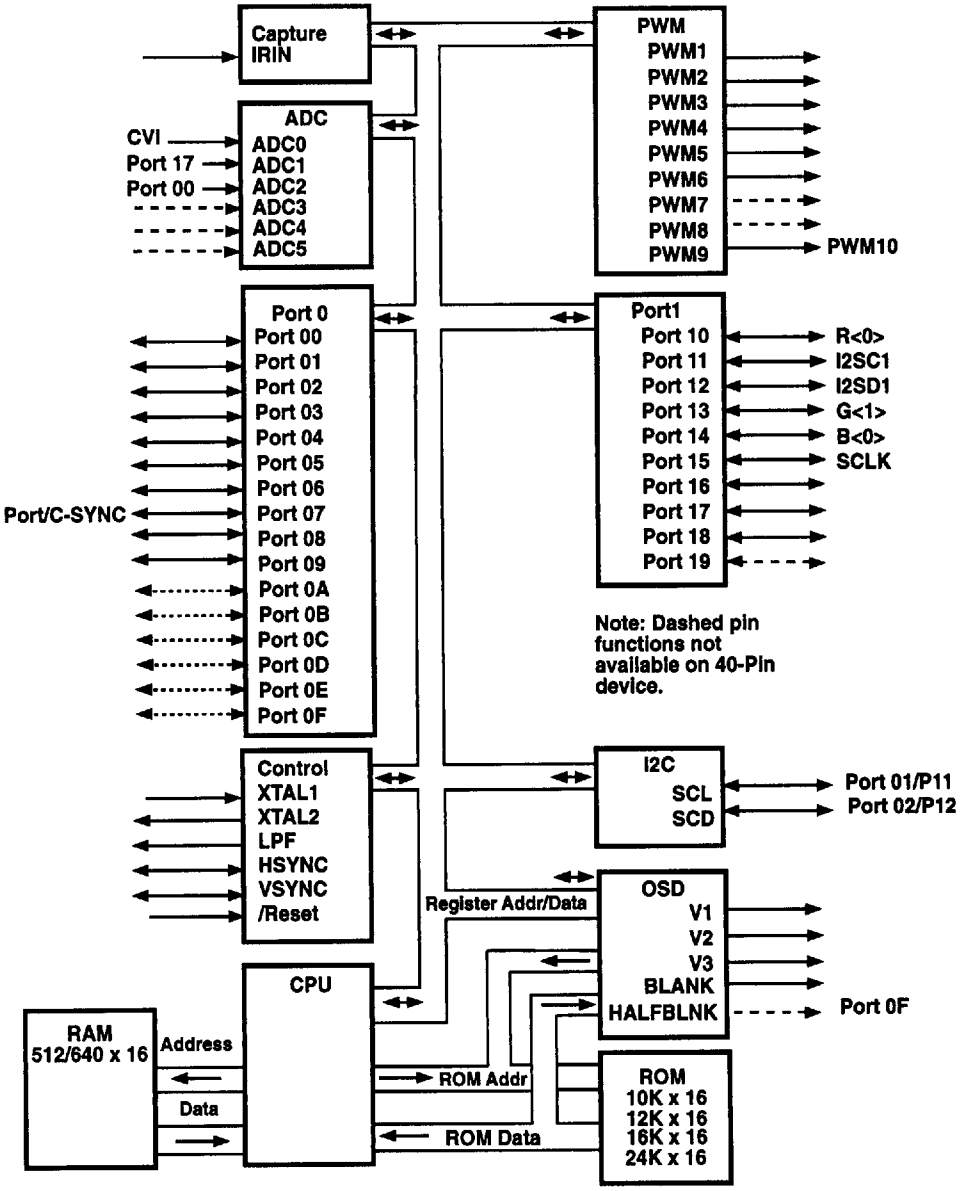


Figure 1. Z89300 Functional Block Diagram

PIN DESCRIPTION

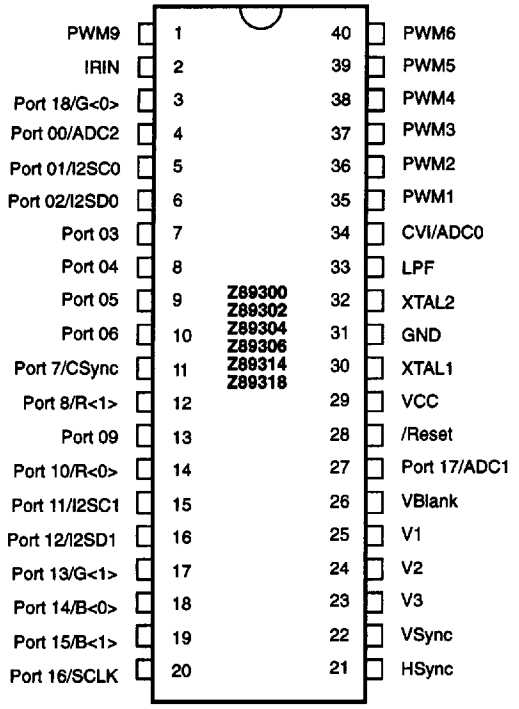


Figure 2. Z89300/02/06 40-Pin DIP

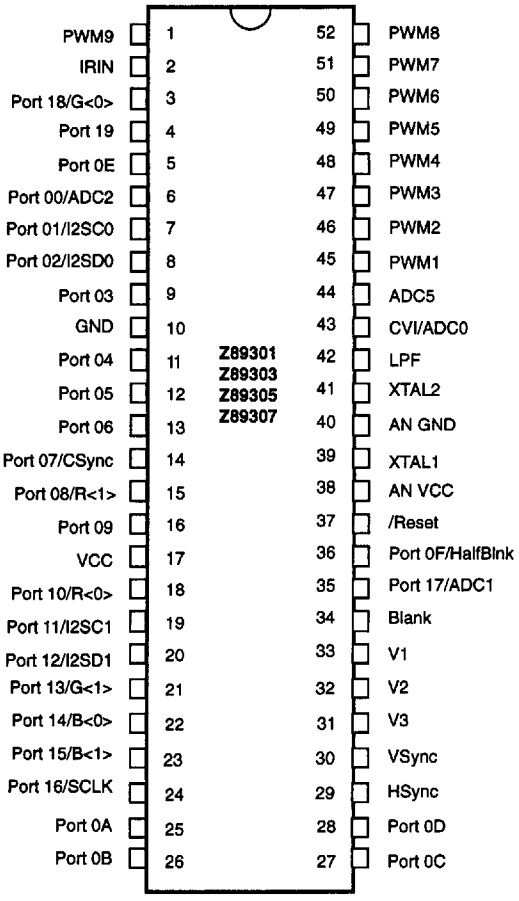


Figure 3. Z89301/03/07 52-Pin DIP

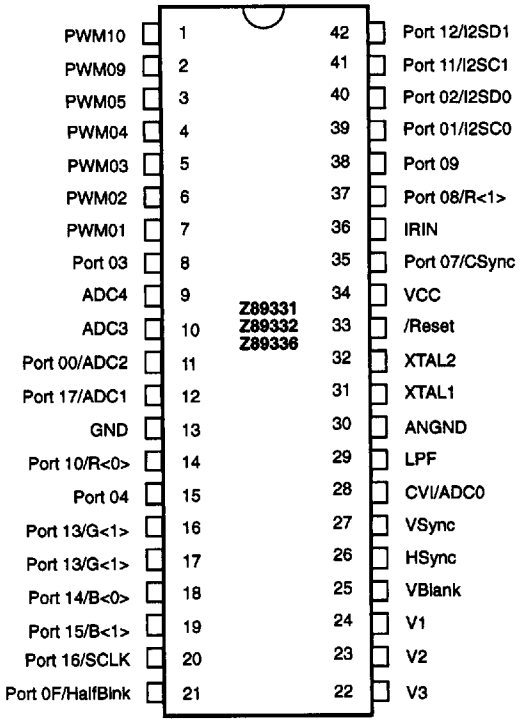


Figure 4. Z89332/336 42-Pin DIP

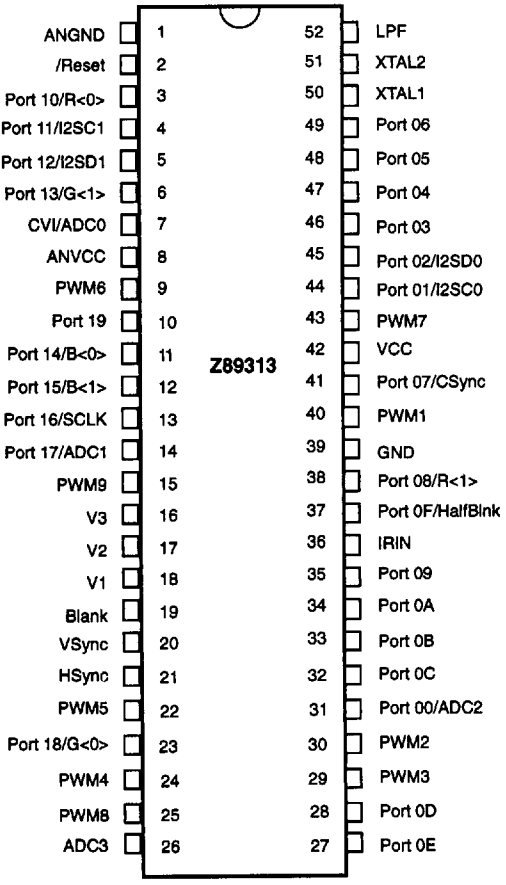


Figure 5. Z89313 52-Pin DIP

Table 7. Register2 - R2(0) PLL Frequency Data Register

Reg field	Bit position	R	W	Data	Description
Port/PWM	fedcba98--------	R	W		Return"0" No effect
PLL_data	--------76543210	R	W	xx	PLL divider = 256 + xx

The VCO, DOT and SCLK frequency are defined as

Fvco = Fdot = Fsclk = 32 kHz x (256 + PLLdata)

Upon POR the PLL frequency data register is preset to %70, which corresponds to the VCO frequency of 12.058 MHz.

REGISTERS (Continued)

Table 18. Register5 - R5(1) Timer Control Register

Reg field	Bit position	R	W	Data	Description
CAPint_r	f----------	R		1 0	Rising edge is captured No rising edge is captured
			W	1 0	Reset flag No effect
CAPint_f	-e---------	R		1 0	Falling edge is captured No falling edge is captured
			W	1 0	Reset flag No effect
Tout_1s	--d--------	R		1 0	Timeout of 1s timer No timeout of 1s timer
			W	1 0	Reset flag No effect
Tout_CAP	---c-------	R		1 0	Timeout of Capture timer No timeout of Capture timer
			W	1 0	Reset flag No effect
Reserved	----ba------	R			Return "0"
			W		No effect
Speed_1s	------98--------	R	W	00 01 10 11	1s 250 ms 62.5 ms 15.625 ms
1s/CAP_int	--------7-------	R	W	1 0	int2 source is 1s timer int2 source is Capture timer
CAP_halt	---------6------	R	W	1 0	Capture timer is halted Capture timer is running
CAP_edge	----------54----	R	W	00 01 10 11	No Capture Capture on rising edge only Capture on falling edge only Capture on both edges
CAP_glitch	------------32--	R	W	00 01 10 11	Glitch filter is disabled <8TSCLK is filtered out <32TSCLK is filtered out <128TSCLK is filtered out
CAP_speed	--------------10	R	W	00 01 10 11	SCLK/4 SCLK/8 SCLK/16 SCLK/32

When capture register is initialized together with a glitch filter, the CAP_speed field should specify the clock of the capture register with the period shorter than the glitch filter for setting defined by the CAP_glitch field.

For example, the following setting is invalid: CAP_glitch = 10b; CAP_speed = 10b;
The example of valid setting is CAP_glitch = 10b; CAP_speed = 11b

Table 19. Register6 - R6(1) Clock Switch Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba9876------	R	W		Return "0" No effect
SVCO/PVCO	----------5-----	R	W	1 0 1 0	SCLK=SVCO (flag) SCLK=PVCO (flag) Switch SCLK to PVCO No effect
No_switch	----------4----	R	W	1 0	SCLK=PVCO, NO clock switching Clock switching is enabled
H_position	----------3210	R	W	%D	Defines delay of Hint by 4D SCLK cycles

The clock switch control register defines the source of SCLK fed into the Z89C00 core. The block diagram of the clock switch circuit is presented on figure below.

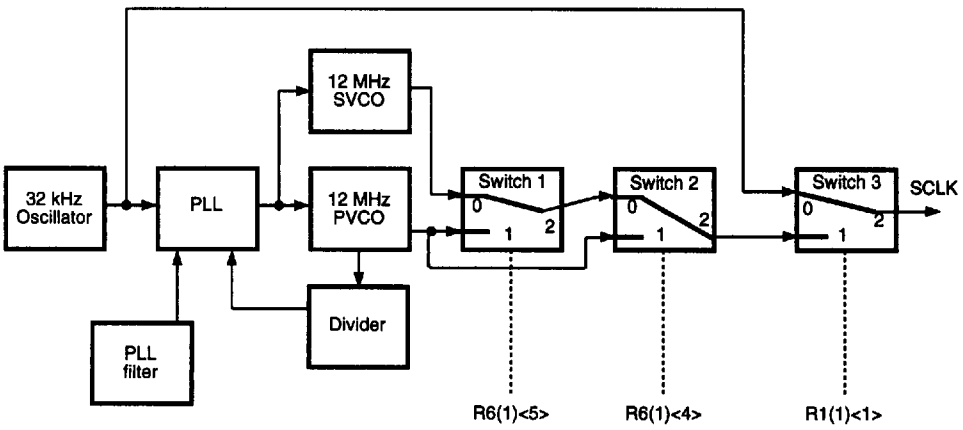


Figure 10. Clock Switch Control Register

Switch1 positioning defines the source of the signal on terminal 0 of switch2. Switch2 is used to override the frequency setting in "no_switch" mode. Whenever "no_switch" mode is set, switch1 continues to switch between PVCO and SVCO. Because of that it is not recommended to switch2 if it is not guaranteed that PVCO signal is fed to terminal0 of switch2. The recommended sequence is as follows:

1. Switch SCLK to PVCO
2. Wait for 2..3 SCLK cycles to ensure that the SCLK is switched
3. Switch R6 (1) <4> to enable/disable "no_switch" mode.

Table 30. Register6 - R6(3) Palette Control Register

Reg field	Bit position	R	W	Data	Description
Palette	f---------------	R	W	1 0	Palette mode is active Palette mode is inactive
Underline color	-edc------------	R	W	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	Black Blue Green Light Blue Red Magenta Yellow White
Palette1	----ba9---------	R	W	%D	Same as Underline color
Palette0	-------876------	R	W	%D	Same as Underline color
Palette3	----------543---	R	W	%D	Same as Underline color
Palette2	------------210	R	W	%D	Same as Underline color

Upon POR the palette control register is reset to "0".

REGISTERS (Continued)

Table 31. Register7 - R7(3) Output Palette Control Register

Reg field	Bit position	R	W	Data	Description
Reserved HBLANK_Delay	fedc----------	R W			Return "0" Delay Value No effect %00 - POR Condition
Background_on/off	----b----------	R	W	1 0	Background is on Background is off - POR condition
Background_color	-----a98--------	R	W	%D	Defines the color of the background (the same as the Palette)
Reserved	--------7-------	R W			Return "0" No effect
StarSight palette	---------6------	R	W	0 1 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	Palette is defined by bits <5..0> StarSight palette: Black V1=0; V2=0; V3=0; Blue V1=0; V2=99% V3=99%; Green V1=66%, V2=99%; V3=99%; Grey V1=66%; V2=66%; V3=66%; Red V1=99%; V2=33%; V3=33%; LtYell V1=99%; V2=99%; V3=0; Yellow V1=99%; V2=99%, V3=0; White V1=99%; V2=99%; V3=99%;
Palette_ red (V1)	----------54----	R	W	0 0 0 1 1 0 1 1	66% red 66% red + 33% blue 66% red + 33% green 66% red + 33% blue + 33% green
Palette_ green (V2)	------------32--	R	W	0 0 0 1 1 0 1 1	66% green 66% green + 33% blue 66% green + 33% red 66% green + 33% blue + 33% red
Palette_ blue (V3)	--------------10	R	W	0 0 0 1 1 0 1 1	66% blue 66% blue + 33% green 66%blue + 33% red 66% blue + 33% green + 33% red
Digital_ mode	----------543210	R	W	000000	Outputs V1, V2, V3 correspond to 100% red, green, and blue outputs

Upon POR the Output palette register is set to "0" - digital output.

Note: If bit R7(3)<6> is set to "1", while bits R7(3)<5:0> are reset to a "0". the outputs V1, V2 and V3 of Z89300 will be switched into a "Digital mode".

REGISTER SUMMARY

Table 32. Register Utilization Rev 2.0

BANK	BANK Sub Address	READ Register	WRITE Register	Description
Bank 0	7	dir1		10-bit I/O port 1 direction control
	6	dir0		16-bit I/O port 0 direction control
	5	port1		10-bit I/O port 1
	4	port0		16-bit I/O port 0
	3	i2c_int		I2C interface register
	2	pll_freq		PLL frequency control
	1	pwm_data10		14-bit PWM10 data
	0	pwm_data9		14-bit PWM9 data
Bank 1	7	wdt_smr_ctl		Stop-Mode Recovery/Watch-Dog Timer Control
	6	clock_ctl		Clock control (switch VCO/DOT)
	5	cap_1s_ctl		Counter timers control
	4	atod_ctl		A/D converter control
	3	standard_ctl		Output H/V-sync/blnk control
	2	stop_wdt_ctl		Stop and Watch-Dog Timer Control
	1	sclk_freq		Stop/Sleep/Normal Mode
	0	clamp_pos		Defines position of video clamp pulse
Bank 2	7	pwm_data8		8-Bit PWM 8 data
	6	pwm_data7		8-Bit PWM 7 data
	5	pwm_data6		8-Bit PWM 6 data
	4	pwm_data5		8-Bit PWM 5 data
	3	pwm_data4		8-Bit PWM 4 data
	2	pwm_data3		8-Bit PWM 3 data
	1	pwm_data2		8-Bit PWM 2 data
	0	pwm_data1		8-Bit PWM 1 data
Bank 3	7	output palette		Output palette
	6	palette_color		Display palette color/underline color
	5	capture_data	(no effect)	Capture register data
	4	osd_control		On-Screen Display Control
	3	attribute_data	vram_data	Character attribute/video ram data
	2	ch_x1_lo_x3	cg_attribute	Character mult./char. graphics attribute
	1	lo_x2_mid_x3	cg_nxt_prv	Character mult./next or previous data
	0	hi_x2_hi_x3	cg_current	Character mult./current data

A to D and Clamp Circuit Operation (Recommended Practice)

A 4-bit A to D implemented in Z89300 has five multiplexed inputs. Three of them are available in 40-pin package (CVI, ADC1/P17 and ADC2/P00). There are two configurations of 52-pin package with different ADC inputs bonded out: 52-pinN - CVI, ADC1/P17, ADC2/P00 and ADC4 and 52-pinW - CVI, ADC1/P17, ADC2/P00 and ADC3. On 124-pin package all five A to D inputs are bonded out.

The allowed range of the input signals is different for different A to D inputs according to the following table:

Table 37. A to D Inputs Typical Range

Input	Range (V)	Clamping	Typical Application
CVI/ADC0	1.5..2.0	Yes-Ref-	CCD sampling input
ADC1/P17	0 ..5.0	No	AFC input
ADC2/P00	0 ..5.0	No	Key scanning input
ADC3	0 ..5.0	No	Key scanning input
ADC4	0 ..5.0	No	Key scanning input
ADC5	1.5 ..2.0	Yes - Ref+	V-SYNC decoder sampling input

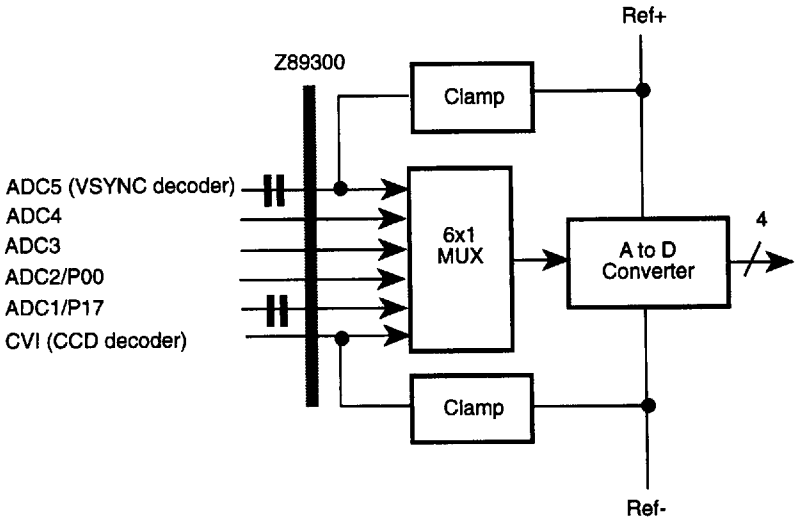


Figure 11. A to D Block Diagram

Internally generated reference voltages define the maximum range of the input signal of the A to D. Nominal values of Ref+ = 2.0V: Ref= 1.5 V @ V_{CC} = 5V for different values of V_{CC} the reference voltages should be pro-rated.

The maximum sampling rate of the A to D converter is 3 MHz. It takes 4 SCLK cycles for the valid data at the output of the A to D to become available. This matter should be taken into consideration especially if application is utilizing a single shot mode.

V1, V2, V3 Analog Output (Continued)

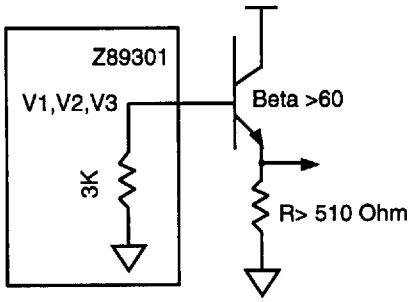


Figure 13. Recommended Circuit

MODULE DESCRIPTIONS

Z89COO Core Processor Module

Memory Organization

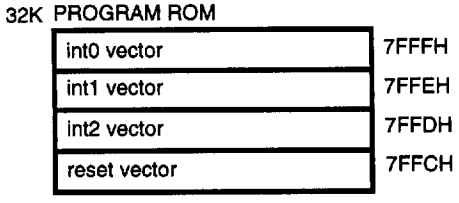
The C00 core has access to three types of memory that are of interest here:

1. **Program Read Only Memory (PROGRAM)**
   Size: 12K, 16K or 24K words (16 bytes) depending on device version selected.

2. **External Registers**
   Addressable Size: Four selectable banks of up to eight registers each, providing access to up to 32 register addresses. Registers can be selected for read or write operations. Some registers are only accessible in either read mode or write mode.

3. **Processor RAM**
   Size: Two banks of 256 words of 16 bits each, providing a total of 512 words of RAM on 89314, extra 128 words on all other parts in the range on third bank.

Other memory exists in the form of internal registers in the processor and registers that are not part of the processor's direct memory map.



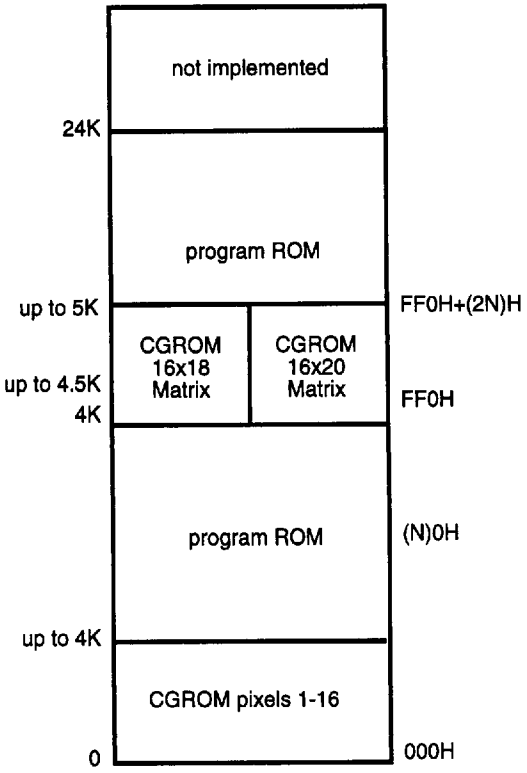


Figure 14. Program Read Only Memory

MODULE DESCRIPTIONS (Continued)

The size of memory used as CGROM depends on the number and resolution of characters stored in memory. 'N' represents the number of characters stored, ranging from 0 to 256. If characters are 16 x 18 or 16 x 20 pixels then the upper region of memory starting at the 4K boundary is used for character storage. If not it can be used as program memory.

Clocking Operation

The processor is able to operate from a number of clock sources.

1. Primary Phase Locked Loop V_{co} source (PVCO)
2. Secondary V_{co} phase-aligned with VSYNC timing (SVCO)
3. 32 kHz oscillator clock (OSC)

In addition the processor clock may be halted temporarily to allow clock selection or ROM accesses to be performed without disrupting normal operation of the processor.

PADS CONFIGURATION

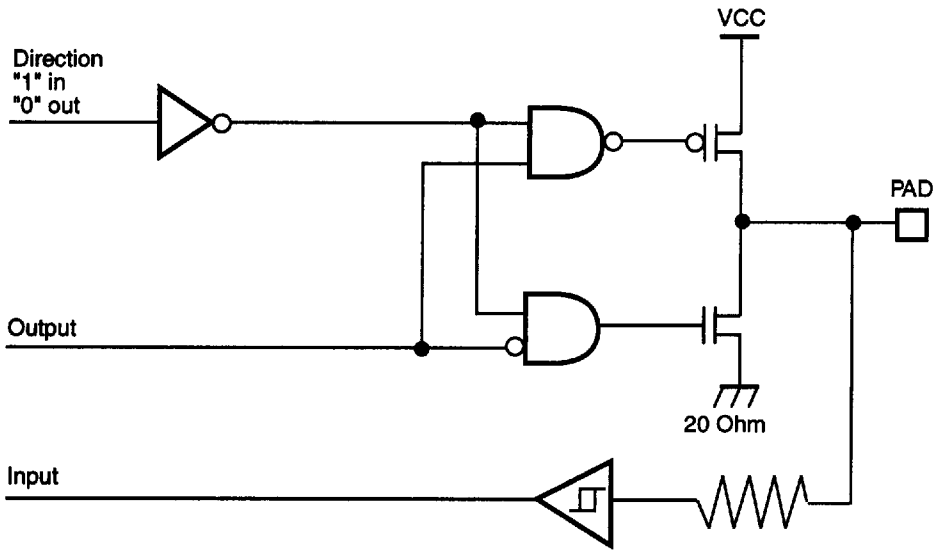


Figure 15. Type1 Bi-directional Port pins (Port 3, Port0f, Port 10, Port 13, Port 16, Port 18, Port 19, H-SYNC and V-SYNC)

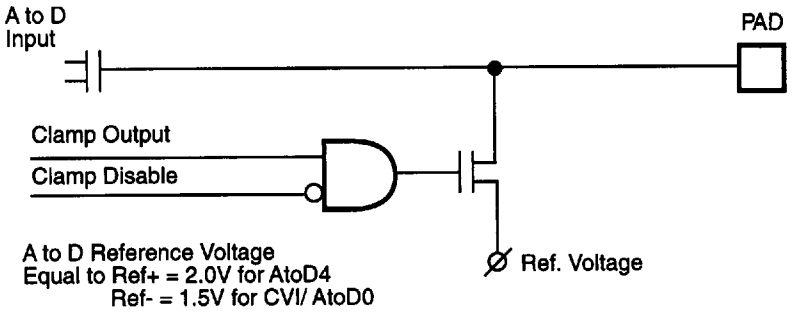


Figure 19. Type5 AtoD Inputs Combined with an Internal Clamp (Composite Video Input/AtoD0 and AtoD4).

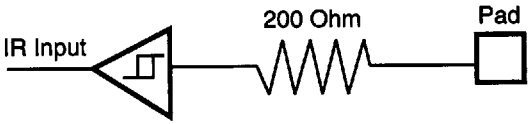


Figure 20. Type6 IR Capture Register Input

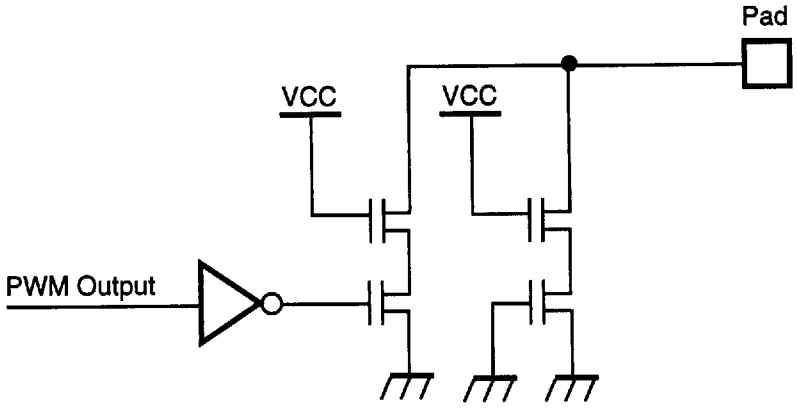


Figure 21. Type7 PWM1, PWM8 Open-Drain Outputs

PADS CONFIGURATION (Continued)

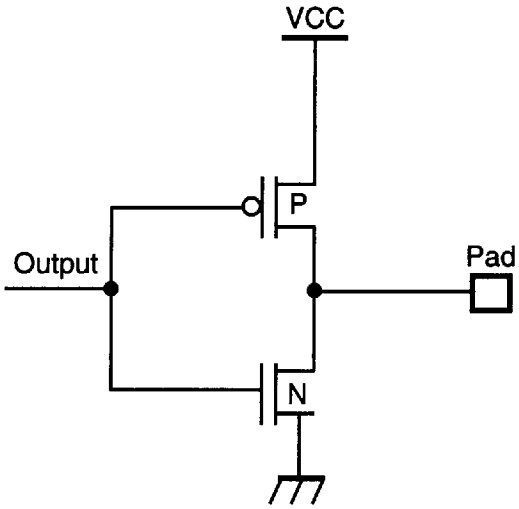


Figure 22. Type8 PWM9 and BLANK outputs; V1, V2, V3 outputs in digital mode

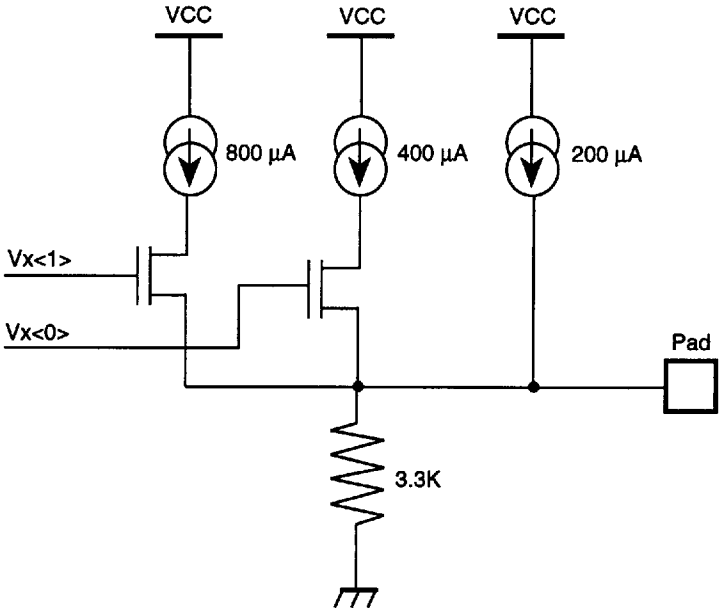


Figure 23. V1, V2 and V3 outputs in analog (palette) mode.

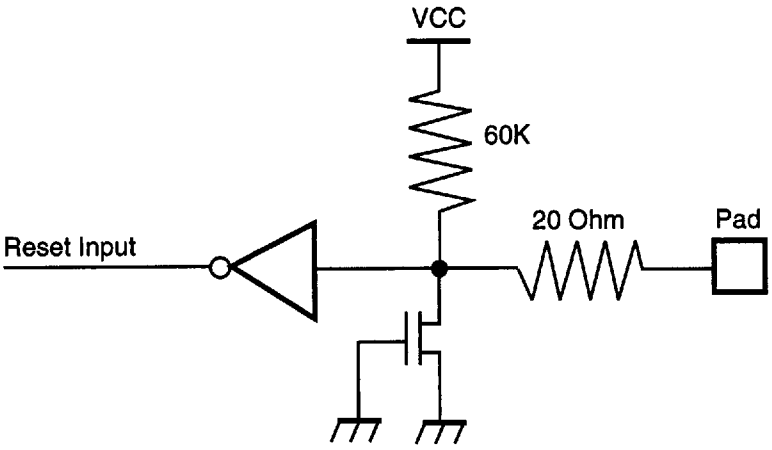


Figure 24. Reset Input

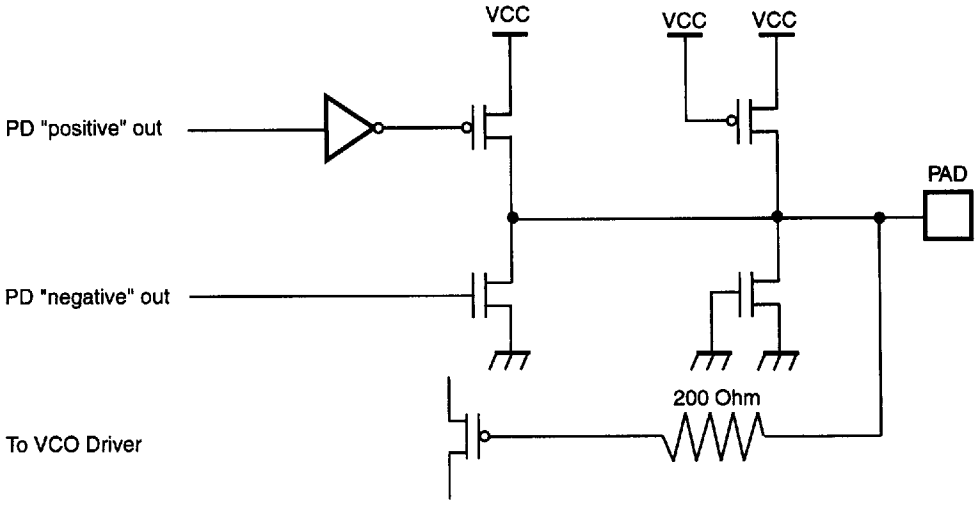


Figure 25. Loop Filter Pin

ABSOLUTE MAXIMUM/MINIMUM RATINGS

Sym	Parameter	Min	Max	Units	Conditions
V_{CC}	Power supply voltage	0	7	V	
V_{ID}	Input voltage	-0.3	V_{CC}+0.3	V	Digital inputs
V_{IA}	Input voltage	-0.3	V_{CC}+0.3	V	Analog inputs (A/D0..A/D4)
V_O	Output voltage	-0.3	V_{CC}+0.3	V	All push-pull digital outputs
V_O	Output voltage	-0.3	V_{CC} +8.0[1]	V	Open-drain PWM outputs (PWM1..PWM8)
I_{OH}	Output current high		-10	mA	one pin
I_{OH}	Output current high		-100	mA	All pins
I_{OL}	Output current low		20	mA	one pin
I_{OL}	Output current low		200	°C	All pins
T_A	Operating Temperature	0	70	°C	
T_A	Storage Temperature	-65	150	°C	

Note:
1. Momentary withstand voltage 16V

DC CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 4.5V to 5.5V; F_{OSC} = 32.768 kHz)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input voltage low	0	0.4	0.2 V_{CC}	V	
V_{IH}	Input voltage high	0.6 V_{CC}	3.6	V_{CC}	V	
V_{IH}	Input voltage high	0.75 V_{CC}	4.2		V	Reset pin only
V_{PU}	Maximum pull-up voltage			12	V	For PWM1..PWM8 only
V_{OL}	Output voltage low		0.16	0.4	V	@ I_{OL} = 1 mA
V_{OL}	Output voltage high	V_{CC} -0.9	4.75		V	@ IOL = 0.75 mA
V_{XL}	Input voltage XTAL1 low		1.0	0.3 V_{CC}	V	External clock generator driven
V_{XH}	Input voltage XTAL1 high	0.6 V_{CC}			V	
V_{HY}	Schmitt Hysteresis	0.3	0.5	0.75	V	XTAL1 input pin
I_{IR}	Reset input current		90	150	µA	VRL = 0V
I_{IL}	Input leakage	-3.0	0.01	3.0	µA	@ 0V and V_{CC}
I_{CC}	Supply current		60	100	mA	
I_{CCIE}	Supply current of the OTP		300	700	µA	Sleep mode @ 32 kHz
I_{CC1}	Supply current		100	300	µA	Sleep mode @ 32 kHz
I_{CC2}	Supply current		5	10	µA	Stop mode

RECOMMENDATIONS

Reset Circuit

The 32 kHz crystal oscillator of the Z89300 has a typical setting time of 800 ms. The reset will be supplied to the Microprocessor core only if the "reset" pin of the device is held "low" for more than 5 clock cycles. In case of the POR, the external RC circuit should provide a time delay of more than the longest possible setting time of the oscillator.

The typical value of the internal pull-up resistor is 60±20 Kohm.

Assuming that the RC constant of the reset circuit should be >1s, the value of the capacitor can be calculated from:

$$C=\frac{1}{R}=\frac{1}{60x10^{3}}=15x10^{-6}=15.0\ \mu f$$

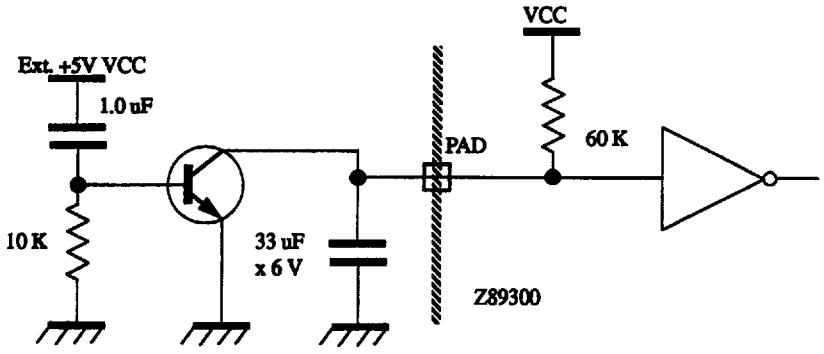


Figure 26. Reset Circuit

HSYNC (HFLYBACK) Recommended Timing (Continued)

CCD data captioning algorithm utilizes sampling of the Composite Video signal during line 21. In order for the CCD algorithm to recognize CCD burst (seven clock cycles of 503 kHz) certain timing relationships between incoming Composite Video signal and HFLYBACK should be maintained.

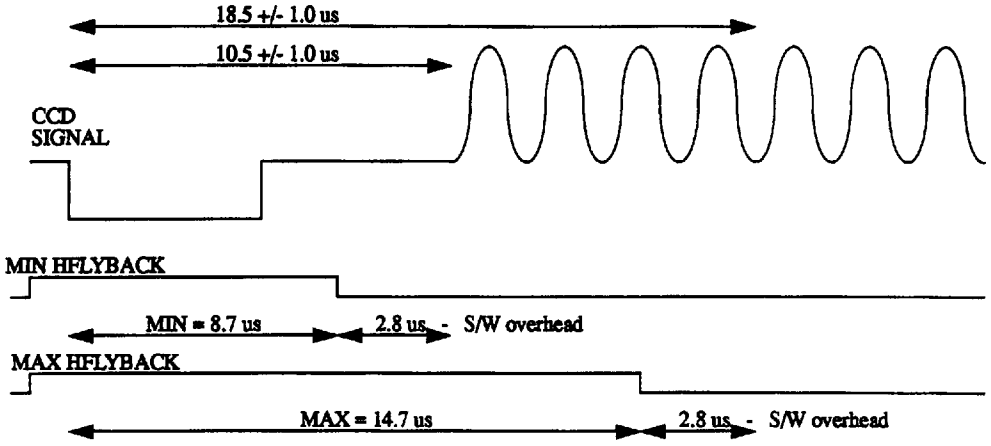


Figure 28. HFLYBACK Timing Diagram

In order to guarantee CCD algorithm performance, the time delay from leading edge of HSYNC to trailing edge of HFLYBACK should be maintained from 8.7 µs to 14.7 µs.

In order to comply with both OSD centering and CCD performance requirements, the time delay of trailing edge of HFLYBACK should be from 8.7 µs to 10.4 µs, which corresponds to HFLYBACK width of 9.7 µs....11.4 µs if leading edge of HFLYBACK is 1.0 µs ahead of leading edge of HSYNC.

Clamp Positioning

The black level of Composite Video signal fed to Z89300 should be set to Ref - voltage of the A to D. In order to shift the DC level of the incoming signal, there is an internal clamp in the Z89300. The clamp pulse should be located during the back porch of the HSYNC.

Clamp position is defined by the "Position" field (bits <6:0>) in Clamp Position register R0(1). The width of clamp pulse cannot be modified and is set to 1 µs. The value which can be assigned to the "Position" field should be >10% and <7%f. The time interval between the leading edge of the H-FLYBACK and the beginning of the clamp pulse can be calculated from:

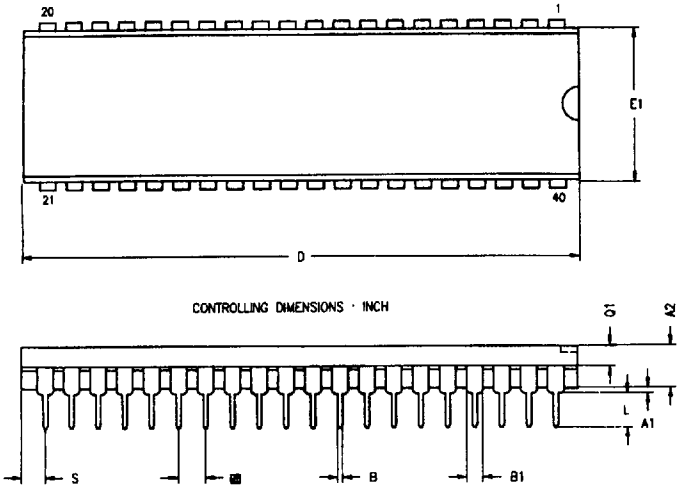
$$Tdelay = Position \times \frac{1}{Tsclk} = Position \times 82\ ns$$

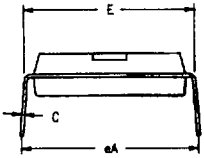
Because the clamp pulse is generated from the leading edge of the incoming HFLYBACK signal, there are certain constraints imposed on the relative positioning of the leading edge of HFLYBACK relative to leading edge of HSYNC.

By setting the "Position" field of Clamp Position register, the clamp pulse can be positioned at 1.3 µs....10.5 µs after the leading edge of HFLYBACK.

The optimal position of the clamp pulse is 6.5 µs after the leading edge of the HSYNC (in the middle of the back porch interval). Wide setting of "Position" field allows for possible variations in HFLYBACK positioning of up to +4.0 µs....-5.0 µs.

PACKAGE INFORMATION





SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	060	.075
S	1 52	2.29	.060	.090

40-DIP Package Diagram