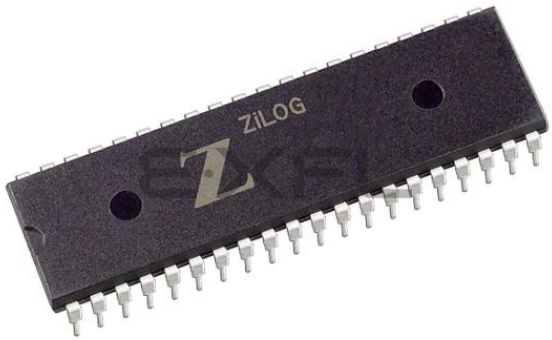

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	TV Controller
Core Processor	Z8
Program Memory Type	OTP (24kB)
Controller Series	Digital Television Controller (DTC)
RAM Size	640 x 16
Interface	-
Number of I/O	19
Voltage - Supply	4.5V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8930012psg

DEVICE IDENTIFICATION AND SUMMARY

Zilog's Z893xx family of television controller products combine On-Screen Display and VBI data capture functions to provide a highly integrated solution for TV, VCR and set-top applications. Family members serve as either stand-alone controllers providing the most cost effective central processing facility or as add-on controllers where time-to-market is a key factor. Common to all devices is a high-speed 16-bit RISC controller that provides ultimate OSD flexibility and allows for digital VBI data capture. The power of the Z893xx family architecture is evident by it's ability to support a variety of OSD applications including Line 21 closed-caption, EDS and Starsight. Table 1 summarizes the features of the devices in the family.

In Circuit Emulation is facilitated by the Z89309 124-pin PGA device. The Z89332/6 are 24K/12K ROM variants in 42-pin SDIP package.

One Time Programmable versions of the parts Z89300/ Z89331, are offered for development and small scale production.

The Z89302, Z89303, Z89304, Z89305, Z89306 and Z89307/8/13/14 are mask ROM devices intended for high volume TV chassis production applications. They offer 40-pin, DIP and 52-pins DIP package configurations with 10K, 12K word, 16K word, and 24K word program memory sizes.

FUNCTIONAL DESCRIPTION

Capture Function

The capture function is intended for Infrared Remote data capture. It employs a capture register that holds the time value from one transition of I.R. data to the next.

The CPU can periodically check the capture status and read the value if a new capture has occurred. Subsequent decoding and command passing of the received I.R. signal is under program control.

Pulse Width Modulator Function

Pulse Width Modulation is used in conjunction with external low pass filters to perform digital to analog conversion. Eight PWM's of 8-bit resolution each find application in generating 0-12 volt signals for control of video and sound attributes. Two 14-bit resolution PWMs may be used with external circuits to generate the controlling voltage for voltage synthesis tuners. In the case of the chassis employing a frequency synthesis tuner, this PWM may also control video or sound attributes.

Each PWM circuit has a data register whose content are set under program control. The data in the register determines the ratio of PWM high to PWM low time.

Analog to Digital Converter Function

This function employs a 4-bit resolution, flash A to D converter. A six to one input multiplexor and conversion start circuits are controlled by the user program. The 4-bit conversion result is available to be read by the CPU at the end of each conversion.

One input channel (ADC0) is dedicated for quantizing VBI (vertical blank interval) data for subsequent digital signal processing. The other channel (ADC5) is typically used for V-SYNC separation from the composite TV signal. These channels have a special video clamp circuit that provides DC restoration of the composite video input signal. Typical VBI applications include Line 21 Closed-Caption, Electronic Data Services and Starsight Telecast. The range of ADC0 and ADC4 is 0.5V p-p from 1.5V to 2.0V.

The remaining four channels are general-purpose. They are typically used for implementation of tuner automatic frequency control and analog key entry. The range of ADC1/2/3/4 is from 0V to 5.0V.

Port Functions

Two input/output port blocks are available for general-purpose digital I/O application. Each port bit is programmable to be either input or output. To conserve device pin count, some port pins are mapped to provide I/0 to the A to D converter block and I^2C interface block.

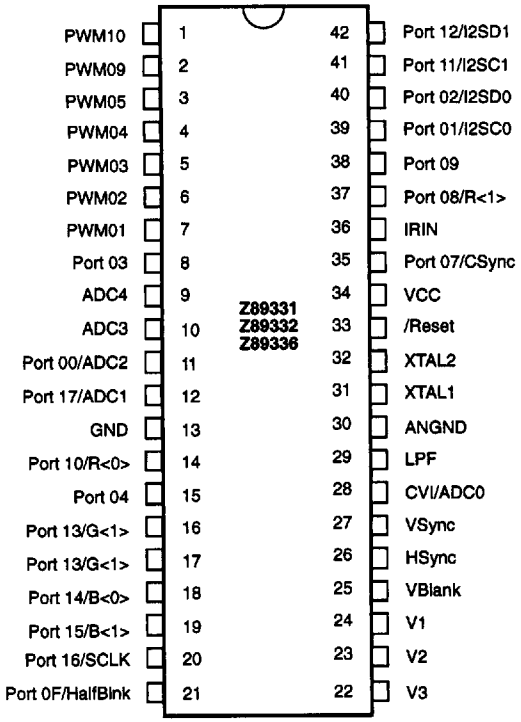

Figure 4. Z89332/336 42-Pin DIP

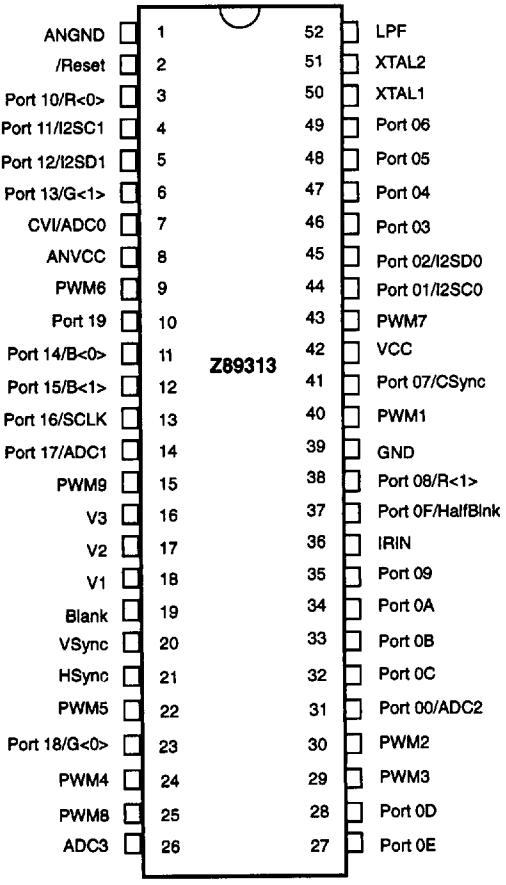

Figure 5. Z89313 52-Pin DIP

PIN IDENTIFICATION

Table 2. Pin Identification

Pin		Package				Configuration	
Name	**Function**	**Z89301/3/5/7 52-pin SDIP**	**Z89313 52-pin SDIP**	**Z89300/02/4/6 14/18 40-pin DIP**	**Z89331/332 /336 42-pin DIP**	**Direction**	**Reset**
VCC	+5 Volts	17,38	8,42	29,–,	34	PWR	–
GND	0 Volts	10,40	1,39	31,–,	13,30	PWR	–
IRIN	Infrared Remote Capture Input	2	36	2	36	I	I
ADC [5:0][1]	4-Bit Analog to Digital Converter input[2].	44,–,–,6, 35,43	–,–,26,31 14,7	–,–, –, 4,27 34	–, 9,10, 11,12,28	AI	I
PWM10, PWM9	14-Bit Pulse Width Modulator Output	–,1	–,15	–,1	1,2	OD	0
PWM[8:1][3]	8-Bit Pulse Width Modulator Output	52,51,50,49, 48,47,46,45	25,43,9,22, 24,29,30,40	–,–.40,39. 38,37,36,35	–,–, –,3,4, 5,6,7	OD	0
Port0[F:0][4]	Bit Programmable Input/Output Ports	36,5,28,27, 26,25,16,15, 14,13,12,11, 9,8,7,6	37,27,28,32, 33,34,35,38, 41,49,48,47, 46,45,44,31,	–,–,–,–,–,–, 13,12,11, 10,9,8,7, 6,5,4	21,–,–,–, –,–,38,37, 35,–,–,15, 8,40,39,11	B	I
Port1[9:0][5]	Bit Programmable Input/Output Ports	4,3,35,24, 23,22,21, 20,19,18	10,23,14, 13,12,11, 6,5,4,3	–,3,27, 20,19,18, 17,16,15, 14	–,16,12, 20,19,18, 17,42,41, 14	B	I
SCL[6]	I^2C Clock I/O	7 or 19	44 or 4	5 or 15	39 or 41	BOD	
SCD[7]	I^2C Data I/O	8 or 20	45 or 5	6 or 16	40 or 42	BOD	
XTAL1	Crystal oscillator input	39	50	30	31	AI	I
XTAL2	Crystal oscillator output	41	51	32	32	AO	0
LPF	LOOP FILTER	42	52	33	29	AB	0
HSYNC	H_SYNC	29	21	21	26	B	I
VSYNC	V_SYNC	30	20	22	27	B	I
/Reset	Device Reset	37	2	28	33	I	I
V[3:1]	OSD Video Output. Typically Drive B, G and R Outputs.	31,32,33	16,17,18	23,24,25	22,23,24	0	0
Blank	OSD Blank Output	34	19	26	25	0	0
HalfBlank[8]	OSD Half Blank Output	36	37	–	21	0	
RGB digital outputs[9]	R[1:0], G[1:0] and B[1:0] Outputs of the RGB Matrix	23,22,21, 20,19,18	12,11,6,5, 4,3	19,18,17,[11] 16,15,14	37,14,17, 16,19,18	0	
SCLK [10,11]	Internal Processor SCLK	24	13	20	20	0	
SCLK [11]	Internal Processor SCLK	–	–	–	L1	0	0
/IE	Data Strobe	–	–	–	K1	0	0
R/W	Read/Write	–	–	–	J3	0	0
EA[2:0]	External Registers Address Bus	–	–	–	L2,K3,H1	0	0

Notes:

1 ADC1 input pin is shared with Port 17, ADC2 input pin is shared with Port 00. ADC3 and ADC4 are not available on 40-Pin DIP version.
2 ADC0 and ADC4 have a clamp circuit that facilitates Composite Video input
3. PWM[8,7] is not available on the 40-Pin DIP version.
4 Port 0 [F.A] is not available on the 40-Pin DIP version
5 Port 19 is not available on the 40-Pin DIP version
6 SCL I/O pin is shared with Port 01 or Port 11
7. SCD I/O pin is shared with Port 02 or Port 12
8 HalfBlank output is a function shared with Port 0F HalfBlank output is not available on the 40-Pin DIP version
9. Digital RGB outputs and the internal SCLK are shared with Port 1 [5:0]
10. Internal processor SCLK is shared with Port 16
11 Not available on Z89314

Character Generation ROM

The required Character Graphics ROM size is dependent on the number of characters that are stored in memory. CGROM always begins at address 0000h, the first byte of ROM. The CGROM is configured in two banks selectable by setting a control bit. Each bank provides up to 256 characters with 16x16, 16x18 or 16x20 pixels matrix. Absolute maximum CGROM size is 9K words (9210 words).

Each character's pixel array is represented as 16 or 18 words of ROM storage,. Each word is 16 bits long. Pixel lines 1 to 16 are mapped sequentially to ROM addresses that are pointed to by the character pointer and a line number offset. In high resolution mode pixel lines 17 and 18 are offset to addresses beginning at the 4K boundary (1000h) for bank0 . Bank1 is mapped into ROM starting from address 1000h. Lines 17 and 18 of bank1 characters are mapped into ROM starting from address 2000h.

The first character in each bank should be a space character. In order to comply with the latter requirement it is recommended that bank0 character to be defined with 16x16 matrix. If the application requires bank0 characters to be in 16x18 pixel format, the first 32 characters of bank1 should be sacrificed and can't be used because line 17 and 18 of the bank0 characters will be mapped in their addresses and first eight characters of bank0 should not have any active dots in lines 17 and 18 in order to comply with the requirement that the first character in bank1 is a space character. For 16x20 format 32 characters need to be sacrificed.

In case, only bank0 of CGROM is used, there is no limitations on characters definition.

The CGROM data addressed by the contents of the character register is latched into the CGROM capture register. This contents of this register will contain a sequence of bits that represent whether the pixels on the pixel line currently being accessed for that character are on or off. This representation can be modified by the character multiplier to be two or three times normal character size by duplicating each bit in the word and expanding the representation to two or three of the character multiplier registers.

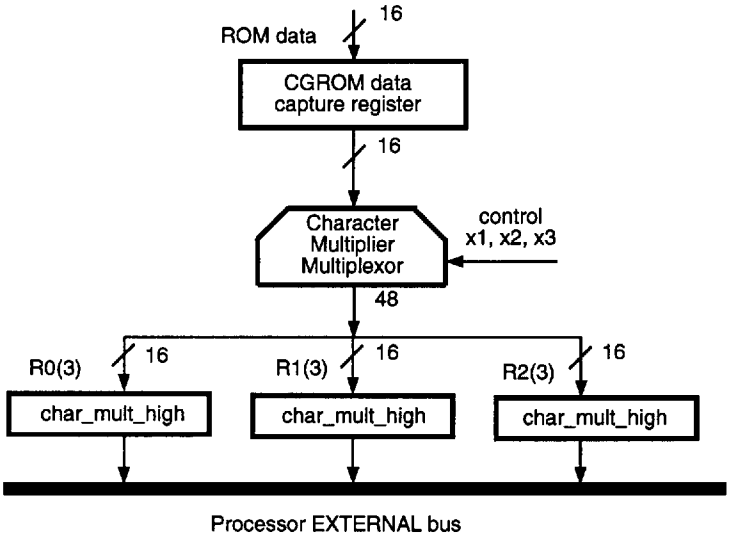

Figure 7. Character Multiplier

Character Multiplier Multiplexor

The character multiplier multiplexor can be controlled to double or triple the size of the pixel line presented to it from the CGROM capture register. It does not perform a numerical multiplication. The bits of the word contained in the capture register are duplicated to enlarge the character as it would be displayed horizontally on the screen. A model of the operation of the character multiplier multiplexor is shown below:

Capture Register Contents	abcdefghijklmnop	abcdefghijklmnop	abcdefghijklmnop
	char_mult_high	char_mult_mid	char_mult_low
x1 operation			abcdefghijklmnop
x2 operation	aabbccddeeffgghh	iijjkkllmmnnoopp	
x3 operation	aaabbbcccdddeeef	ffgggghhhiiijjjkk	kllmmmnnnooopppp

Tuner Control

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices such as digital channel tuning adjustment may be accessed through the industry standard I^2C port.

Voltage synthesis tuning systems are supported by 14-bit PWM (PWM9/10).

Video and Sound Attribute Control

Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports and one 14-bit pulse width modulated port[1].

Two 14-bit and up to eight 8-bit pulse width modulated are available to provide PWM control of analog signal levels such as volume or color.

Vertical Blank Interval Data Capture

Closed caption text can be decoded directly from the composite video signal with the assistance of the processor's digital signal processing capabilities and displayed on the screen. The character representation in this mode allows for simple attribute control through the insertion of control characters, and each word of RAM specifies two displayed characters.

The 4-bit flash A/D converter provides the ability to directly receive the composite video signal and process the closed caption text embedded in the signal. Signal processing can be applied directly to the signal to improve decoder performance.

I/O Ports

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register.

Up to[2] 26 configurable I/O pins are general-purpose pins that can be utilized to provide functions such as serial data I/O, LED control, key scanning, power control and monitoring and I^2C serial data communications.

Notes:

1. All nine PWM ports are only available in the 52-pin package. In the 40-pin package only six 8-bit and one 14-bit PWM output pins are available
2. The 52-pin device has one 10-bit port and one 16-bit port. The 40-pin device has one 10-bit port and one 9-bit port.
3. The 42-pin device has two 14-bit PWMs and five 8-bit PWMs.

REGISTERS (Continued)

Table 8. Register3 - R3 (0) I2C Interface Register

Reg field	Bit position	R	W	Data	Description
Command	fedc----------	R			Return"0"
			W	%DD	See footnote below the Table
Reset	----b----------	R			Return "0"
			W	1	Reset the I2C interface
				0	No effect
HI/LO_ Speed	-----a----------	R	W	1	High speed (400 kHz) - implemented in Rev. BA
				0	Low Speed (100 kHz)
Slave_ mode	------9---------	R		1	Slave mode
			W	0	Master mode
					No effect
Busy	-------8--------	R		1	I2C interface is busy
			W	0	I2C interface is idle
					No effect
Data	--------76543210	R		xx	Received data
			W	xx	Data to be sent

Master Mode

0000 - Send start bit followed by address byte <Data>
0010 - Send data byte specified in <Data>
0100 - Send <7> as an Ack to Slave after Data byte was received **IN READ FRAME** and receive next Data byte.
0110 - Send <7> as an Ack to Slave, do nothing
1001 - Set Slave address defined in <Data> (BE PREPARED FOR SLAVE MODE)
1100 - Receive Ack from Slave after Address byte was transmitted IN READ FRAME If Ack=0, receive Data, else (Ack=1) do nothing.
1110 - Send stop bit
0011,0101,0111,10xx,1101,1111 - RESERVED COMBINATIONS (SHOULD NOT BE USED).

Slave Mode

0010 - Send <Data> **IN READ FRAME** then latch Master's Ack
0100 - Send <7> = 0 as an Ack **IN WRITE FRAME.**
1110 - Send <7> -1 as an Nak **IN WRITE FRAME** OR Send <7> as an Ack **IN READ FRAME** If <7>=0, "Send <Data>" **IN READ FRAME** command should be executed next, else (<7>!=0) release the bus.
1001 - Set Slave address defined in <Data>
ALL THE RESET COMBINATIONS ARE RESERVED AND SHOULD NOT BE USED.

The received data is available for reading only when the "busy" bit is reset to "0". Upon POR the speed of the I2C interface is set to "low".

Upon POR, SMR and WDT reset both of these bits are reset to "0", which corresponds to SCLK frequency of 32 kHz.

In order to switch from 32 kHz SCLK to 12 MHz, the following procedure is recommended:

- Setting Fast _enable bit to a "1":
- Waiting for 300 .. 400 ms for 12 MHz PLL to be stabilized (approximately 15000 clock cycles)
- Setting Fast/Slow bit to a "1":

In order to switch from 12 MHz SCLK to 32 kHz, the following procedure is recommended:

- Setting Fast/Slow bit to a "0":
- Waiting for 32 µs for SCLK to be switched (approximately 360 clock cycles);
- Setting Fast_enable bit to a "0".

Table 15. Register2 - R2(1) WDT/STOP Mode Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba98765432--	R	W		Return"0" No effect
WDT_instr	--------------1-	R	W	1 0	Return "0" WDT enable, WDT reset No effect
STOP_instr	---------------0	R	W	1 0	Return "0" STOP instruction No effect

Upon POR, SMR and WDT reset the WDT is disabled. The WDT can be re-enabled only after the PVCO and SVCO are enabled and the part is switched into a Fast mode (SCLK = 12 MHz). Upon switching the part into a Slow mode (SCLK = 32 MHz) the WDT will be suspended and the WDT counter will resume count when the Fast operation will be restored. In the latter case an additional re-initialization of the WDT is not necessary.

REGISTERS (Continued)

Table 16. Register3 - R3(1) Standard Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fe----------	R	W		Return"0" No effect
Mask HV-SYNC	--d----------	R	W	1 0	Enable HV output HV input only - POR
Char_Size 16_18/20	---c----------	R	W	1 0	16x20 Char. Matrix 16x16 or 16x18 Char. - POR
Bank0_128/ Bank0_256	----b----------	R	W	1 0 POR	Extended RAM - 128 words Basic Bank - 256 words - POR condition
P07/ ComSYNC	-----a----------	R	W	1 0 POR	Composite SYNC output P07 I/O - POR condition
RGBC/ Port1	------9---------	R	W	1 0 POR	SCLK, R<1:0>,G<1:0>,B<1:0> P16,P08,P10,P13,P18,P15,P14
I2C_port	-------8--------	R	W	1 0	I2C data - P12, I2C clock - P11 I2C data - P02, I2C clock - P01
CGROM blank	--------7-------	R	W	1 0	Bank1 is selected (starts @ % 1000) Bank0 is selected (starts @ % 0000)
HBLANK/ P0f	---------6------	R	W	1 0	HBLANK output P0f output
OSD_ on/off	----------5-----	R	W	1 0	OSD is enabled OSD is disabled
RGB_ polarity	----------4----	R	W	1 0	Negative Positive
Positive/ Negative	----------3---	R	W	1 0	Negative HV-SYNC in output mode Positive HV-SYNC in output mode
SYNC/BLANK	----------2--	R	W	1 0	HV-SYNC outputs HV-SYNC outputs
25/30_Hz and HV polarity	----------10	R	W	10 00 10 00	Internal mode ONLY (TV Standard) 50 Hz/625 lines support 60 Hz/525 lines support External mode ONLY (HV Polarity) Positive Negative
External/ Internal	----------0	R	W	1 0	External (HV-SYNC in input mode) Internal (HV-SYNC in output mode)

Upon POR the HV-SYNC pins are configured in input mode and OSD_on/off bit is reset to "0".

There are two different bits which define polarity of HV-SYNC signals. Bit <3> defines polarity of the output signals on the pads of the device (it does not effect the internal HV-SYNC signals). Bit <1> defines the polarity of the external HV-SYNC signals and effects the synchronization of the device.

REGISTERS (Continued)

Table 25. Register2 - R2(3) Attributes Register (Write Only)

Reg field	Bit position	Data	Description
Reserved	f---------------	x	No effect
Background color	-edc------------	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	Black Blue Green Light Blue Red Magenta Yellow White
Foreground color NOT PALETTE MODE	----ba9---------	%D	Same as Background mode
Palette selection PALETTE MODE	----ba----------	0 0 0 1 1 0 1 1	Palette0 Palette1 Palette2 Palette3
2nd_underline PALETTE MODE	------9---------	1 0	Underline is active Underline is NOT active
1st_underline	-------8--------	1 0	Underline is active Underline is NOT active
Shift_video	--------7-------	1 0	Video signal is delayed by 8 pixels Standard character positioning
Transparent	---------6------	1 0	Transparent background Background color defined by "background color" field
Blinking	----------5-----	1 0	Blinking character Not blinking character
Italic	-----------4----	1 0	Italic character Not italic character
Color_ delay	------------32--	0 0 0 1 1 0 1 1	Char. color changes instantly Color changes with 4 pixels delay Color changes with 8 pixels delay Color chagnes with 12 pixels delay
Fringing	--------------1-	1 0	Fringing logic is enabled Fringing logic is disabled
Smoothing	---------------0	1 0	Smoothing logic is enabled Smoothing logic is disabled

REGISTER SUMMARY (Continued)

Table 36. Control Character Format (CCD Mode)

Reg field	Bit position	Data	Description
Control bit	7-------	1 0	Control character Display character
Transparernt	-6------	1 0	Transparent background Background color defined by "background color" field
Blinking	--5-----	1 0	Blinking character Not blinking character
Italic	---4----	1 0	Italic character Not italic character
Foreground color	----321-	000 001 010 011 100 101 110 111	Black Blue Green Light blue Red Magenta Yellow White
First underline	-------0	1 0	Underline attribute is active Underline attribute is inactive

By default background color in CCD mode is "black"; foreground and background color, blinking and italic attributes are delayed by 1/2 character, smoothing attribute is always enabled.

MODULE DESCRIPTIONS (Continued)

The size of memory used as CGROM depends on the number and resolution of characters stored in memory. 'N' represents the number of characters stored, ranging from 0 to 256. If characters are 16 x 18 or 16 x 20 pixels then the upper region of memory starting at the 4K boundary is used for character storage. If not it can be used as program memory.

Clocking Operation

The processor is able to operate from a number of clock sources.

1. Primary Phase Locked Loop V_{co} source (PVCO)
2. Secondary V_{co} phase-aligned with VSYNC timing (SVCO)
3. 32 kHz oscillator clock (OSC)

In addition the processor clock may be halted temporarily to allow clock selection or ROM accesses to be performed without disrupting normal operation of the processor.

PADS CONFIGURATION

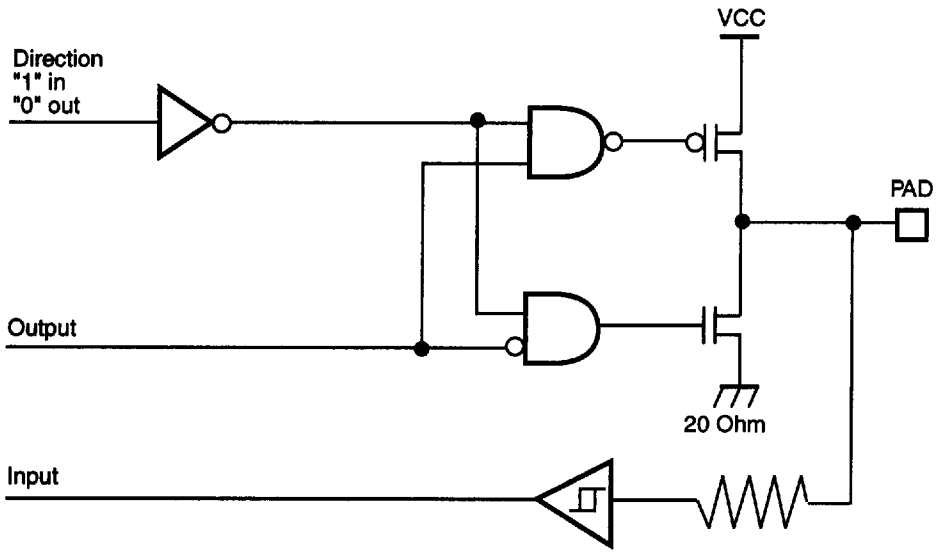

Figure 15. Type1 Bi-directional Port pins (Port 3, Port0f, Port 10, Port 13, Port 16, Port 18, Port 19, H-SYNC and V-SYNC)

PADS CONFIGURATION (Continued)

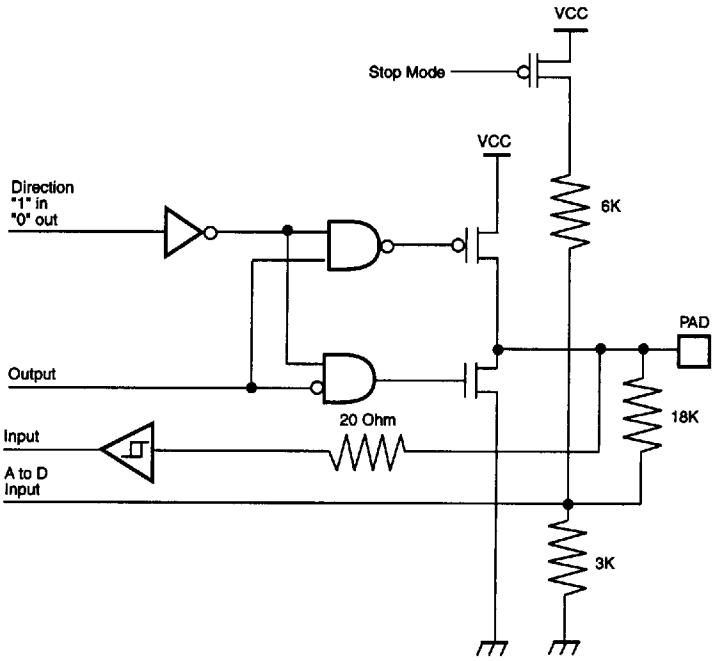

Figure 17. Type3 Bi-Directional Pins Multiplexed with AtoD Inputs (Port 00/AtoD2 and Port 17/AtoD1)

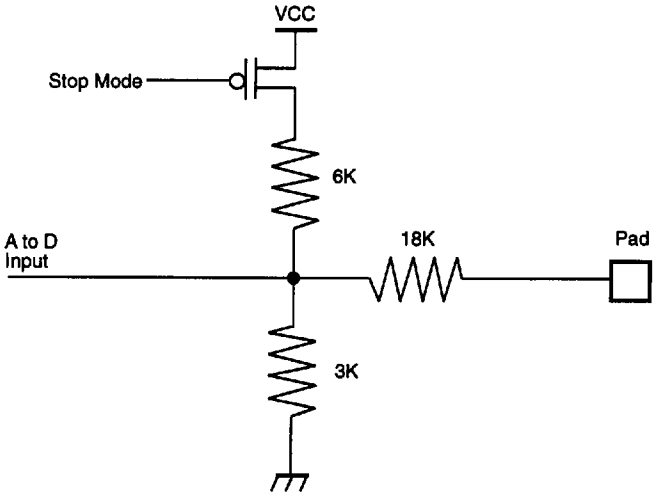

Figure 18. Type4 AtoD Input (AtoD3)

PADS CONFIGURATION (Continued)

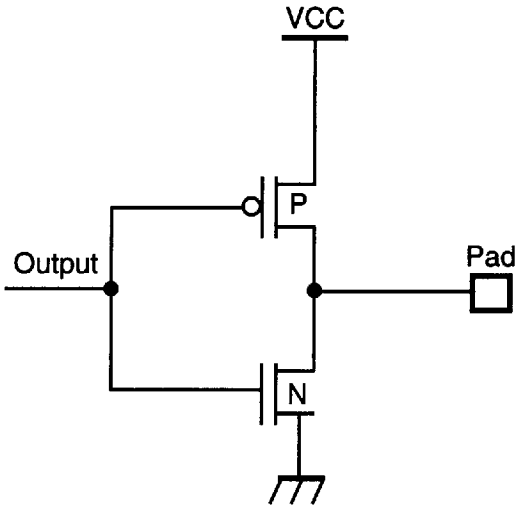

Figure 22. Type8 PWM9 and BLANK outputs; V1, V2, V3 outputs in digital mode

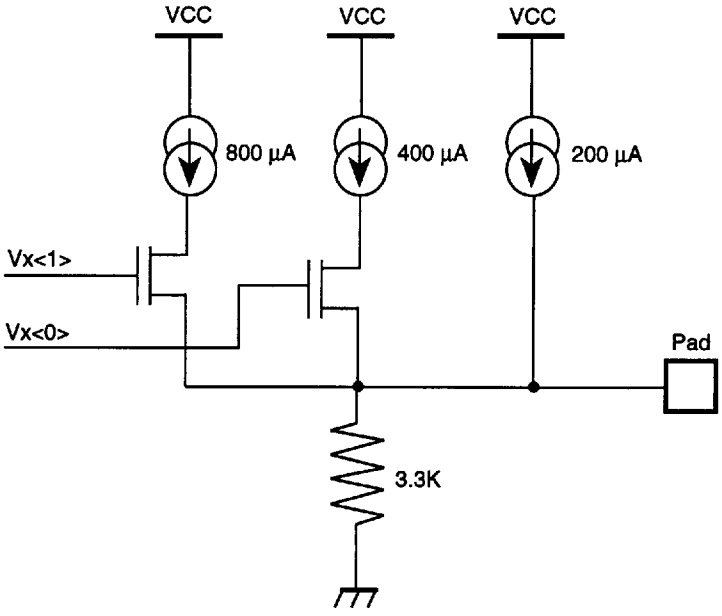

Figure 23. V1, V2 and V3 outputs in analog (palette) mode.

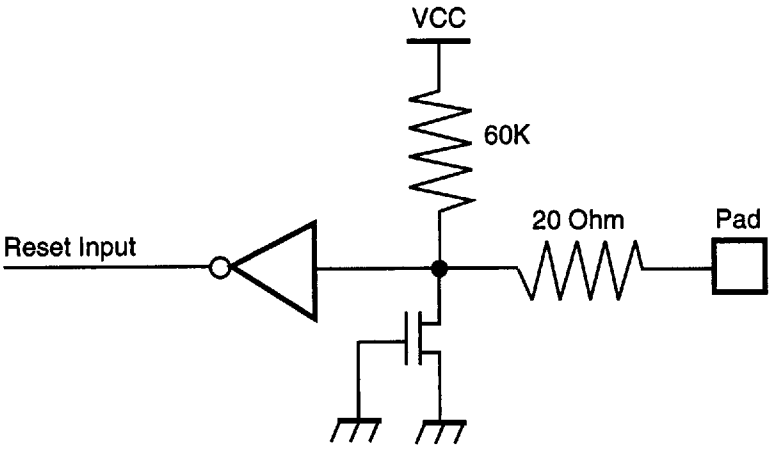

Figure 24. Reset Input

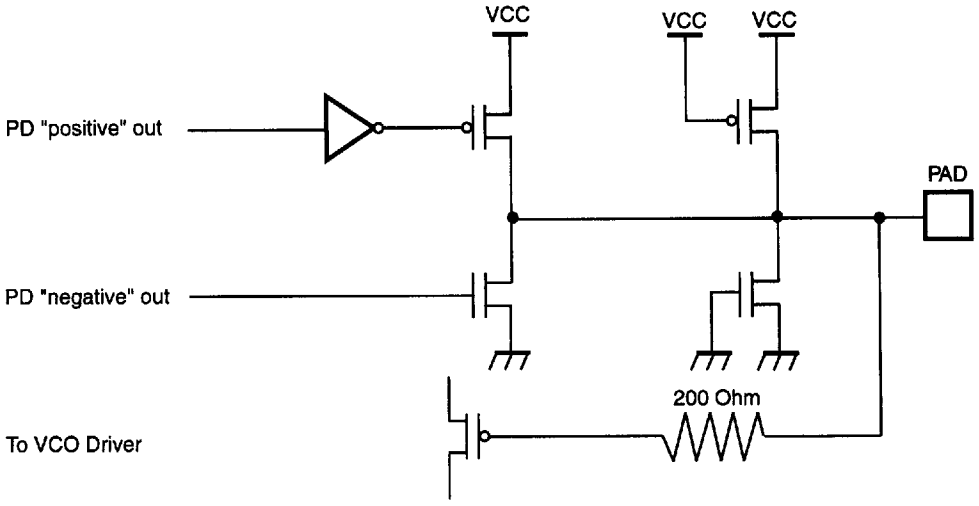

Figure 25. Loop Filter Pin

ABSOLUTE MAXIMUM/MINIMUM RATINGS

Sym	Parameter	Min	Max	Units	Conditions
V_{CC}	Power supply voltage	0	7	V	
V_{ID}	Input voltage	-0.3	V_{CC}+0.3	V	Digital inputs
V_{IA}	Input voltage	-0.3	V_{CC}+0.3	V	Analog inputs (A/D0..A/D4)
V_O	Output voltage	-0.3	V_{CC}+0.3	V	All push-pull digital outputs
V_O	Output voltage	-0.3	V_{CC} +8.0[1]	V	Open-drain PWM outputs (PWM1..PWM8)
I_{OH}	Output current high		-10	mA	one pin
I_{OH}	Output current high		-100	mA	All pins
I_{OL}	Output current low		20	mA	one pin
I_{OL}	Output current low		200	°C	All pins
T_A	Operating Temperature	0	70	°C	
T_A	Storage Temperature	-65	150	°C	

Note:
1. Momentary withstand voltage 16V

DC CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 4.5V to 5.5V; F_{OSC} = 32.768 kHz)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input voltage low	0	0.4	0.2 V_{CC}	V	
V_{IH}	Input voltage high	0.6 V_{CC}	3.6	V_{CC}	V	
V_{IH}	Input voltage high	0.75 V_{CC}	4.2		V	Reset pin only
V_{PU}	Maximum pull-up voltage			12	V	For PWM1..PWM8 only
V_{OL}	Output voltage low		0.16	0.4	V	@ I_{OL} = 1 mA
V_{OL}	Output voltage high	V_{CC} -0.9	4.75		V	@ IOL = 0.75 mA
V_{XL}	Input voltage XTAL1 low		1.0	0.3 V_{CC}	V	External clock generator driven
V_{XH}	Input voltage XTAL1 high	0.6 V_{CC}			V	
V_{HY}	Schmitt Hysteresis	0.3	0.5	0.75	V	XTAL1 input pin
I_{IR}	Reset input current		90	150	µA	VRL = 0V
I_{IL}	Input leakage	-3.0	0.01	3.0	µA	@ 0V and V_{CC}
I_{CC}	Supply current		60	100	mA	
I_{CCIE}	Supply current of the OTP		300	700	µA	Sleep mode @ 32 kHz
I_{CC1}	Supply current		100	300	µA	Sleep mode @ 32 kHz
I_{CC2}	Supply current		5	10	µA	Stop mode

RECOMMENDATIONS

Reset Circuit

The 32 kHz crystal oscillator of the Z89300 has a typical setting time of 800 ms. The reset will be supplied to the Microprocessor core only if the "reset" pin of the device is held "low" for more than 5 clock cycles. In case of the POR, the external RC circuit should provide a time delay of more than the longest possible setting time of the oscillator.

The typical value of the internal pull-up resistor is 60±20 Kohm.

Assuming that the RC constant of the reset circuit should be >1s, the value of the capacitor can be calculated from:

$$C=\frac{1}{R}=\frac{1}{60x10^{3}}=15x10^{-6}=15.0\ \mu f$$

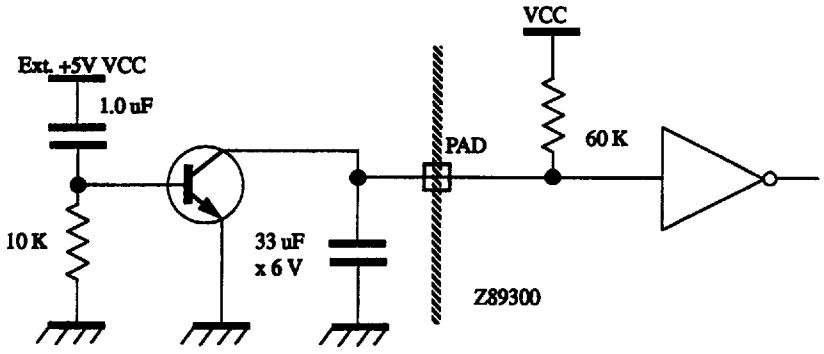

Figure 26. Reset Circuit

HSYNC (HFLYBACK) Recommended Timing (Continued)

CCD data captioning algorithm utilizes sampling of the Composite Video signal during line 21. In order for the CCD algorithm to recognize CCD burst (seven clock cycles of 503 kHz) certain timing relationships between incoming Composite Video signal and HFLYBACK should be maintained.

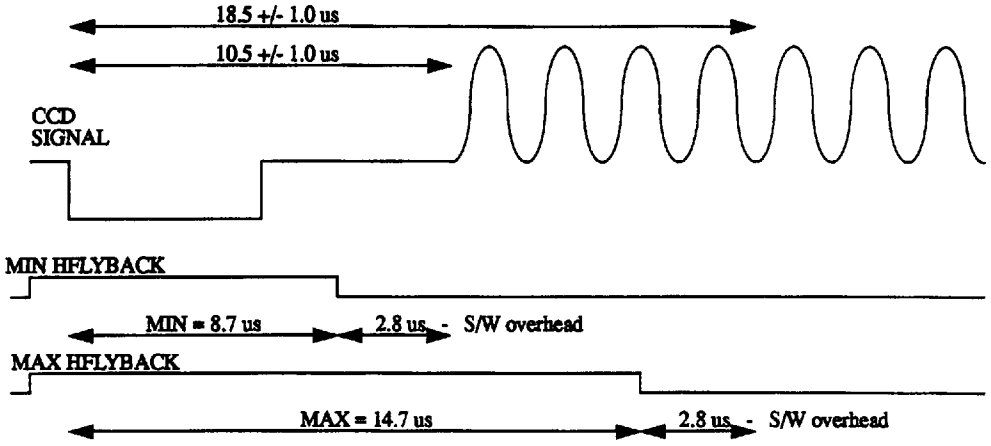

Figure 28. HFLYBACK Timing Diagram

In order to guarantee CCD algorithm performance, the time delay from leading edge of HSYNC to trailing edge of HFLYBACK should be maintained from 8.7 µs to 14.7 µs.

In order to comply with both OSD centering and CCD performance requirements, the time delay of trailing edge of HFLYBACK should be from 8.7 µs to 10.4 µs, which corresponds to HFLYBACK width of 9.7 µs....11.4 µs if leading edge of HFLYBACK is 1.0 µs ahead of leading edge of HSYNC.

Clamp Positioning

The black level of Composite Video signal fed to Z89300 should be set to Ref - voltage of the A to D. In order to shift the DC level of the incoming signal, there is an internal clamp in the Z89300. The clamp pulse should be located during the back porch of the HSYNC.

Clamp position is defined by the "Position" field (bits <6:0>) in Clamp Position register R0(1). The width of clamp pulse cannot be modified and is set to 1 µs. The value which can be assigned to the "Position" field should be >10% and <7%f. The time interval between the leading edge of the H-FLYBACK and the beginning of the clamp pulse can be calculated from:

$$Tdelay = Position \times \frac{1}{Tsclk} = Position \times 82\ ns$$

Because the clamp pulse is generated from the leading edge of the incoming HFLYBACK signal, there are certain constraints imposed on the relative positioning of the leading edge of HFLYBACK relative to leading edge of HSYNC.

By setting the "Position" field of Clamp Position register, the clamp pulse can be positioned at 1.3 µs....10.5 µs after the leading edge of HFLYBACK.

The optimal position of the clamp pulse is 6.5 µs after the leading edge of the HSYNC (in the middle of the back porch interval). Wide setting of "Position" field allows for possible variations in HFLYBACK positioning of up to +4.0 µs....-5.0 µs.

Practical example of registers setting implementation

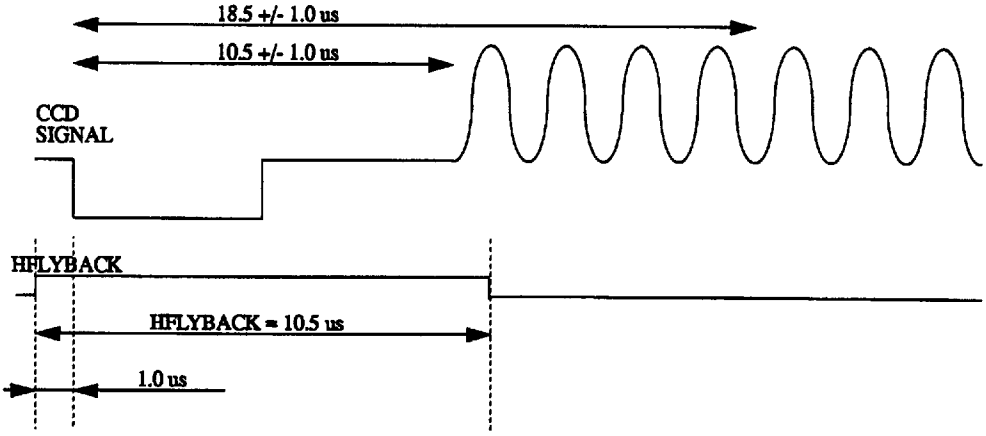

Figure 29. Register Settling Timing Diagram

In this example the time delay from leading edge of HSYNC to trailing edge of HFLYBACK is specified to be 9.5 µs.

In order to position the clamp in the middle of the back porch, the "Position" field of Clamp Position register should be set to 57% (7.2 µs).

The CCD data capture algorithm requirements are satisfied and this particular setting corresponds to the middle of the operating range.

ORDERING INFORMATION

Z89300

24 MHz
42-Pin DIP
Z8930024PSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
P = Plastic DIP

Temperature
S = 0°C to 70°C

Speeds
24 = 24 MHz

Environmental
C = Plastic Standard

Example:

Z 89300 24 P S C is a Z89300, 24 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 24 — Speed
- 89300 — Product Number
- Z — Zilog Prefix