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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	TV Controller
Core Processor	Z8
Program Memory Type	OTP (24kB)
Controller Series	Digital Television Controller (DTC)
RAM Size	640 x 16
Interface	-
Number of I/O	26
Voltage - Supply	4.5V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Through Hole
Package / Case	52-DIP
Supplier Device Package	52-SDIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8930112psc

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Table 1. Zilog Z893xx Product Family

Device	Application	Feature Summary							
		ROM (word)	RAM (word)	Pkg.	I^2C	IR Capture	ADC	Bit I/O	PWM
Z89300	TV Receiver Controller OTP	24K OTP	640	40-DIP	Yes	Yes	3-ch	19	7
Z89301	TV Receiver Controller OTP	24K OTP	640	50-SDIP	Yes	Yes	4-ch	26	9
Z89309	TV Receiver Controller ICE device	Bond Out	640	124 PGA	Yes	Yes	6-ch	26	10
Z89302	TV Receiver Controller	24K Mask	640	40-DIP	Yes	Yes	3-ch	19	7
Z89303	TV Receiver Controller	24K Mask	640	52-SDIP	Yes	Yes	4-ch	26	9
Z89313	TV Receiver Controller	24K Mask	640	52-SDIP	Yes	Yes	4-ch	26	9
Z89304	TV Receiver Controller	16K Mask	640	40-DIP	Yes	Yes	3-ch	19	7
Z89305	TV Receiver Controller	16K Mask	640	52-SDIP	Yes	Yes	4-ch	26	9
Z89306	TV Receiver Controller	12K Mask	640	40-DIP	Yes	Yes	3-ch	19	7
Z89307	TV Receiver Controller	12K Mask	640	52-SDIP	Yes	Yes	4-ch	26	9
Z89331	One Time Programmable	24K OTP	640	42-SDIP	Yes	Yes	5-ch	20	7
Z89332	TV Receiver Controller	24K Mask	640	42-SDIP	Yes	Yes	5-ch	20	7
Z89336	TV Receiver Controller	12K Mask	640	42-SDIP	Yes	Yes	5-ch	20	7
Z89314	TV Receiver Controller	16K Mask	512	40-DIP	No	Yes	3-ch	19	7
Z89318	TV Receiver Controller	10K Mask	512	40-DIP	No	Yes	3-ch	19	7

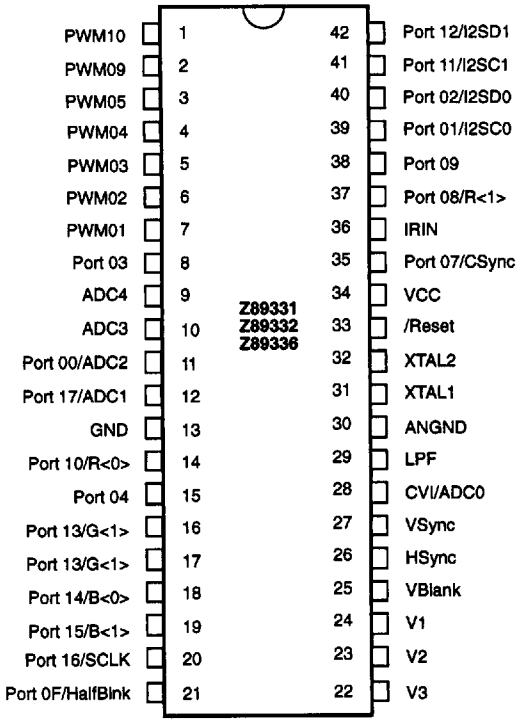


Figure 4. Z89332/336 42-Pin DIP

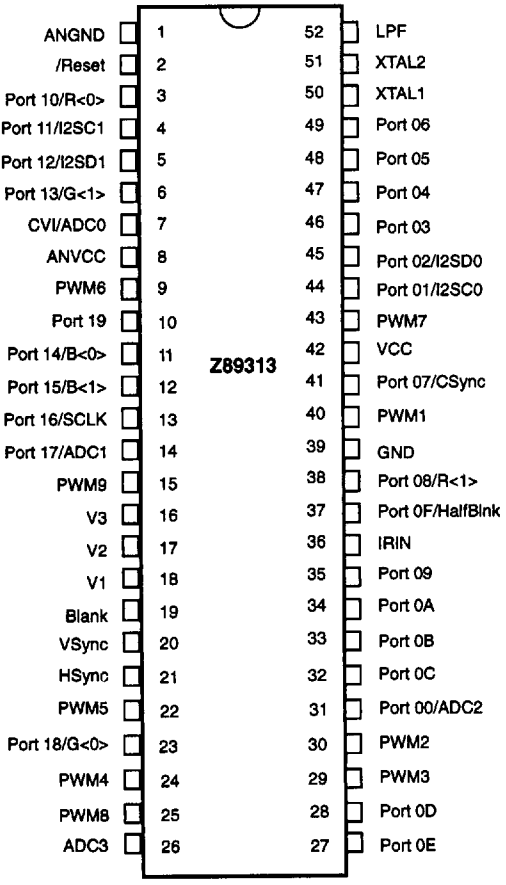


Figure 5. Z89313 52-Pin DIP

PIN IDENTIFICATION

Table 2. Pin Identification

Pin		Package				Configuration	
Name	**Function**	**Z89301/3/5/7 52-pin SDIP**	**Z89313 52-pin SDIP**	**Z89300/02/4/6 14/18 40-pin DIP**	**Z89331/332 /336 42-pin DIP**	**Direction**	**Reset**
VCC	+5 Volts	17,38	8,42	29,–,	34	PWR	–
GND	0 Volts	10,40	1,39	31,–,	13,30	PWR	–
IRIN	Infrared Remote Capture Input	2	36	2	36	I	I
ADC [5:0][1]	4-Bit Analog to Digital Converter input[2].	44,–,–,6, 35,43	–,–,26,31 14,7	–,–, –, 4,27 34	–, 9,10, 11,12,28	AI	I
PWM10, PWM9	14-Bit Pulse Width Modulator Output	–,1	–,15	–,1	1,2	OD	0
PWM[8:1][3]	8-Bit Pulse Width Modulator Output	52,51,50,49, 48,47,46,45	25,43,9,22, 24,29,30,40	–,–.40,39. 38,37,36,35	–,–, –,3,4, 5,6,7	OD	0
Port0[F:0][4]	Bit Programmable Input/Output Ports	36,5,28,27, 26,25,16,15, 14,13,12,11, 9,8,7,6	37,27,28,32, 33,34,35,38, 41,49,48,47, 46,45,44,31,	–,–,–,–,–,–, 13,12,11, 10,9,8,7, 6,5,4	21,–,–,–, –,–,38,37, 35,–,–,15, 8,40,39,11	B	I
Port1[9:0][5]	Bit Programmable Input/Output Ports	4,3,35,24, 23,22,21, 20,19,18	10,23,14, 13,12,11, 6,5,4,3	–,3,27, 20,19,18, 17,16,15, 14	–,16,12, 20,19,18, 17,42,41, 14	B	I
SCL[6]	I^2C Clock I/O	7 or 19	44 or 4	5 or 15	39 or 41	BOD	
SCD[7]	I^2C Data I/O	8 or 20	45 or 5	6 or 16	40 or 42	BOD	
XTAL1	Crystal oscillator input	39	50	30	31	AI	I
XTAL2	Crystal oscillator output	41	51	32	32	AO	0
LPF	LOOP FILTER	42	52	33	29	AB	0
HSYNC	H_SYNC	29	21	21	26	B	I
VSYNC	V_SYNC	30	20	22	27	B	I
/Reset	Device Reset	37	2	28	33	I	I
V[3:1]	OSD Video Output. Typically Drive B, G and R Outputs.	31,32,33	16,17,18	23,24,25	22,23,24	0	0
Blank	OSD Blank Output	34	19	26	25	0	0
HalfBlank[8]	OSD Half Blank Output	36	37	–	21	0	
RGB digital outputs[9]	R[1:0], G[1:0] and B[1:0] Outputs of the RGB Matrix	23,22,21, 20,19,18	12,11,6,5, 4,3	19,18,17,[11] 16,15,14	37,14,17, 16,19,18	0	
SCLK [10,11]	Internal Processor SCLK	24	13	20	20	0	
SCLK [11]	Internal Processor SCLK	–	–	–	L1	0	0
/IE	Data Strobe	–	–	–	K1	0	0
R/W	Read/Write	–	–	–	J3	0	0
EA[2:0]	External Registers Address Bus	–	–	–	L2,K3,H1	0	0

Notes:

1 ADC1 input pin is shared with Port 17, ADC2 input pin is shared with Port 00. ADC3 and ADC4 are not available on 40-Pin DIP version.
2 ADC0 and ADC4 have a clamp circuit that facilitates Composite Video input
3. PWM[8,7] is not available on the 40-Pin DIP version.
4 Port 0 [F.A] is not available on the 40-Pin DIP version
5 Port 19 is not available on the 40-Pin DIP version
6 SCL I/O pin is shared with Port 01 or Port 11
7. SCD I/O pin is shared with Port 02 or Port 12
8 HalfBlank output is a function shared with Port 0F HalfBlank output is not available on the 40-Pin DIP version
9. Digital RGB outputs and the internal SCLK are shared with Port 1 [5:0]
10. Internal processor SCLK is shared with Port 16
11 Not available on Z89314

System Description (Continued)

Analog functions such as volume and color controls can be controlled by the pulse width modulated outputs from the Z89300. Other digital controls such as channel fine tuning can be controlled through the serial I²C bus.

An infrared remote control receiver can be directly decoded through the capture register, and keypad input can be scanned by directly controlling I/0 pins as keyscan ports.

The processor clock is provided by referencing an internal phase locked loop to an external 32.768 kHz crystal oscillator, which enables EMI emissions from the clock circuitry to be minimized. The internal system clock frequency can be software selected to be up to 12.059 MHz in normal operation or 32.768 kHz in low power mode. The Z89300 can also be placed in STOP mode, suspending processor clocking for power down suspension of operation.

Program, display and character graphics memories are on the chip, eliminating the need for any external memory components. Characters can be displayed as two or three times normal size. Smoothing and fringing circuits are provided to enhance display appearance.

The device is available in a one-time-programmable version as well as a 12K, 16K and 24K masked ROM sizes and is available in 40 and 52-pin DIP packages

FUNCTIONAL DESCRIPTION

Core Processor

The processor core is a high-performance RISC processor.

The powerful 12 MHz Z89C00 RISC processor core allows the user to control the on-board peripheral functions and registers using the standard processor instruction set.

The Z89300 controller processor core is a Z89C00 high performance 16-bit RISC processor optimized for data processing and transfer. 16-bit peripheral registers are programmed to control the operation of the peripheral devices. Two banks of 256 words each of RAM in the processor core can be used for video character sequence storage. Program and character graphics are stored in the PROM.

External Registers

The C00 module is capable of directly accessing up to eight external registers using only the three external register address signals that are normally available. In this implementation, two user signals are combined with the register address signals to provide the ability to address four banks of eight registers each. The most speed critical registers are located together in bank 3. In this document all external registers will be referred to as follows:

RX(Y)<Z>;

where - X is a register number within a register bank;
Y is a bank number;
Z is a bit field number

The user can select a register by setting the user bits to define the bank that the register is in and then specifying the address of the register on the external register address bus.

The external registers reside on the chip and are used to control the operation of all of the peripheral modules of the device. By reading or writing to the fields in the external registers the user can interact with the peripheral devices of the chip.

Interrupt Control

The Z89C00 core has three external interrupt signals that are used to provide interrupt signalling from the Z89300 peripheral modules to the core. In order to provide handling of all four of the device's interrupt sources, that is, horizontal sync (H-SYNC), vertical sync (V-SYNC) and the two timers (1s/CAP), the latter interrupt source is treated as a vectored interrupt where the vector is a bit in a register that selects one of the two timers. The more critical synchronization interrupts are non-vectored.

Interrupt priorities are programmable and each interrupt can be masked by setting fields in the external registers.

The timer interrupts are wire ORed to a single interrupt input. When a timer generates an interrupt it sets the condition of the interrupt vector flag depending on which timer initiated the interrupt request. When the processor is ready to service the interrupt request, it reads the vector bit and executes the appropriate service routine.

When the Z89300 receives an interrupt request from one of the non-vectored interrupt sources it directly executes the interrupt service routine for that source.

Programmable Read Only Memory

The programmable ROM is designed to provide storage for both program memory PROGRAM and character set graphics pixel arrays (CGROM). The address boundaries between these applications is dependent on the storage required for character graphics.

The program ROM section can in theory be accessed anywhere in the addressable ROM space. However, since CGROM usually start at location 0000h, PROGRAM will reside in the higher address locations. The maximum available ROM space for program memory depends on the ROM reserved for CGROM for an application and the ROM size of the device selected. Memory accesses can be considered to be PROGRAM accesses when the ROM address is being provided by the processor ROM address bus.

The Z89300 ROM is either 10K, 12K, 16K or 24K words, depending on the part selected. The first byte of ROM is located at address 0000h, and is mapped as shown in Table 3.

Table 3. PROM Addressing

ROM Size (Words)	Low Address	High Address
12K	000h	2FFFh
16K	000h	3FFFh
24K	000h	5FFFh

The address multiplexor can be selected so that either the processor external address bus or the character registers provide the physical ROM address. For PROGRAM access the processor external address bus should be selected, otherwise the access is to CGROM space.

Clocks and Control

The Z89300 has two internal 12 MHz VCOs (PVCO - primary VCO &SVCO - Secondary - VCO) that are referenced to a 32 kHz internal oscillator to provide the system clock (SCLK). SCLK is generated internally by dividing the frequency of an appropriate oscillator (PVCO or SVCO) by 2. The frequency of the SCLK after POR is 12.058 MHz. In SLEEP mode the controller uses the 32 kHz clock for the system clock to reduce power consumption. The processor can be suspended by placing it into STOP mode when main power is not available for minimal power consumption.

An external crystal controls the internal 32 kHz oscillator, and is used as the clock source for the internal 24 MHz phase locked loop. The PLL provides the internal 12 MHz system clock for processor operation.

On-Screen Display

The extensive character attributes can be controlled in two modes by the on-screen display controller: character control mode for maximum display control flexibility and closed caption mode for optimum display of closed caption text.

Character control mode provides access to the full set of attribute controls. Each word of RAM specifies a single displayed character and basic character attributes, allowing the modification of attributes on a character-by-character basis. The insertion of control characters allows control of other character attributes.

The fully customizable 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes, including underlining, italics and blinking, eight foreground and background colors, character position offset delay, and background transparency. The 16-bit display character representation allows the modification of some key attributes on a character by character basis. A character's pixel array is stored as a 16,18 or 20 word representation in Character Graphics ROM (CGROM). The ROM contents are referenced by a 16-bit word stored in video RAM (VRAM) defining the character type and its key attributes.

Additional hardware provides the capability to display two and three times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Fringing circuitry can be activated to improve the visibility of text by surrounding the character lines with a one pixel border.

RGB outputs provide the direct video signals, and a blanking output is provided to control the video multiplexor. Dot clock and vertical line synchronization is normally obtained from H_FLYBACK and V_FLYBACK, but can be generated by the Z89300 and driven to the external deflection unit through the bi-directional SYNC ports when external video synchronization signals are not present.

REGISTERS (Continued)

Table 8. Register3 - R3 (0) I2C Interface Register

Reg field	Bit position	R	W	Data	Description
Command	fedc----------	R			Return"0"
			W	%DD	See footnote below the Table
Reset	----b----------	R			Return "0"
			W	1	Reset the I2C interface
				0	No effect
HI/LO_ Speed	-----a----------	R	W	1	High speed (400 kHz) - implemented in Rev. BA
				0	Low Speed (100 kHz)
Slave_ mode	------9---------	R		1	Slave mode
			W	0	Master mode
					No effect
Busy	-------8--------	R		1	I2C interface is busy
			W	0	I2C interface is idle
					No effect
Data	--------76543210	R		xx	Received data
			W	xx	Data to be sent

Master Mode

0000 - Send start bit followed by address byte <Data>
0010 - Send data byte specified in <Data>
0100 - Send <7> as an Ack to Slave after Data byte was received **IN READ FRAME** and receive next Data byte.
0110 - Send <7> as an Ack to Slave, do nothing
1001 - Set Slave address defined in <Data> (BE PREPARED FOR SLAVE MODE)
1100 - Receive Ack from Slave after Address byte was transmitted IN READ FRAME If Ack=0, receive Data, else (Ack=1) do nothing.
1110 - Send stop bit
0011,0101,0111,10xx,1101,1111 - RESERVED COMBINATIONS (SHOULD NOT BE USED).

Slave Mode

0010 - Send <Data> **IN READ FRAME** then latch Master's Ack
0100 - Send <7> = 0 as an Ack **IN WRITE FRAME.**
1110 - Send <7> -1 as an Nak **IN WRITE FRAME** OR Send <7> as an Ack **IN READ FRAME** If <7>=0, "Send <Data>" **IN READ FRAME** command should be executed next, else (<7>!=0) release the bus.
1001 - Set Slave address defined in <Data>
ALL THE RESET COMBINATIONS ARE RESERVED AND SHOULD NOT BE USED.

The received data is available for reading only when the "busy" bit is reset to "0". Upon POR the speed of the I2C interface is set to "low".

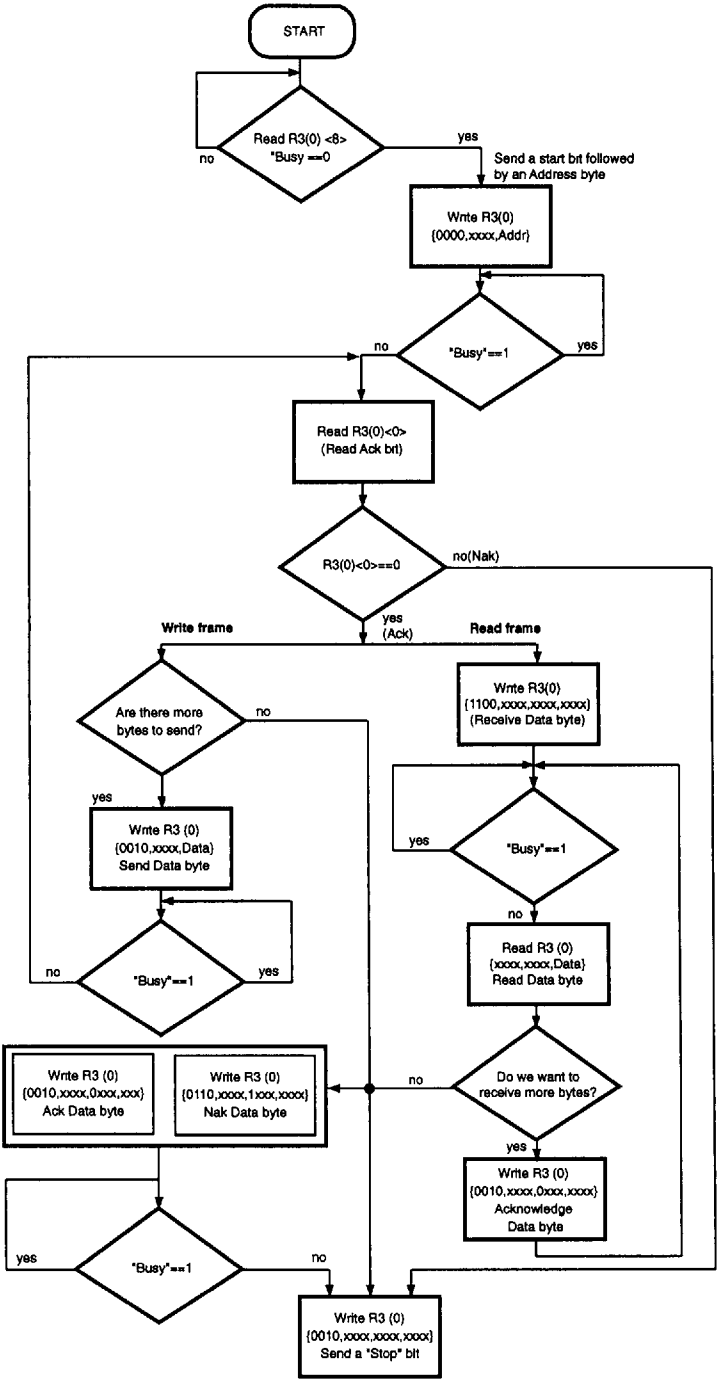


Figure 8. Master Mode

Table 9. Register4 - R4(0) Port 0 Data Register

Reg field	Bit position	R	W	Data	Description
Port_data	fedcba9876543210	R		xxxx	If port is configured in input mode - the input data on the port pins If Port is configured in Output mode - the data actually written to the port
			W	xxxx	Data

Table 10. Register5 - R5 (0) Port 1 Data Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba----------	R			Return "0"
			W		No effect
Port_data	------9876543210	R		xxxx	If port is configured in input mode - the input data on the prot pins If Port is configured in Output mode - the data actually written to the port
			W	xxxx	Data

Table 11. Register6 - R6(0) Port 0 Direction Register

Reg field	Bit position	R	W	Data	Description
Port_ direction	fedcba9876543210	R	W	xxxx	1 Input mode for corresponding bit 0 Output mode for corresponding bit

Table 19. Register6 - R6(1) Clock Switch Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba9876------	R	W		Return "0" No effect
SVCO/PVCO	----------5-----	R	W	1 0 1 0	SCLK=SVCO (flag) SCLK=PVCO (flag) Switch SCLK to PVCO No effect
No_switch	----------4----	R	W	1 0	SCLK=PVCO, NO clock switching Clock switching is enabled
H_position	----------3210	R	W	%D	Defines delay of Hint by 4D SCLK cycles

The clock switch control register defines the source of SCLK fed into the Z89C00 core. The block diagram of the clock switch circuit is presented on figure below.

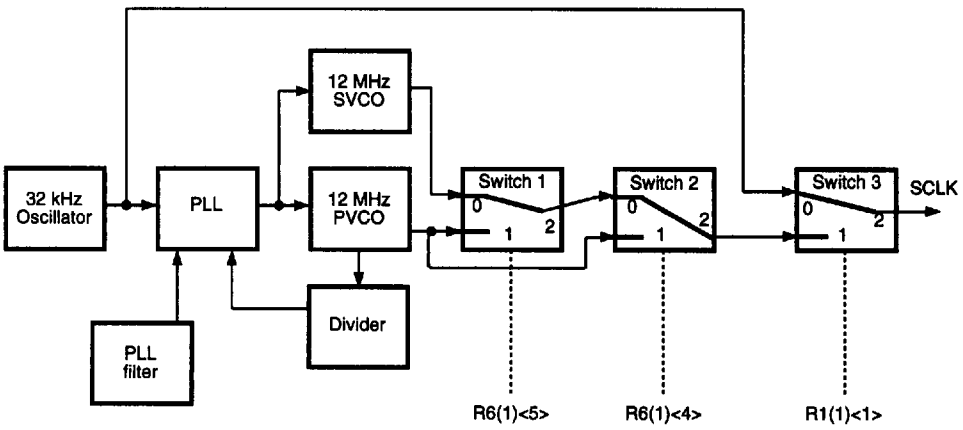


Figure 10. Clock Switch Control Register

Switch1 positioning defines the source of the signal on terminal 0 of switch2. Switch2 is used to override the frequency setting in "no_switch" mode. Whenever "no_switch" mode is set, switch1 continues to switch between PVCO and SVCO. Because of that it is not recommended to switch2 if it is not guaranteed that PVCO signal is fed to terminal0 of switch2. The recommended sequence is as follows:

1. Switch SCLK to PVCO
2. Wait for 2..3 SCLK cycles to ensure that the SCLK is switched
3. Switch R6 (1) <4> to enable/disable "no_switch" mode.

Bank 2 (PWM Registers)

Table 22. Register0. Register7 - R0(2)..R7(2) PWM1..8 Registers

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba98--------	R W			Return "0" No effect
PWM_data	--------76543210	R	W	xx	8-bit PWM data

All of the PWMs have open-drain outputs. The outputs of all PWMs are staged by one PVCO clock. The repetition frequency of PWM output signals can be calculated from:

$$Fpwm = \frac{Fpvco}{8(256)} = \frac{12\ MHz}{2048} = 6\ kHz$$

Bank 3 (On-Screen Display [OSD] Registers)

Table 23. Register 0. Register2 - R0(3).R2(3) Character Multiplier Registers (Read Only)

Reg field	CGROM data	Reg addr.	Description
cgrom_x2_hi cgrom_x3_hi	ffeeddccbbaa9988 ffeeddccbbaa9988	R0(3)	High word of double size character R4(3)<6>=0 High word of triple size character R4(3)<6>=1
cgrom_x2_lo cgrom_x3_mid	7766554433221100 aa99988877766655	R1(3)	Low word of double size character R4(3)<6>=0 Middle word of triple size character R4(3)<6>=1
cgrom_x1 cgrom_x3_lo	fedcba9876543210	R2(3)	Single size character R4(3)<6>=0 Low word of triple size character R4(3)<6>=1

Table 24. Register0..Register1-R0(3)..R1(3) Shift Registers (Write Only)

Reg field	CGROM data	Reg addr.	Description
current_reg	fedcba9876543210	R0(3)	current line shift register
next/previous_reg	fedcba9876543210	R1(3)	next/previous line shift register

These register should be loaded with video data once every 16 cycles. The current line register should be loaded first, followed by next/previous register during the next cycle. The next/previous register should be loaded only if smoothing/fringing attributes are activated for the current character. If both of those registers are not loaded, the space character will be displayed. There is no difference between loading "000" h into either of the registers or not loading them at all.

REGISTERS (Continued)

Table 25. Register2 - R2(3) Attributes Register (Write Only)

Reg field	Bit position	Data	Description
Reserved	f---------------	x	No effect
Background color	-edc------------	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	Black Blue Green Light Blue Red Magenta Yellow White
Foreground color NOT PALETTE MODE	----ba9---------	%D	Same as Background mode
Palette selection PALETTE MODE	----ba----------	0 0 0 1 1 0 1 1	Palette0 Palette1 Palette2 Palette3
2nd_underline PALETTE MODE	------9---------	1 0	Underline is active Underline is NOT active
1st_underline	-------8--------	1 0	Underline is active Underline is NOT active
Shift_video	--------7-------	1 0	Video signal is delayed by 8 pixels Standard character positioning
Transparent	---------6------	1 0	Transparent background Background color defined by "background color" field
Blinking	----------5-----	1 0	Blinking character Not blinking character
Italic	-----------4----	1 0	Italic character Not italic character
Color_ delay	------------32--	0 0 0 1 1 0 1 1	Char. color changes instantly Color changes with 4 pixels delay Color changes with 8 pixels delay Color chagnes with 12 pixels delay
Fringing	--------------1-	1 0	Fringing logic is enabled Fringing logic is disabled
Smoothing	---------------0	1 0	Smoothing logic is enabled Smoothing logic is disabled

REGISTERS (Continued)

Table 28. Register4 - R4(3) OSD Control Register

Reg field	Bit position	R	W	Data	Description
Underline	fe----------	R	W	1x 0x x1 x0	Second underline is active Second underline is inactive First underline is active First underline is inactive
OSD/CCD	--d----------	R	W	1 0	OSD mode CCD mode
CCD_ top/btm	---c----------	R	W	1 0	Blinking character is displayed Blinking character is NOT displayed (hidden)
Italic_shift	-----ba98-------	R	W	x	Defines delay of the character
Blink on/off	---------7------	R	W	1 0	Blinking character is not displayed Blinking character is displayed (hidden)
MPX_bus	---------65-----	R	W	0 0 0 1 1 0 1 1	x1 character size x2 character size x3 character size Reserved
CGROM scan_line	----------43210	R	W	%D	Defines CGROM addressing IN REV.BA also defines italic shift

The Underline field should be set by the firmware during the line/lines of the OSD when the second/first underline is active. The bits will be ANDed with the 2nd/1st underline active fields of data loaded into an attribute register R2(3) allowing character on screen to be underlined.

Italic shift field defines the delay of current video data. Typically it is used to generate italic characters. The firmware decrements by "1" the value of the Italic_shift field for each consecutive line. The video signal will be delayed only for those characters, which have R2(3)<4>("italic") bit set to a "1"

Table 29. Register5 - R5(3) Capture Register

Reg field	Bit position	R	W	Data	Description
Capture_data	fedcba9876543210	R	W	%xxxx	16-bit captured data No effect

REGISTERS (Continued)

Table 31. Register7 - R7(3) Output Palette Control Register

Reg field	Bit position	R	W	Data	Description
Reserved HBLANK_Delay	fedc----------	R W			Return "0" Delay Value No effect %00 - POR Condition
Background_on/off	----b----------	R	W	1 0	Background is on Background is off - POR condition
Background_color	-----a98--------	R	W	%D	Defines the color of the background (the same as the Palette)
Reserved	--------7-------	R W			Return "0" No effect
StarSight palette	---------6------	R	W	0 1 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	Palette is defined by bits <5..0> StarSight palette: Black V1=0; V2=0; V3=0; Blue V1=0; V2=99% V3=99%; Green V1=66%, V2=99%; V3=99%; Grey V1=66%; V2=66%; V3=66%; Red V1=99%; V2=33%; V3=33%; LtYell V1=99%; V2=99%; V3=0; Yellow V1=99%; V2=99%, V3=0; White V1=99%; V2=99%; V3=99%;
Palette_ red (V1)	----------54----	R	W	0 0 0 1 1 0 1 1	66% red 66% red + 33% blue 66% red + 33% green 66% red + 33% blue + 33% green
Palette_ green (V2)	------------32--	R	W	0 0 0 1 1 0 1 1	66% green 66% green + 33% blue 66% green + 33% red 66% green + 33% blue + 33% red
Palette_ blue (V3)	--------------10	R	W	0 0 0 1 1 0 1 1	66% blue 66% blue + 33% green 66%blue + 33% red 66% blue + 33% green + 33% red
Digital_ mode	----------543210	R	W	000000	Outputs V1, V2, V3 correspond to 100% red, green, and blue outputs

Upon POR the Output palette register is set to "0" - digital output.

Note: If bit R7(3)<6> is set to "1", while bits R7(3)<5:0> are reset to a "0". the outputs V1, V2 and V3 of Z89300 will be switched into a "Digital mode".

A to D and Clamp Circuit Operation (Recommended Practice) (Continued)

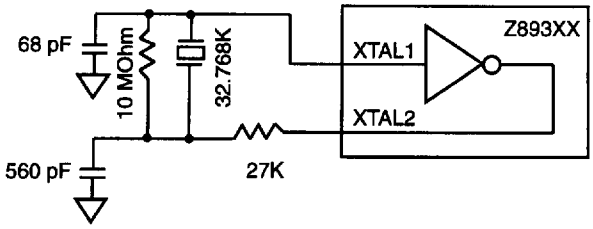


Figure 12. 32K Oscillator Recommended Circuit

V1, V2, V3 Analog Output

Table 38. V_{cc} = 5.25V

VCC=5.25V	Condition	Limit
Output Voltage	bit=11	4.55V ± 0.25V
	bit=10	3.25V ± 0.2V
	bit=01	1.95V ± 0.15V
	bit=00	0.65V ± 0.1V
Settling Time	70% of DC level, 10 pf load	<50 nsec

Table 39. V_{cc} = 4.75V

VCC=5.25V	Condition	Limit
Output Voltage	bit=11	3.90V ± 0.25V
	bit=10	2.90V ± 0.2V
	bit=01	1.90V ± 0.15V
	bit=00	0.1V ± 0.1V
Settling Time	70% of DC level, 10 pf load	<50 nsec

V1, V2, V3 Analog Output (Continued)

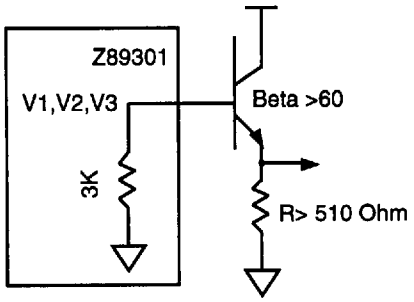


Figure 13. Recommended Circuit

MODULE DESCRIPTIONS

Z89COO Core Processor Module

Memory Organization

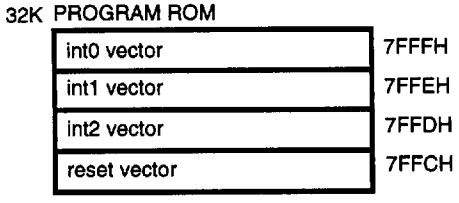
The C00 core has access to three types of memory that are of interest here:

1. **Program Read Only Memory (PROGRAM)**
   Size: 12K, 16K or 24K words (16 bytes) depending on device version selected.

2. **External Registers**
   Addressable Size: Four selectable banks of up to eight registers each, providing access to up to 32 register addresses. Registers can be selected for read or write operations. Some registers are only accessible in either read mode or write mode.

3. **Processor RAM**
   Size: Two banks of 256 words of 16 bits each, providing a total of 512 words of RAM on 89314, extra 128 words on all other parts in the range on third bank.

Other memory exists in the form of internal registers in the processor and registers that are not part of the processor's direct memory map.



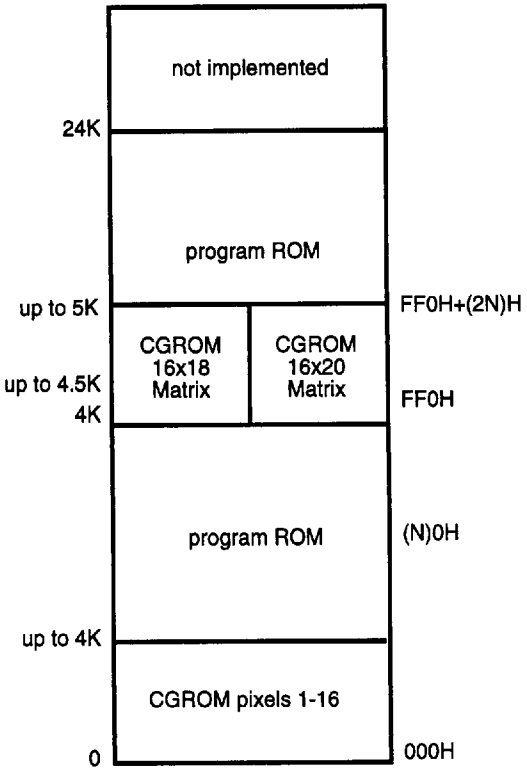


Figure 14. Program Read Only Memory

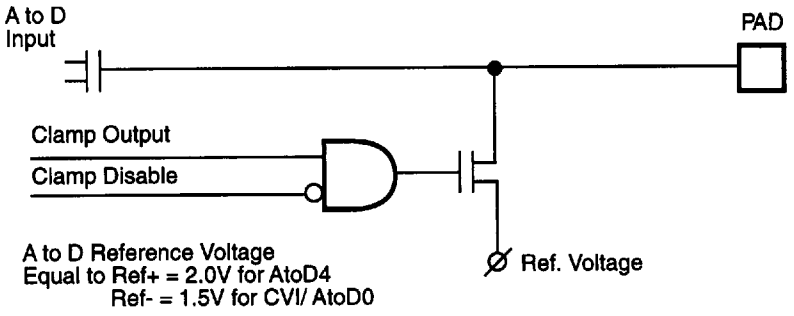


Figure 19. Type5 AtoD Inputs Combined with an Internal Clamp (Composite Video Input/AtoD0 and AtoD4).

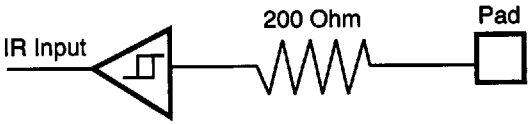


Figure 20. Type6 IR Capture Register Input

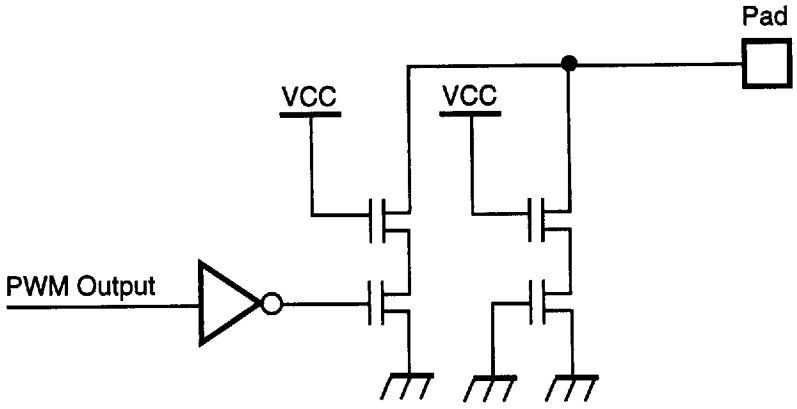


Figure 21. Type7 PWM1, PWM8 Open-Drain Outputs

RECOMMENDATIONS

Reset Circuit

The 32 kHz crystal oscillator of the Z89300 has a typical setting time of 800 ms. The reset will be supplied to the Microprocessor core only if the "reset" pin of the device is held "low" for more than 5 clock cycles. In case of the POR, the external RC circuit should provide a time delay of more than the longest possible setting time of the oscillator.

The typical value of the internal pull-up resistor is 60±20 Kohm.

Assuming that the RC constant of the reset circuit should be >1s, the value of the capacitor can be calculated from:

$$C=\frac{1}{R}=\frac{1}{60x10^{3}}=15x10^{-6}=15.0\ \mu f$$

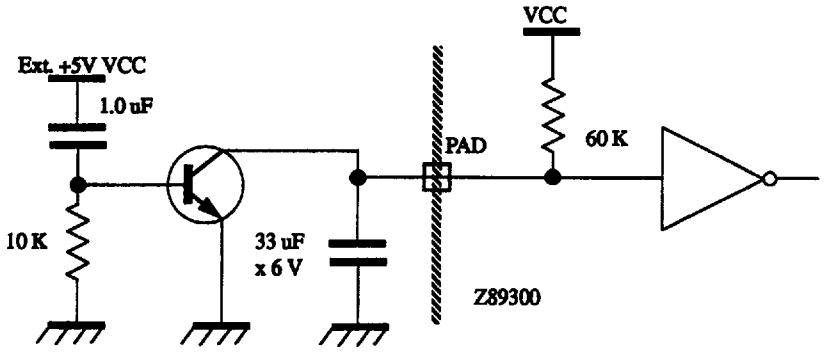


Figure 26. Reset Circuit

HSYNC (HFLYBACK) Recommended Timing (Continued)

CCD data captioning algorithm utilizes sampling of the Composite Video signal during line 21. In order for the CCD algorithm to recognize CCD burst (seven clock cycles of 503 kHz) certain timing relationships between incoming Composite Video signal and HFLYBACK should be maintained.

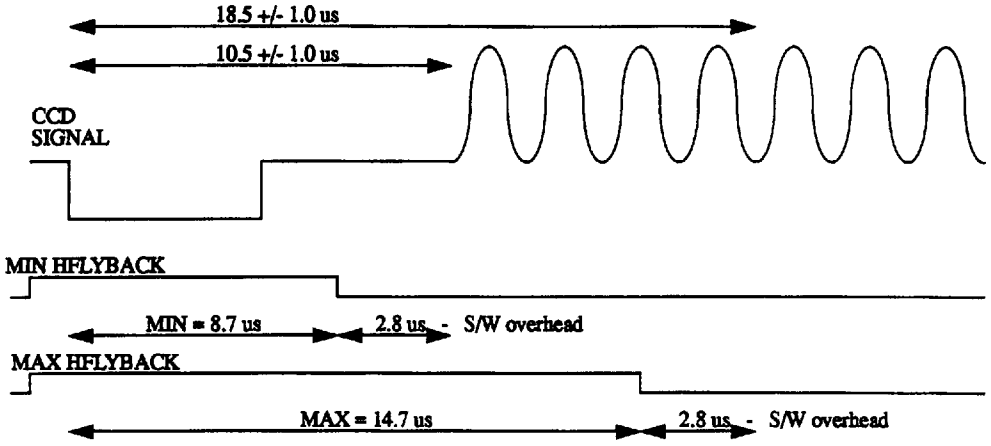


Figure 28. HFLYBACK Timing Diagram

In order to guarantee CCD algorithm performance, the time delay from leading edge of HSYNC to trailing edge of HFLYBACK should be maintained from 8.7 µs to 14.7 µs.

In order to comply with both OSD centering and CCD performance requirements, the time delay of trailing edge of HFLYBACK should be from 8.7 µs to 10.4 µs, which corresponds to HFLYBACK width of 9.7 µs....11.4 µs if leading edge of HFLYBACK is 1.0 µs ahead of leading edge of HSYNC.

Clamp Positioning

The black level of Composite Video signal fed to Z89300 should be set to Ref - voltage of the A to D. In order to shift the DC level of the incoming signal, there is an internal clamp in the Z89300. The clamp pulse should be located during the back porch of the HSYNC.

Clamp position is defined by the "Position" field (bits <6:0>) in Clamp Position register R0(1). The width of clamp pulse cannot be modified and is set to 1 µs. The value which can be assigned to the "Position" field should be >10% and <7%f. The time interval between the leading edge of the H-FLYBACK and the beginning of the clamp pulse can be calculated from:

$$Tdelay = Position \times \frac{1}{Tsclk} = Position \times 82\ ns$$

Because the clamp pulse is generated from the leading edge of the incoming HFLYBACK signal, there are certain constraints imposed on the relative positioning of the leading edge of HFLYBACK relative to leading edge of HSYNC.

By setting the "Position" field of Clamp Position register, the clamp pulse can be positioned at 1.3 µs....10.5 µs after the leading edge of HFLYBACK.

The optimal position of the clamp pulse is 6.5 µs after the leading edge of the HSYNC (in the middle of the back porch interval). Wide setting of "Position" field allows for possible variations in HFLYBACK positioning of up to +4.0 µs....-5.0 µs.

Practical example of registers setting implementation

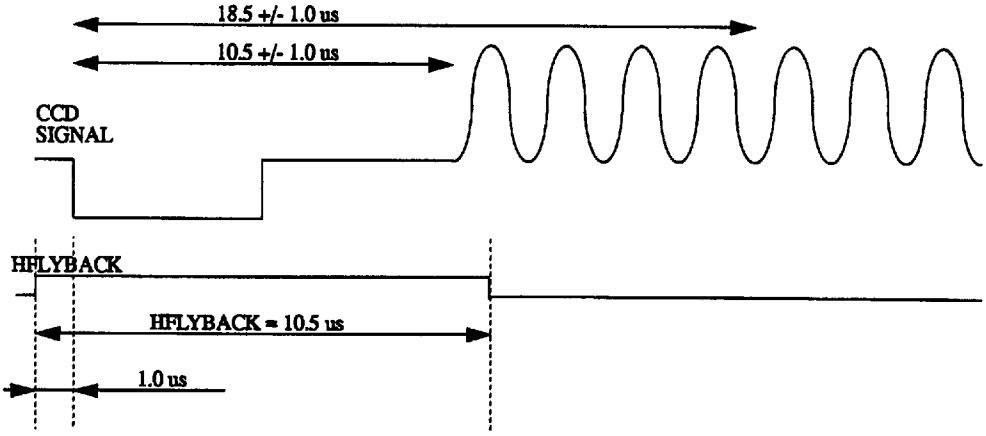


Figure 29. Register Settling Timing Diagram

In this example the time delay from leading edge of HSYNC to trailing edge of HFLYBACK is specified to be 9.5 µs.

In order to position the clamp in the middle of the back porch, the "Position" field of Clamp Position register should be set to 57% (7.2 µs).

The CCD data capture algorithm requirements are satisfied and this particular setting corresponds to the middle of the operating range.

ORDERING INFORMATION

Z89300

24 MHz
42-Pin DIP
Z8930024PSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
P = Plastic DIP

Temperature
S = 0°C to 70°C

Speeds
24 = 24 MHz

Environmental
C = Plastic Standard

Example:

Z 89300 24 P S C is a Z89300, 24 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 24 — Speed
- 89300 — Product Number
- Z — Zilog Prefix