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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	TV Controller
Core Processor	Z8
Program Memory Type	OTP (24kB)
Controller Series	Digital Television Controller (DTC)
RAM Size	640 x 16
Interface	-
Number of I/O	26
Voltage - Supply	4.5V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Through Hole
Package / Case	52-DIP
Supplier Device Package	52-SDIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8930112psg

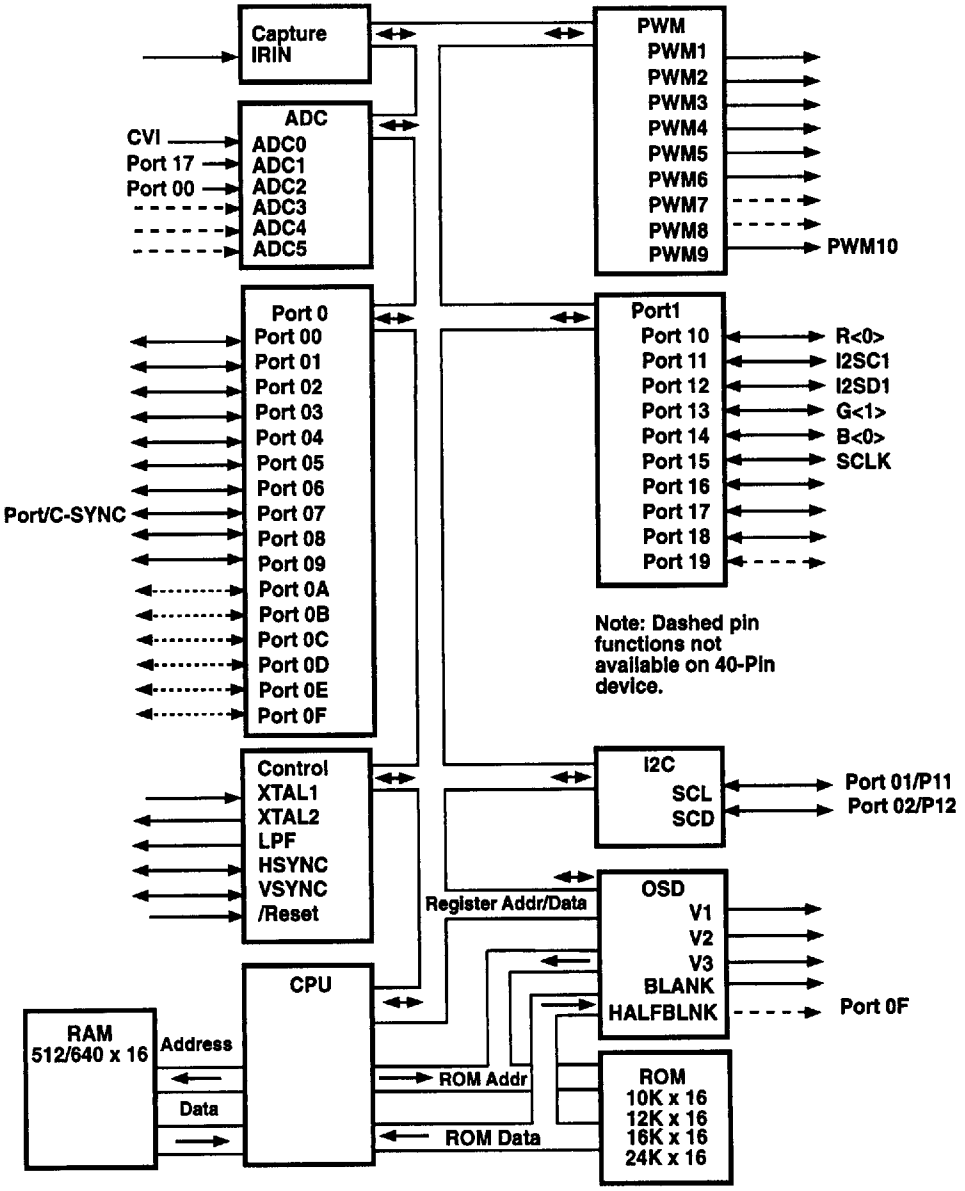

Figure 1. Z89300 Functional Block Diagram

PIN DESCRIPTION

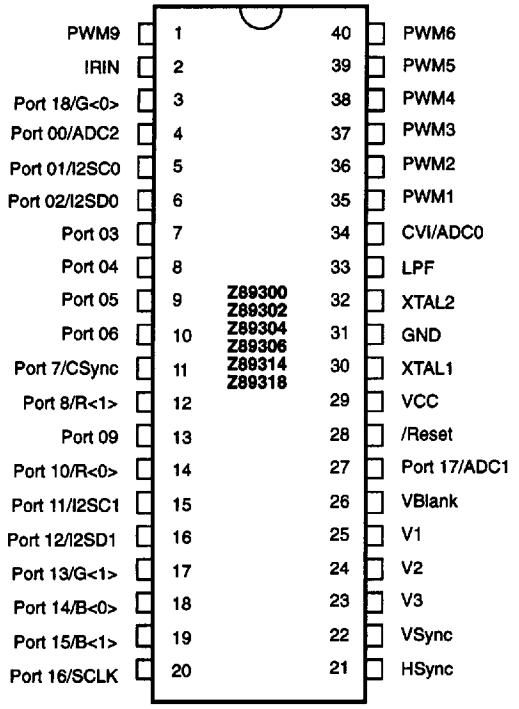

Figure 2. Z89300/02/06 40-Pin DIP

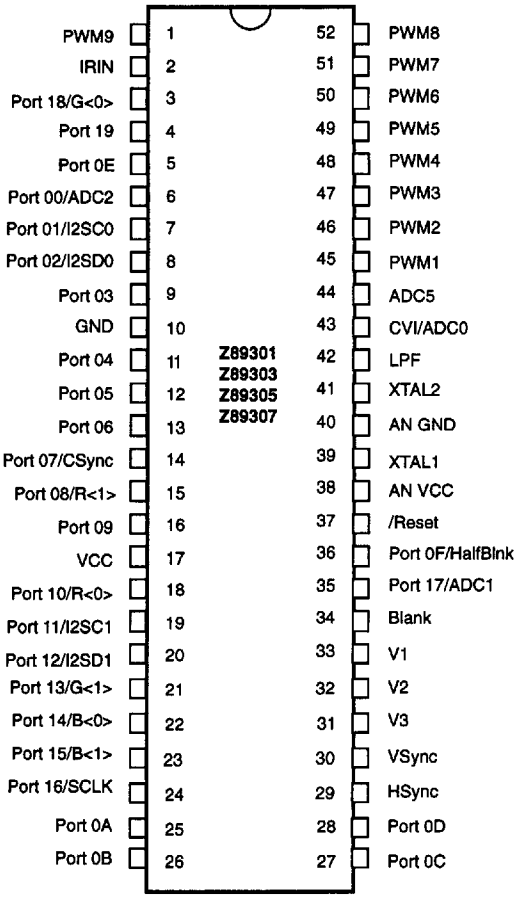

Figure 3. Z89301/03/07 52-Pin DIP

Character Multiplier Multiplexor

The character multiplier multiplexor can be controlled to double or triple the size of the pixel line presented to it from the CGROM capture register. It does not perform a numerical multiplication. The bits of the word contained in the capture register are duplicated to enlarge the character as it would be displayed horizontally on the screen. A model of the operation of the character multiplier multiplexor is shown below:

Capture Register Contents	abcdefghijklmnop	abcdefghijklmnop	abcdefghijklmnop
	char_mult_high	char_mult_mid	char_mult_low
x1 operation			abcdefghijklmnop
x2 operation	aabbccddeeffgghh	iijjkkllmmnnoopp	
x3 operation	aaabbbcccdddeeef	ffgggghhhiiijjjkk	kllmmmnnnooopppp

Tuner Control

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices such as digital channel tuning adjustment may be accessed through the industry standard I^2C port.

Voltage synthesis tuning systems are supported by 14-bit PWM (PWM9/10).

Video and Sound Attribute Control

Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports and one 14-bit pulse width modulated port[1].

Two 14-bit and up to eight 8-bit pulse width modulated are available to provide PWM control of analog signal levels such as volume or color.

Vertical Blank Interval Data Capture

Closed caption text can be decoded directly from the composite video signal with the assistance of the processor's digital signal processing capabilities and displayed on the screen. The character representation in this mode allows for simple attribute control through the insertion of control characters, and each word of RAM specifies two displayed characters.

The 4-bit flash A/D converter provides the ability to directly receive the composite video signal and process the closed caption text embedded in the signal. Signal processing can be applied directly to the signal to improve decoder performance.

I/O Ports

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register.

Up to[2] 26 configurable I/O pins are general-purpose pins that can be utilized to provide functions such as serial data I/O, LED control, key scanning, power control and monitoring and I^2C serial data communications.

Notes:

1. All nine PWM ports are only available in the 52-pin package. In the 40-pin package only six 8-bit and one 14-bit PWM output pins are available
2. The 52-pin device has one 10-bit port and one 16-bit port. The 40-pin device has one 10-bit port and one 9-bit port.
3. The 42-pin device has two 14-bit PWMs and five 8-bit PWMs.

REGISTERS (Continued)

Table 8. Register3 - R3 (0) I2C Interface Register

Reg field	Bit position	R	W	Data	Description
Command	fedc----------	R			Return"0"
			W	%DD	See footnote below the Table
Reset	----b----------	R			Return "0"
			W	1	Reset the I2C interface
				0	No effect
HI/LO_ Speed	-----a----------	R	W	1	High speed (400 kHz) - implemented in Rev. BA
				0	Low Speed (100 kHz)
Slave_ mode	------9---------	R		1	Slave mode
			W	0	Master mode
					No effect
Busy	-------8--------	R		1	I2C interface is busy
			W	0	I2C interface is idle
					No effect
Data	--------76543210	R		xx	Received data
			W	xx	Data to be sent

Master Mode

0000 - Send start bit followed by address byte <Data>
0010 - Send data byte specified in <Data>
0100 - Send <7> as an Ack to Slave after Data byte was received **IN READ FRAME** and receive next Data byte.
0110 - Send <7> as an Ack to Slave, do nothing
1001 - Set Slave address defined in <Data> (BE PREPARED FOR SLAVE MODE)
1100 - Receive Ack from Slave after Address byte was transmitted IN READ FRAME If Ack=0, receive Data, else (Ack=1) do nothing.
1110 - Send stop bit
0011,0101,0111,10xx,1101,1111 - RESERVED COMBINATIONS (SHOULD NOT BE USED).

Slave Mode

0010 - Send <Data> **IN READ FRAME** then latch Master's Ack
0100 - Send <7> = 0 as an Ack **IN WRITE FRAME.**
1110 - Send <7> -1 as an Nak **IN WRITE FRAME** OR Send <7> as an Ack **IN READ FRAME** If <7>=0, "Send <Data>" **IN READ FRAME** command should be executed next, else (<7>!=0) release the bus.
1001 - Set Slave address defined in <Data>
ALL THE RESET COMBINATIONS ARE RESERVED AND SHOULD NOT BE USED.

The received data is available for reading only when the "busy" bit is reset to "0". Upon POR the speed of the I2C interface is set to "low".

REGISTERS (Continued)

Table 12. Register 7 - R7(0) Port 1 Direction Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba----------	R	W		Return "0" No effect
Port_ direction	------9876543210	R	W	xxxx	1 Input mode for corresponding bit 0 Output mode for corresponding bit

Bank 1 (Control Registers)

Table 13. Register0 - R0(1) Clamp Position Register

Reg field	Bit position	R	W	Data	Description
Disable_clamp_1	f---------------	R	W	1 0	ADC0 Clamp generation is disabled ADC0 Clamp generation is enabled
Disable_clamp_2	-e---------------	R	W	1 0	ADC5 Clamp generation is disabled ADC5 Clamp generation is enabled Implemented in Rev. BA
Reserved	--dcba987-------	R	W		Return "0" No effect
Position	---------6543210	R	W	xx	Position of clamp pulse (from leading edge of the H-FLYBACK)

Upon POR both disable_clamp bits are set to a "1".

The clamp pulse will be generated if it is Enabled bit (bit <f>) and the SCLK frequency was switched "back" to PVCO (SVCO/PVCO flag in R6 (1) should be reset to "0") before the current h-sync regardless whether the SVCO is enabled or disabled. Clamp position is defined by the "Position" field. The width of clamp pulse cannot be modified and is set to 1 µs. The value which can be assigned to the "Position" field should be >%10 and <%ff. The time interval between the leading edge of the H-FLY-BACK and the beginning of the clamp pulse can be calculated from:

$$Tdelay = Position \times \frac{1}{Tsclk} = Position \times 82\ ns$$

Table 14. Register 1 - R1(1) Speed Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba98765432--	R	W		Return"0" No effect
Fast_enable	--------------1-	R	W	1 0	PVCO,SVCO enabled PVCO,SVCO disabled
Fast/Slow	---------------0	R	W	1 0	SCLK is 12 MHz SCLK is 32 kHz

Upon POR, SMR and WDT reset both of these bits are reset to "0", which corresponds to SCLK frequency of 32 kHz.

In order to switch from 32 kHz SCLK to 12 MHz, the following procedure is recommended:

- Setting Fast _enable bit to a "1":
- Waiting for 300 .. 400 ms for 12 MHz PLL to be stabilized (approximately 15000 clock cycles)
- Setting Fast/Slow bit to a "1":

In order to switch from 12 MHz SCLK to 32 kHz, the following procedure is recommended:

- Setting Fast/Slow bit to a "0":
- Waiting for 32 µs for SCLK to be switched (approximately 360 clock cycles);
- Setting Fast_enable bit to a "0".

Table 15. Register2 - R2(1) WDT/STOP Mode Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba98765432--	R	W		Return"0" No effect
WDT_instr	--------------1-	R	W	1 0	Return "0" WDT enable, WDT reset No effect
STOP_instr	---------------0	R	W	1 0	Return "0" STOP instruction No effect

Upon POR, SMR and WDT reset the WDT is disabled. The WDT can be re-enabled only after the PVCO and SVCO are enabled and the part is switched into a Fast mode (SCLK = 12 MHz). Upon switching the part into a Slow mode (SCLK = 32 MHz) the WDT will be suspended and the WDT counter will resume count when the Fast operation will be restored. In the latter case an additional re-initialization of the WDT is not necessary.

Table 19. Register6 - R6(1) Clock Switch Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba9876------	R	W		Return "0" No effect
SVCO/PVCO	----------5-----	R	W	1 0 1 0	SCLK=SVCO (flag) SCLK=PVCO (flag) Switch SCLK to PVCO No effect
No_switch	----------4----	R	W	1 0	SCLK=PVCO, NO clock switching Clock switching is enabled
H_position	----------3210	R	W	%D	Defines delay of Hint by 4D SCLK cycles

The clock switch control register defines the source of SCLK fed into the Z89C00 core. The block diagram of the clock switch circuit is presented on figure below.

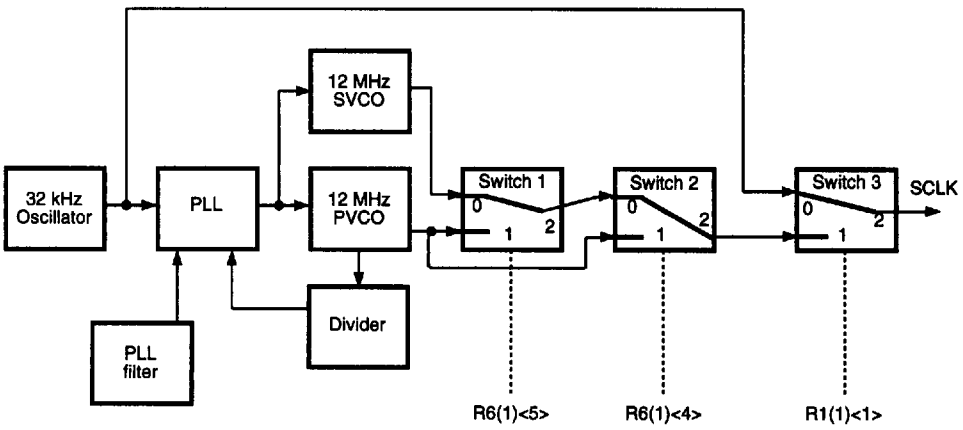

Figure 10. Clock Switch Control Register

Switch1 positioning defines the source of the signal on terminal 0 of switch2. Switch2 is used to override the frequency setting in "no_switch" mode. Whenever "no_switch" mode is set, switch1 continues to switch between PVCO and SVCO. Because of that it is not recommended to switch2 if it is not guaranteed that PVCO signal is fed to terminal0 of switch2. The recommended sequence is as follows:

1. Switch SCLK to PVCO
2. Wait for 2..3 SCLK cycles to ensure that the SCLK is switched
3. Switch R6 (1) <4> to enable/disable "no_switch" mode.

Bank 2 (PWM Registers)

Table 22. Register0. Register7 - R0(2)..R7(2) PWM1..8 Registers

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba98--------	R W			Return "0" No effect
PWM_data	--------76543210	R	W	xx	8-bit PWM data

All of the PWMs have open-drain outputs. The outputs of all PWMs are staged by one PVCO clock. The repetition frequency of PWM output signals can be calculated from:

$$Fpwm = \frac{Fpvco}{8(256)} = \frac{12\ MHz}{2048} = 6\ kHz$$

Bank 3 (On-Screen Display [OSD] Registers)

Table 23. Register 0. Register2 - R0(3).R2(3) Character Multiplier Registers (Read Only)

Reg field	CGROM data	Reg addr.	Description
cgrom_x2_hi cgrom_x3_hi	ffeeddccbbaa9988 ffeeddccbbaa9988	R0(3)	High word of double size character R4(3)<6>=0 High word of triple size character R4(3)<6>=1
cgrom_x2_lo cgrom_x3_mid	7766554433221100 aa99988877766655	R1(3)	Low word of double size character R4(3)<6>=0 Middle word of triple size character R4(3)<6>=1
cgrom_x1 cgrom_x3_lo	fedcba9876543210	R2(3)	Single size character R4(3)<6>=0 Low word of triple size character R4(3)<6>=1

Table 24. Register0..Register1-R0(3)..R1(3) Shift Registers (Write Only)

Reg field	CGROM data	Reg addr.	Description
current_reg	fedcba9876543210	R0(3)	current line shift register
next/previous_reg	fedcba9876543210	R1(3)	next/previous line shift register

These register should be loaded with video data once every 16 cycles. The current line register should be loaded first, followed by next/previous register during the next cycle. The next/previous register should be loaded only if smoothing/fringing attributes are activated for the current character. If both of those registers are not loaded, the space character will be displayed. There is no difference between loading "000" h into either of the registers or not loading them at all.

REGISTERS (Continued)

Table 28. Register4 - R4(3) OSD Control Register

Reg field	Bit position	R	W	Data	Description
Underline	fe----------	R	W	1x 0x x1 x0	Second underline is active Second underline is inactive First underline is active First underline is inactive
OSD/CCD	--d----------	R	W	1 0	OSD mode CCD mode
CCD_ top/btm	---c----------	R	W	1 0	Blinking character is displayed Blinking character is NOT displayed (hidden)
Italic_shift	-----ba98-------	R	W	x	Defines delay of the character
Blink on/off	---------7------	R	W	1 0	Blinking character is not displayed Blinking character is displayed (hidden)
MPX_bus	---------65-----	R	W	0 0 0 1 1 0 1 1	x1 character size x2 character size x3 character size Reserved
CGROM scan_line	----------43210	R	W	%D	Defines CGROM addressing IN REV.BA also defines italic shift

The Underline field should be set by the firmware during the line/lines of the OSD when the second/first underline is active. The bits will be ANDed with the 2nd/1st underline active fields of data loaded into an attribute register R2(3) allowing character on screen to be underlined.

Italic shift field defines the delay of current video data. Typically it is used to generate italic characters. The firmware decrements by "1" the value of the Italic_shift field for each consecutive line. The video signal will be delayed only for those characters, which have R2(3)<4>("italic") bit set to a "1"

Table 29. Register5 - R5(3) Capture Register

Reg field	Bit position	R	W	Data	Description
Capture_data	fedcba9876543210	R	W	%xxxx	16-bit captured data No effect

REGISTERS (Continued)

Table 31. Register7 - R7(3) Output Palette Control Register

Reg field	Bit position	R	W	Data	Description
Reserved HBLANK_Delay	fedc----------	R W			Return "0" Delay Value No effect %00 - POR Condition
Background_on/off	----b----------	R	W	1 0	Background is on Background is off - POR condition
Background_color	-----a98--------	R	W	%D	Defines the color of the background (the same as the Palette)
Reserved	--------7-------	R W			Return "0" No effect
StarSight palette	---------6------	R	W	0 1 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	Palette is defined by bits <5..0> StarSight palette: Black V1=0; V2=0; V3=0; Blue V1=0; V2=99% V3=99%; Green V1=66%, V2=99%; V3=99%; Grey V1=66%; V2=66%; V3=66%; Red V1=99%; V2=33%; V3=33%; LtYell V1=99%; V2=99%; V3=0; Yellow V1=99%; V2=99%, V3=0; White V1=99%; V2=99%; V3=99%;
Palette_ red (V1)	----------54----	R	W	0 0 0 1 1 0 1 1	66% red 66% red + 33% blue 66% red + 33% green 66% red + 33% blue + 33% green
Palette_ green (V2)	------------32--	R	W	0 0 0 1 1 0 1 1	66% green 66% green + 33% blue 66% green + 33% red 66% green + 33% blue + 33% red
Palette_ blue (V3)	--------------10	R	W	0 0 0 1 1 0 1 1	66% blue 66% blue + 33% green 66%blue + 33% red 66% blue + 33% green + 33% red
Digital_ mode	----------543210	R	W	000000	Outputs V1, V2, V3 correspond to 100% red, green, and blue outputs

Upon POR the Output palette register is set to "0" - digital output.

Note: If bit R7(3)<6> is set to "1", while bits R7(3)<5:0> are reset to a "0". the outputs V1, V2 and V3 of Z89300 will be switched into a "Digital mode".

REGISTER SUMMARY

Table 32. Register Utilization Rev 2.0

BANK	BANK Sub Address	READ Register	WRITE Register	Description
Bank 0	7	dir1		10-bit I/O port 1 direction control
	6	dir0		16-bit I/O port 0 direction control
	5	port1		10-bit I/O port 1
	4	port0		16-bit I/O port 0
	3	i2c_int		I2C interface register
	2	pll_freq		PLL frequency control
	1	pwm_data10		14-bit PWM10 data
	0	pwm_data9		14-bit PWM9 data
Bank 1	7	wdt_smr_ctl		Stop-Mode Recovery/Watch-Dog Timer Control
	6	clock_ctl		Clock control (switch VCO/DOT)
	5	cap_1s_ctl		Counter timers control
	4	atod_ctl		A/D converter control
	3	standard_ctl		Output H/V-sync/blnk control
	2	stop_wdt_ctl		Stop and Watch-Dog Timer Control
	1	sclk_freq		Stop/Sleep/Normal Mode
	0	clamp_pos		Defines position of video clamp pulse
Bank 2	7	pwm_data8		8-Bit PWM 8 data
	6	pwm_data7		8-Bit PWM 7 data
	5	pwm_data6		8-Bit PWM 6 data
	4	pwm_data5		8-Bit PWM 5 data
	3	pwm_data4		8-Bit PWM 4 data
	2	pwm_data3		8-Bit PWM 3 data
	1	pwm_data2		8-Bit PWM 2 data
	0	pwm_data1		8-Bit PWM 1 data
Bank 3	7	output palette		Output palette
	6	palette_color		Display palette color/underline color
	5	capture_data	(no effect)	Capture register data
	4	osd_control		On-Screen Display Control
	3	attribute_data	vram_data	Character attribute/video ram data
	2	ch_x1_lo_x3	cg_attribute	Character mult./char. graphics attribute
	1	lo_x2_mid_x3	cg_nxt_prv	Character mult./next or previous data
	0	hi_x2_hi_x3	cg_current	Character mult./current data

Video RAM Specification (Supported data format in VRAM)

The H/W of the Z893xx supports two different data formats in the VRAM. The first one supports a standard OSD with full set of features (OSD mode). The second format supports reduced features which comply with the recommendations of the FCC on Closed Caption support (CCD mode). In CCD mode the background color of the characters can not be changed and is always preset to a "black".

In OSD mode each character occupies 16-bit word in VRAM. There are two possible character formates defined: a "display" character and a "control" character. The code stored in a "display" character format defines a character code and up to 7 attributes of the character. The "control" character defines up to eight attributes of the next character and is presented on screen as a space character. Combination of "display" and "control" characters allows to generate a versatile OSD.

Table 33. Display Character Format (OSD Mode)

Reg field	Bit position	Data	Description
Control bit	f---------------	1 0	Control character Display character
Background color	-edc------------	000 001 010 011 100 101 110 111	Black Blue Green Light Blue Red Magenta Yellow White
Foreground color (Not palette mode)	----ba9---------	%D	Same as Background_color
Foreground palette (Palette mode)		00x 01x 10x 11x	Palette 0 (defined in R6(3)<8..6> Palette 1 (defined in R6(3)<b..9> Palette 2 (defined in R6(3)<5..3> Palette 3 (defined in R6(3)<2..0>
Second underline (Palette mode)		xx1 xx0	Second underline attribute is active Second underline attribute is inactive
First underline	-------8--------	1 0	First underline attribute is active First underline attribute is inactive
Character code	--------76543210	%DD	Defines the character in CGROM

If background and foreground colors of a character are set to be the same, the character will be displayed as a transparent one.

A to D and Clamp Circuit Operation (Recommended Practice) (Continued)

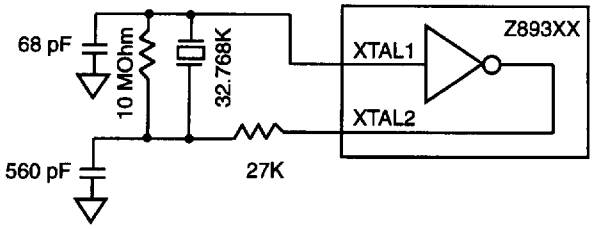

Figure 12. 32K Oscillator Recommended Circuit

V1, V2, V3 Analog Output

Table 38. V_{cc} = 5.25V

VCC=5.25V	Condition	Limit
Output Voltage	bit=11	4.55V ± 0.25V
	bit=10	3.25V ± 0.2V
	bit=01	1.95V ± 0.15V
	bit=00	0.65V ± 0.1V
Settling Time	70% of DC level, 10 pf load	<50 nsec

Table 39. V_{cc} = 4.75V

VCC=5.25V	Condition	Limit
Output Voltage	bit=11	3.90V ± 0.25V
	bit=10	2.90V ± 0.2V
	bit=01	1.90V ± 0.15V
	bit=00	0.1V ± 0.1V
Settling Time	70% of DC level, 10 pf load	<50 nsec

MODULE DESCRIPTIONS (Continued)

The size of memory used as CGROM depends on the number and resolution of characters stored in memory. 'N' represents the number of characters stored, ranging from 0 to 256. If characters are 16 x 18 or 16 x 20 pixels then the upper region of memory starting at the 4K boundary is used for character storage. If not it can be used as program memory.

Clocking Operation

The processor is able to operate from a number of clock sources.

1. Primary Phase Locked Loop V_{co} source (PVCO)
2. Secondary V_{co} phase-aligned with VSYNC timing (SVCO)
3. 32 kHz oscillator clock (OSC)

In addition the processor clock may be halted temporarily to allow clock selection or ROM accesses to be performed without disrupting normal operation of the processor.

PADS CONFIGURATION

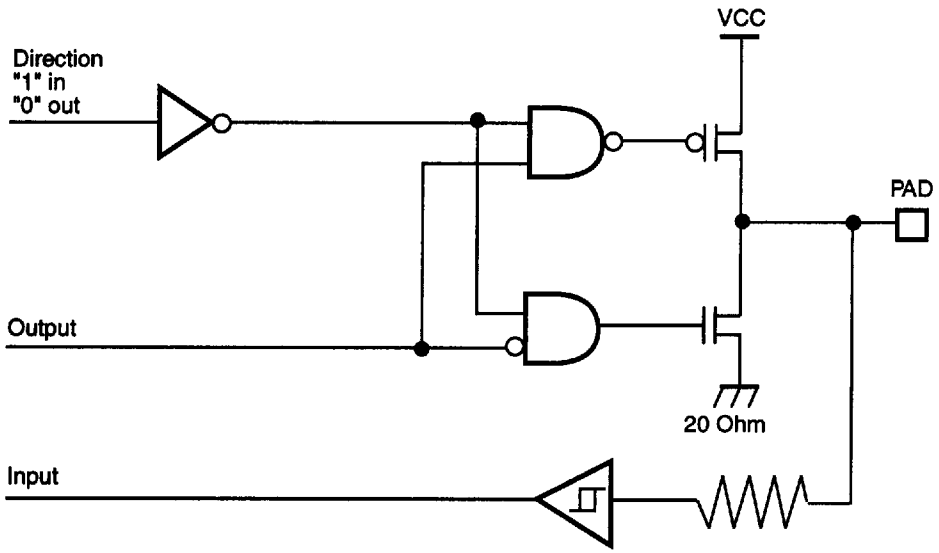

Figure 15. Type1 Bi-directional Port pins (Port 3, Port0f, Port 10, Port 13, Port 16, Port 18, Port 19, H-SYNC and V-SYNC)

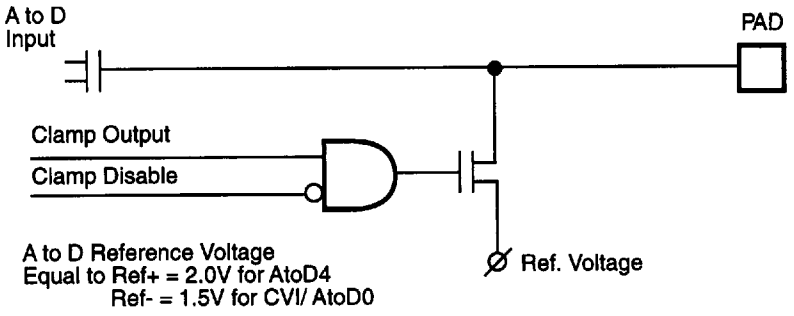

Figure 19. Type5 AtoD Inputs Combined with an Internal Clamp (Composite Video Input/AtoD0 and AtoD4).

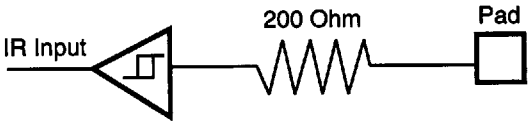

Figure 20. Type6 IR Capture Register Input

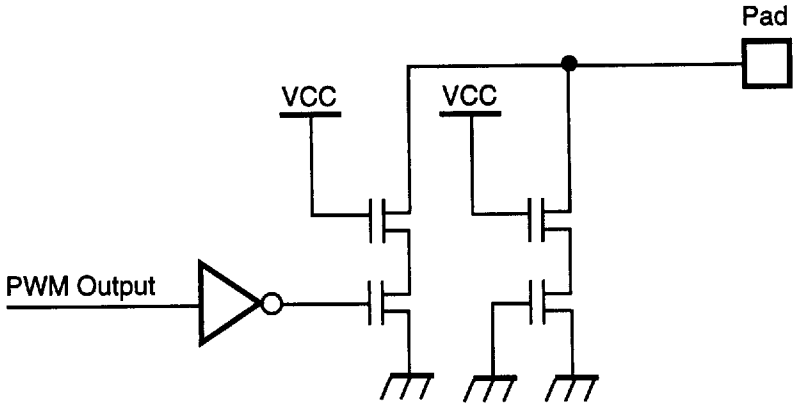

Figure 21. Type7 PWM1, PWM8 Open-Drain Outputs

PADS CONFIGURATION (Continued)

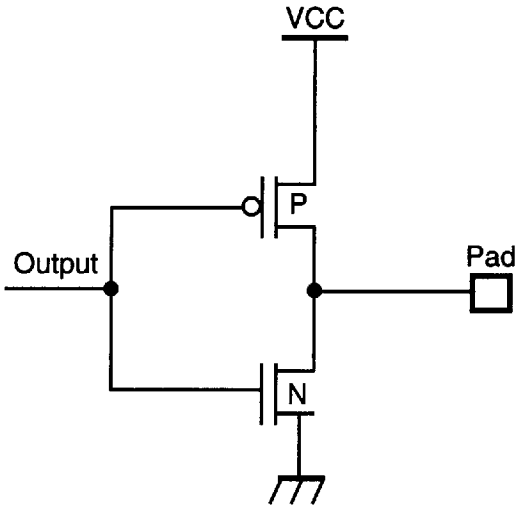

Figure 22. Type8 PWM9 and BLANK outputs; V1, V2, V3 outputs in digital mode

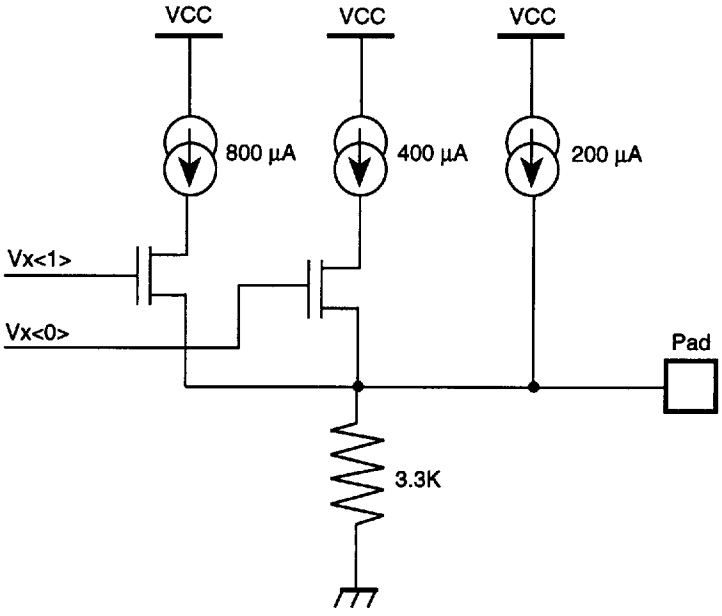

Figure 23. V1, V2 and V3 outputs in analog (palette) mode.

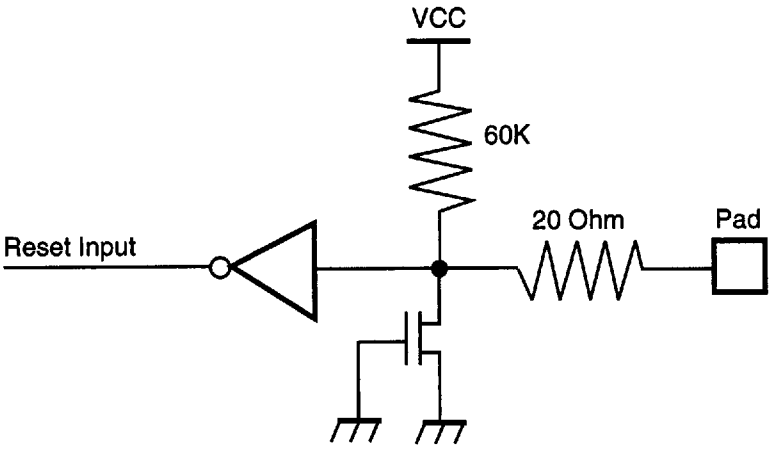

Figure 24. Reset Input

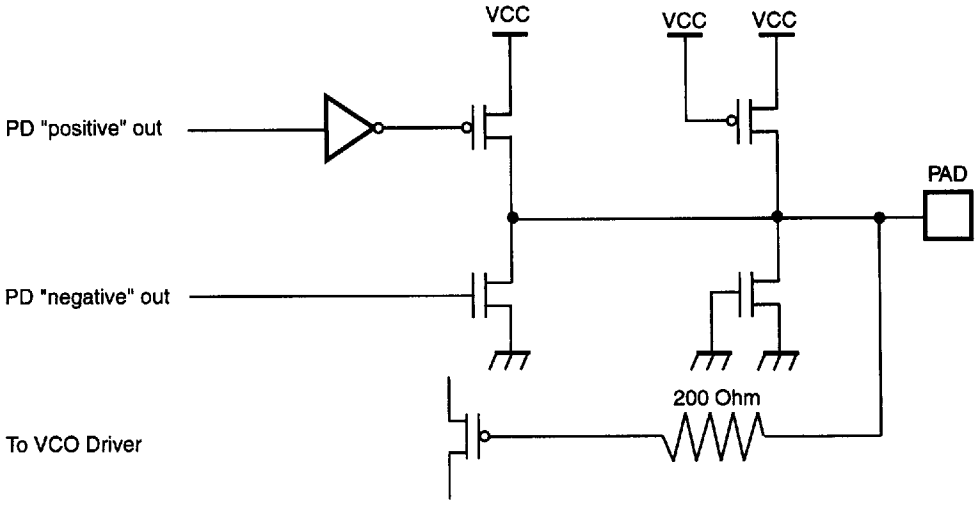

Figure 25. Loop Filter Pin

AC CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC}=4.5V to 5.5V; F_{OSC} = 32.768 kHz)

Sym	Parameter	Min	Typ	Max	Units
T_pC	Input clock period	16	32	100	µs
T_RC, T_fC	Clock input Rise and Fall		12		µs
T_DPOR	Power-on reset delay	0.8	1.2		S
T_wRES	Power-on reset minimum			5 TpC	µs
T_DH_S	H-SYNC incoming signal width	5.5	11	12.5	µs
T_DV_S	V-SYNC incoming signal width	0.15	1.0	1.5	ms
T_DE_S	Time delay between leading edge of V-SYNC and H-SYNC in EVEN filed	-12	0	+12	µs
T_DO_S	Time delay between leading edge of V-SYNC and H-SYNC in ODD field	20	32	44	µs
T_wHV_S	H-SYNC/V-SYNC edge width		0.5	2.0	µs

Note:
All timing of the I²C bus interface are defined by related specifications of the I²C bus interface

HSYNC (HFLYBACK) Recommended Timing (Continued)

CCD data captioning algorithm utilizes sampling of the Composite Video signal during line 21. In order for the CCD algorithm to recognize CCD burst (seven clock cycles of 503 kHz) certain timing relationships between incoming Composite Video signal and HFLYBACK should be maintained.

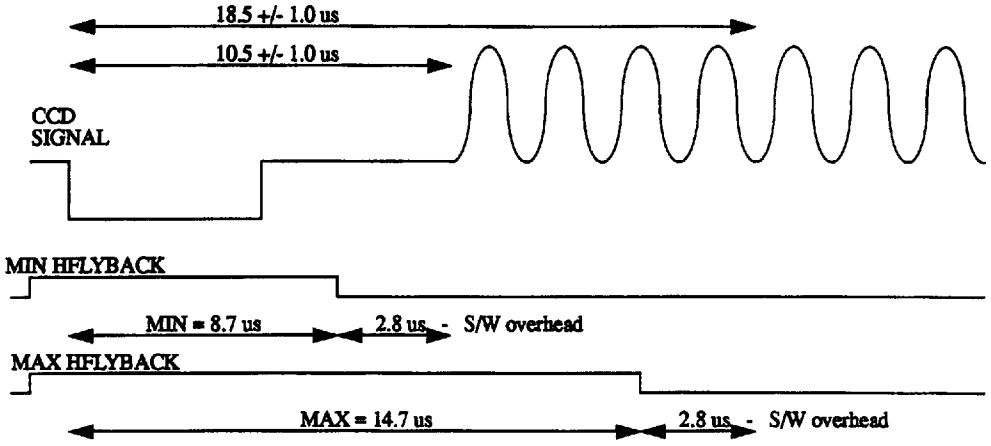

Figure 28. HFLYBACK Timing Diagram

In order to guarantee CCD algorithm performance, the time delay from leading edge of HSYNC to trailing edge of HFLYBACK should be maintained from 8.7 µs to 14.7 µs.

In order to comply with both OSD centering and CCD performance requirements, the time delay of trailing edge of HFLYBACK should be from 8.7 µs to 10.4 µs, which corresponds to HFLYBACK width of 9.7 µs....11.4 µs if leading edge of HFLYBACK is 1.0 µs ahead of leading edge of HSYNC.

Clamp Positioning

The black level of Composite Video signal fed to Z89300 should be set to Ref - voltage of the A to D. In order to shift the DC level of the incoming signal, there is an internal clamp in the Z89300. The clamp pulse should be located during the back porch of the HSYNC.

Clamp position is defined by the "Position" field (bits <6:0>) in Clamp Position register R0(1). The width of clamp pulse cannot be modified and is set to 1 µs. The value which can be assigned to the "Position" field should be >10% and <7%f. The time interval between the leading edge of the H-FLYBACK and the beginning of the clamp pulse can be calculated from:

$$Tdelay = Position \times \frac{1}{Tsclk} = Position \times 82\ ns$$

Because the clamp pulse is generated from the leading edge of the incoming HFLYBACK signal, there are certain constraints imposed on the relative positioning of the leading edge of HFLYBACK relative to leading edge of HSYNC.

By setting the "Position" field of Clamp Position register, the clamp pulse can be positioned at 1.3 µs....10.5 µs after the leading edge of HFLYBACK.

The optimal position of the clamp pulse is 6.5 µs after the leading edge of the HSYNC (in the middle of the back porch interval). Wide setting of "Position" field allows for possible variations in HFLYBACK positioning of up to +4.0 µs....-5.0 µs.

Practical example of registers setting implementation

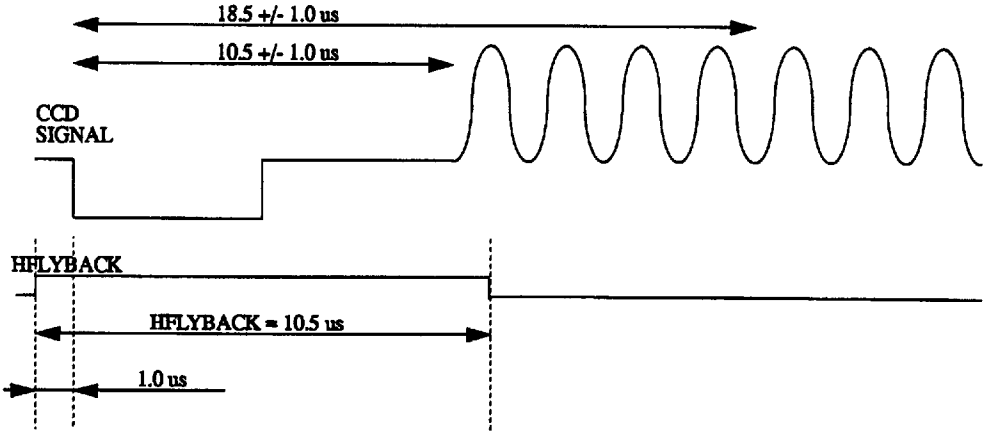

Figure 29. Register Settling Timing Diagram

In this example the time delay from leading edge of HSYNC to trailing edge of HFLYBACK is specified to be 9.5 µs.

In order to position the clamp in the middle of the back porch, the "Position" field of Clamp Position register should be set to 57% (7.2 µs).

The CCD data capture algorithm requirements are satisfied and this particular setting corresponds to the middle of the operating range.