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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560b40l3b6e0y

Contents

1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

1.2 Description

The SPC560B40x/50x and SPC560C40x/50x is a family of next generation microcontrollers built on the Power Architecture embedded category.

The SPC560B40x/50x and SPC560C40x/50x family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 6. Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT — WKPU[19][4]	SIUL eMIOS_0 CGL — WKPU	I/O I/O O — I	M	Tristate	5	12	16	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — —	GPIO[1] E0UC[1] — — NMI[5] WKPU[2][4]	SIUL eMIOS_0 — — WKPU WKPU	I/O I/O — — I I	S	Tristate	4	7	11	F3
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — — WKPU[3][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	3	5	9	F2
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 —	GPIO[3] E0UC[3] — — EIRQ[0]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	43	68	90	K15
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — — WKPU[9][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	20	29	43	N6
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	51	79	118	C11
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — — EIRQ[1]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	52	80	119	D11

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2]	SIUL eMIOS_0 LINFlex_3 — SIUL	I/O I/O O — I	S	Tristate	44	71	104	D16
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[6] —	GPIO[8] E0UC[8] — — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 — — SIUL BAM LINFlex_3	I/O I/O — — I I I	S	Input, weak pull-up	45	72	105	C16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[6]	GPIO[9] E0UC[9] — — FAB	SIUL eMIOS_0 — — BAM	I/O I/O — — I	S	Pull-down	46	73	106	C15
PA[10]	PCR[10]	AF0 AF1 AF2 AF3	GPIO[10] E0UC[10] SDA —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	S	Tristate	47	74	107	B16
PA[11]	PCR[11]	AF0 AF1 AF2 AF3	GPIO[11] E0UC[11] SCL —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	S	Tristate	48	75	108	B15
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 —	GPIO[12] — — — SIN_0	SIUL — — — DSPI0	I/O — — — I	S	Tristate	22	31	45	T7
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 — —	SIUL DSPI_0 — —	I/O O — —	M	Tristate	21	30	44	R7

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX — —	SIUL LINFlex_2 — —	I/O O — —	S	Tristate	63	99	143	A1
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — — — LIN2RX WKPU[13][4]	SIUL — — — LINFlex_2 WKPU	I/O — — — I I	S	Tristate	2	2	2	B1
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX[11] MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC	I/O O O O	M	Tristate	13	22	28	M3
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — — CAN1RX CAN4RX[11] WKPU[5][4]	SIUL — — — FlexCAN_1 FlexCAN_4 WKPU	I/O — — — I I I	S	Tristate	—	21	27	M4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — SIN_2	SIUL eMIOS_0 — — DSPI_2	I/O I/O — — I	M	Tristate	—	97	141	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	—	98	142	A2
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	—	3	3	C1

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ANS[5]	SIUL DSPI_1 eMIOS_0 — ADC	I/O I/O I/O — I	J	Tristate	—	62	84	M14
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — ANS[6]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	64	86	L15
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — ANS[7]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	66	88	L14
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] — — CAN5RX[11] WKPU[6][4]	SIUL eMIOS_0 — — FlexCAN_5 WKPU	I/O I/O — — I I	S	Tristate	—	6	10	F1
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] CAN5TX[11] —	SIUL eMIOS_0 FlexCAN_5 —	I/O I/O O —	M	Tristate	—	8	12	F4
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 —	GPIO[66] E0UC[18] — — SIN_1	SIUL eMIOS_0 — — DSPI_1	I/O I/O — — I	M	Tristate	—	89	128	D7
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS_0 DSPI_1 —	I/O I/O O —	M	Tristate	—	90	129	C7

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

Caution: All LQFP64 information is indicative and must be confirmed during silicon validation.

3.10 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.11 NVUSRO register

Bit values in the Non-Volatile User Options (NVUSRO) Register control portions of the device configuration, namely electrical parameters such as high voltage supply and oscillator margin, as well as digital functionality (watchdog enable/disable after reset).

For a detailed description of the NVUSRO register, please refer to the device reference manual.

3.11.1 NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. *Table 9* shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 9. PAD3V5V field description

Value(1)	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

3.11.2 NVUSRO[OSCILLATOR_MARGIN] field description

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value. *Table 10* shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 10. OSCILLATOR_MARGIN field description

Value(1)	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

1. Default manufacturing value is '1'. Value can be programmed by customer in Shadow Flash.

3.11.3 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. *Table 11* shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 11. WATCHDOG_EN field description

Value(1)	Description
0	Disable after reset
1	Enable after reset

1. Default manufacturing value is '1'. Value can be programmed by customer in Shadow Flash.

3.12 Absolute maximum ratings

Table 12. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	–0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_BV}	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	–0.3	V_{DD}+0.3	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_ADC}	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} –0.3	V_{DD}+0.3	

Table 21. Output pin transition times (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
t_{tr}	CC	D	Output transition time output pin[2] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).

3.15.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 22*.

Table 22. I/O supply segment

Package	Supply segment					
	1	2	3	4	5	6
LBGA208[1]	Equivalent to LQFP144 segment pad distribution				MCKO	MDOn/MSEO
LQFP144	pin20–pin49	pin51–pin99	pin100–pin122	pin 123–pin19	—	—
LQFP100	pin16–pin35	pin37–pin69	pin70–pin83	pin 84–pin15	—	—
LQFP64[2]	pin8–pin26	pin28–pin55	pin56–pin7	—	—	—

1. LBGA208 available only as development package for Nexus2+
2. All LQFP64 information is indicative and must be confirmed during silicon validation.

Table 23 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 26. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	W
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100 [3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
$\left\|\frac{d}{dt}VDD\right\|$	SR	—	Maximum slope on V_{DD}		—	—	250	mV/µs
$\|\Delta_{VDD(STDBY)}\|$	SR	—	Maximum instant variation on V_{DD} during standby exit		—	—	30	mV
$\left\|\frac{d}{dt}VDD(STDBY)\right\|$	SR	—	Maximum slope on V_{DD} during standby exit		—	—	15	mV/µs
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.16	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{p2} substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{p2} equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_c \times (C_S+C_{p2}))$, where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{p2}) and the sum of $R_S + R_F$, the external circuit must be designed to respect the *Equation 4*:

Equation 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on a resistive path.

Table 45. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
| INL |	CC	T	Absolute value for integral non-linearity	No overload		—	0.5	1.5	LSB
| DNL |	CC	T	Absolute differential non-linearity	No overload		—	0.5	1.0	LSB
| E_O |	CC	T	Absolute offset error	—		—	0.5	—	LSB
| E_G |	CC	T	Absolute gain error	—		—	0.6	—	LSB
TUEp	CC	P	Total unadjusted error[7] for precise channels, input only pins	Without current injection		–2	0.6	2	LSB
		T		With current injection		–3		3	
TUEx	CC	T	Total unadjusted error[7] for extended channel	Without current injection		–3	1	3	LSB
		T		With current injection		–4		4	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. Analog and digital V_{SS} **must** be common (to be tied together externally).
3. V_{AINx} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
4. Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.
5. During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_s. After the end of the sampling time t_s, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_s depend on programming.
6. This parameter does not include the sampling time t_s, but only the time for determining the digital result and the time to load the result's register with the conversion result.
7. Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

3.27 On-chip peripherals

3.27.1 Current consumption

Figure 28. DSPI modified transfer format timing – master, CPHA = 1

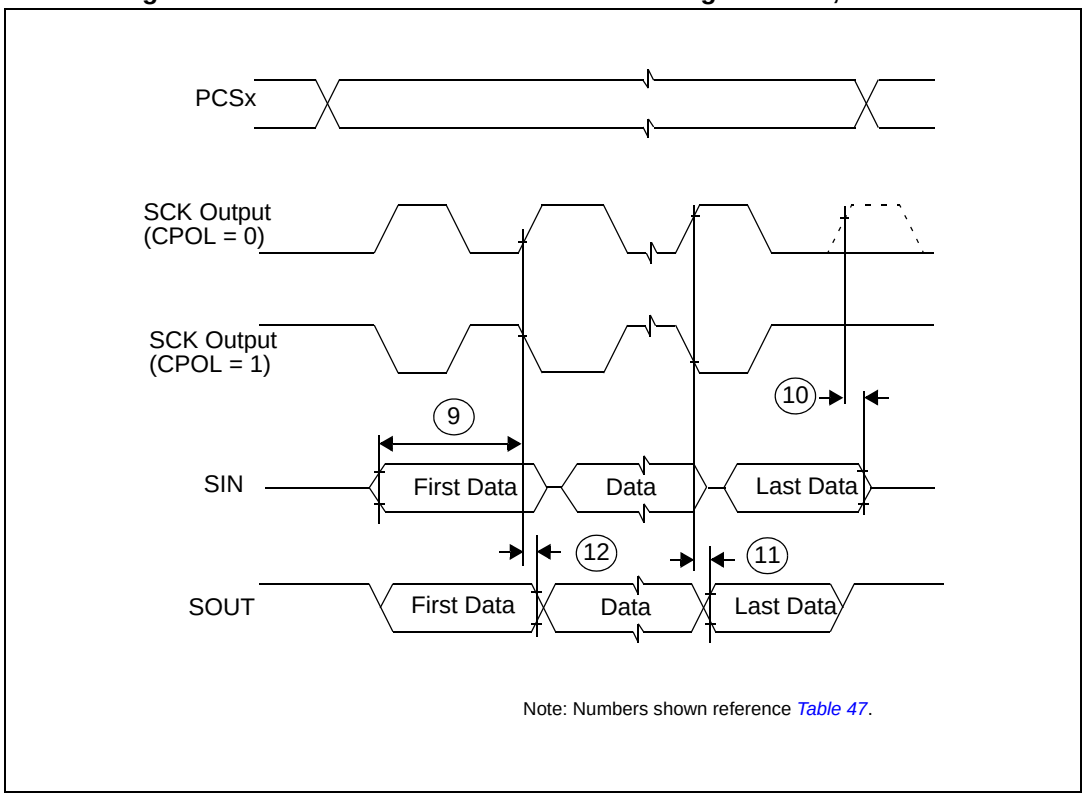


Figure 29. DSPI modified transfer format timing – slave, CPHA = 0

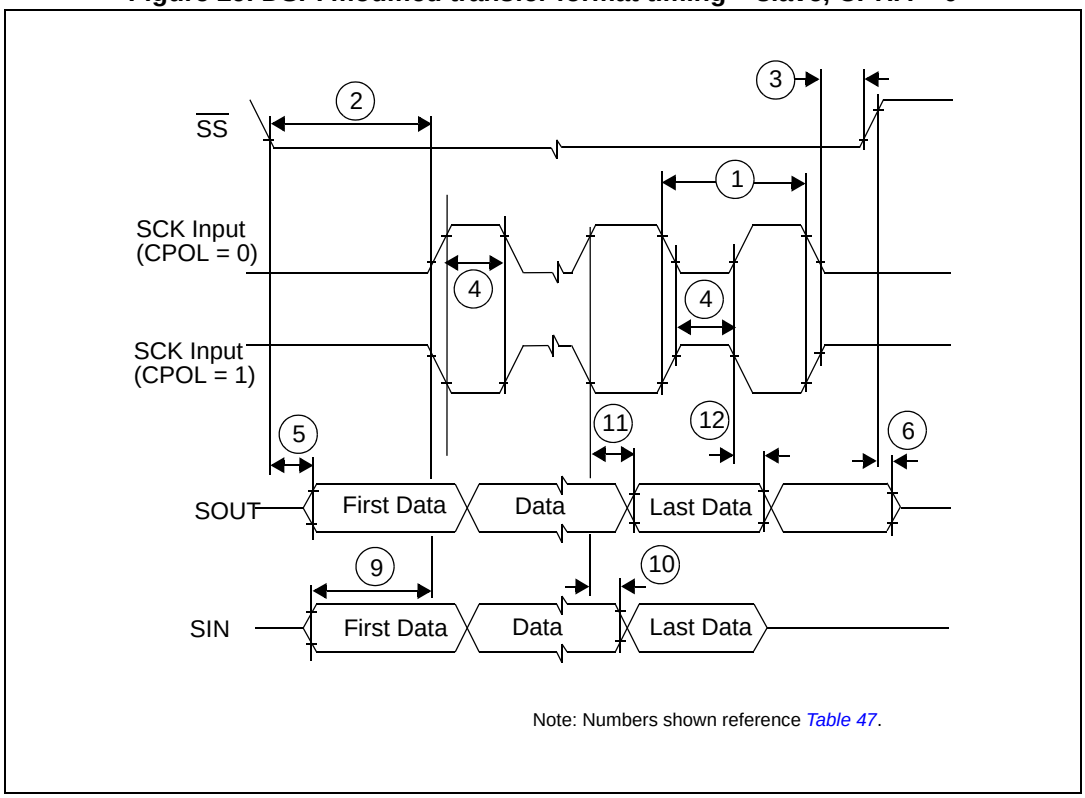
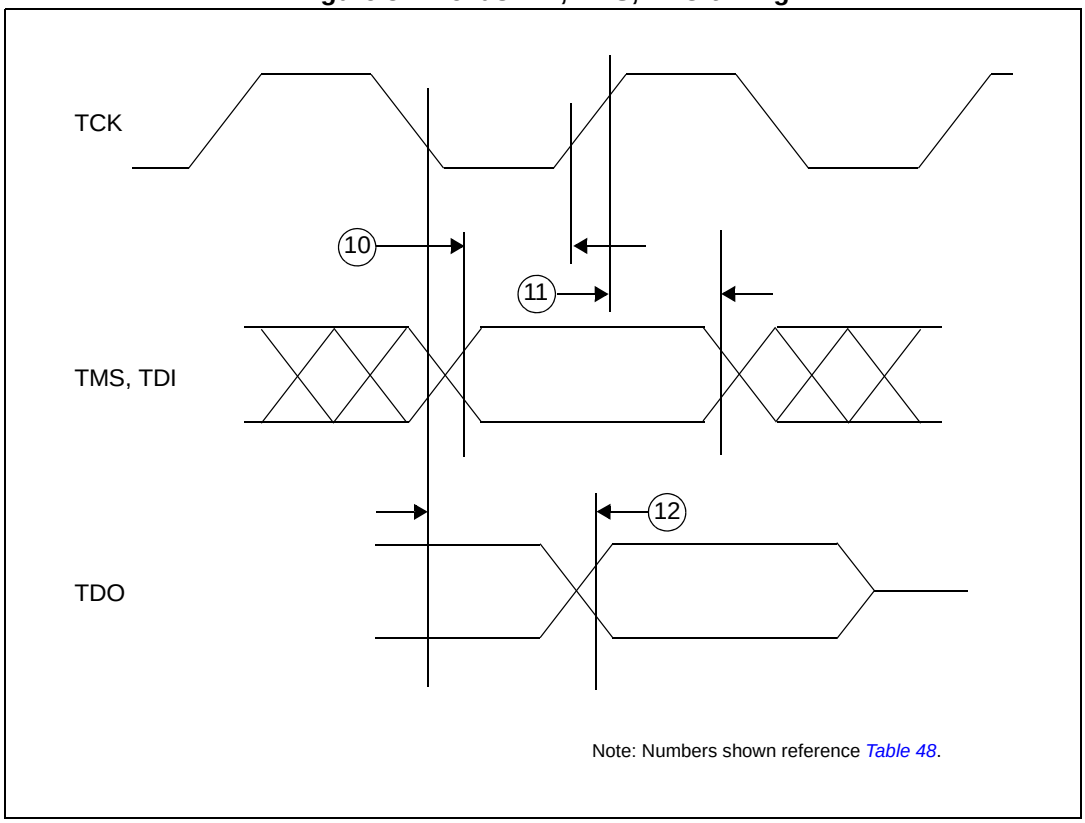


Table 48. Nexus characteristics (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
4	t_{MSEOV}	CC	D	MCKO low to MSEO_b data valid	—	—	8	ns
5	t_{EVTOV}	CC	D	MCKO low to EVTO data valid	—	—	8	ns
10	t_{NTDIS}	CC	D	TDI data setup time	15	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	15	—	—	ns
11	t_{NTDIH}	CC	D	TDI data hold time	5	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	5	—	—	ns
12	t_{TDOV}	CC	D	TCK low to TDO data valid	35	—	—	ns
13	t_{TDOI}	CC	D	TCK low to TDO data invalid	6	—	—	ns

Figure 32. Nexus TDI, TMS, TDO timing



Note: Numbers shown reference *Table 48*.

Table 50. LQFP64 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D1	9.8	10	10.2	0.3858	0.3937	0.4016
D3	—	7.5	—	—	0.2953	—
E	11.8	12	12.2	0.4646	0.4724	0.4803
E1	9.8	10	10.2	0.3858	0.3937	0.4016
E3	—	7.5	—	—	0.2953	—
e	—	0.5	—	—	0.0197	—
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1	—	1	—	—	0.0394	—
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	—	—	0.08	—	—	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

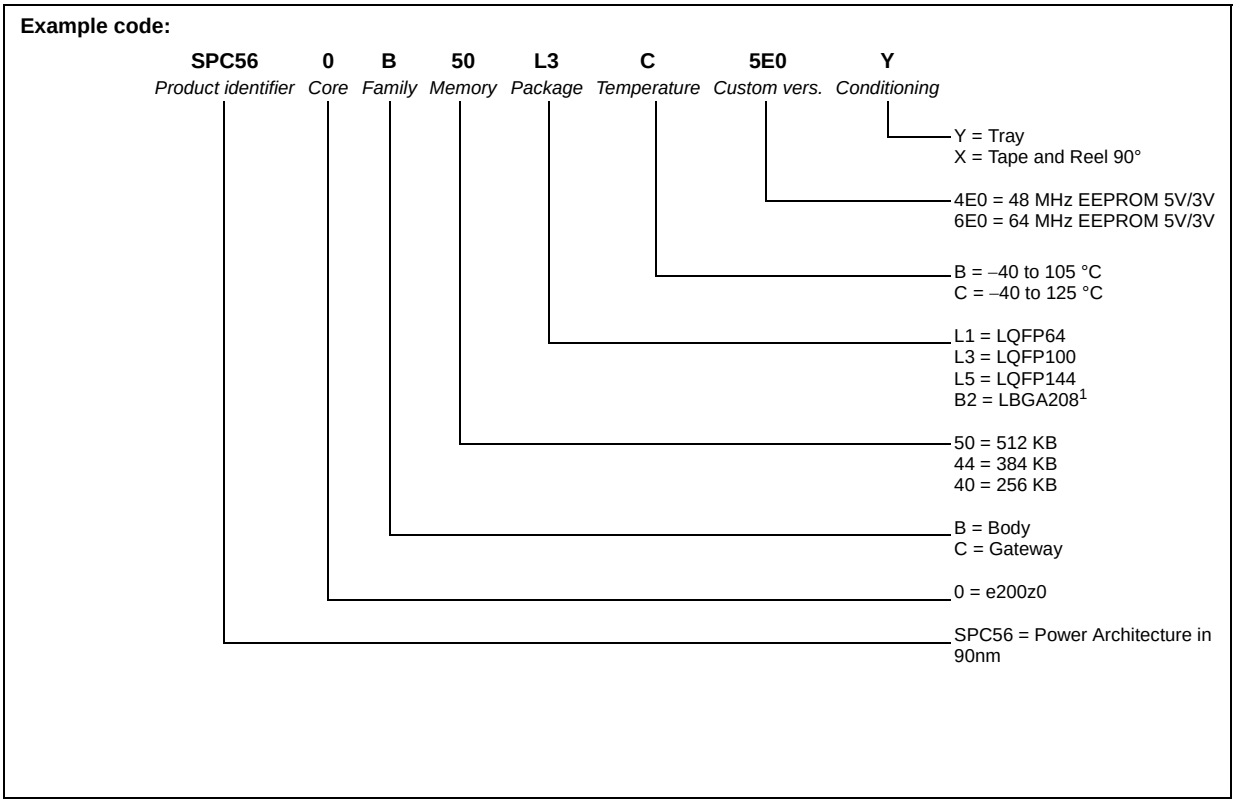
Table 52. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	—	17.500	—	—	0.6890	—
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	—	17.500	—	—	0.6890	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0°	3.5 °	0.0 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

5 Ordering information

Figure 38. Commercial product code structure



1. LBGA208 available only as development package for Nexus2+

Table 55. Document revision history (continued)

Date	Revision	Changes
06-Mar-2009	2 (continued)	Updated tables: – “I/O input DC electrical characteristics” – “I/O pull-up/pull-down DC electrical characteristics” – “SLOW configuration output buffer electrical characteristics” – “MEDIUM configuration output buffer electrical characteristics” – “FAST configuration output buffer electrical characteristics” Added “Output pin transition times” section Updated “I/O consumption” table Updated “Start-up reset requirements” figure Updated “Reset electrical characteristics” table “Voltage regulator electrical characteristics” section: – Amended description of LV_PLL “Voltage regulator capacitance connection” figure: – Exchanged position of symbols C_{DEC1} and C_{DEC2} Updated tables” – “Voltage regulator electrical characteristics” – “Low voltage monitor electrical characteristics” – “Low voltage power domain electrical characteristics” Added “Low voltage monitor vs reset” figure Updated “Flash memory electrical characteristics” section Added “Electromagnetic compatibility (EMC) characteristics” section Updated “Fast external crystal oscillator (4 to 16 MHz) electrical characteristics” section Updated “Slow external crystal oscillator (32 kHz) electrical characteristics” section Updated tables: – “FMPLL electrical characteristics” – “Fast internal RC oscillator (16 MHz) electrical characteristics” – “Slow internal RC oscillator (128 kHz) electrical characteristics” Added “On-chip peripherals” section Added “ADC input leakage current” table Updated “ADC conversion characteristics” table Updated “ECOPACK®” section Corrected inverted column headings for typical and minimum dimensions in “LQFP64 mechanical data” and “LQFP100 mechanical data” tables Added “Abbrevation” appendix
03-Jun-2009	3	Corrected “Commercial product code structure” figure

Table 55. Document revision history (continued)

Date	Revision	Changes
22-Jul-2010	7 (continued)	Table “Start-up time/Switch-off time“ – Entirely updated Figures “Crystal oscillator and resonator connection scheme“ – Relocated a note Table ”Slow external crystal oscillator (32 kHz) electrical characteristics” – Removed g_{mSXOSC} row – Inserted values of $I_{SXOSCBIAS}$ Table ”FMPLL electrical characteristics” – Rounded the values of f_{VCO} Table “Fast internal RC oscillator (16 MHz) electrical characteristics“ – Entirely updated. Table “ADC conversion characteristics” – Updated the description of the conditions of t_{ADC_PU} and $t_{ADC\_S.}$ – Added “I_{ADCPWD}” and “I_{ADCRUN}” rows Table “DSPI characteristics“ – Entirely updated. Updated “Order codes” table. Figure “Commercial product code structure” – Replaced PowerPC with “Power Architecture™“ in the product identifier – Removed the note about the condition from “Flash read access timing“ table – Removed the notes that assert the values need to be confirmed before validation – Exchanged the order of “LQFP 100-pin configuration” and “LQFP 144-pin configuration” – Exchanged the order of “LQFP 100-pin package mechanical drawing” and “LQFP 144-pin package mechanical drawing”
25-Nov-2010	8	Editorial changes and improvements. In the “SPC560B40x/50x and SPC560C40x/50x device comparison” table, changed the temperature value from 105 to 125 °C, in the footnote regarding “Execution speed”. In the “LQFP thermal characteristics” table, added values concerning LQFP64 package. In the “MEDIUM configuration output buffer electrical characteristics” table: fixed a typo in last row of conditions column, there was I_{OH} that now is I_{OL}. In the “Reset electrical characteristics” table, changed the parameter classification tag for V_{OL} and $\|I_{WPU}\|$. In the “Low voltage monitor electrical characteristics” table, changed the max value of $V_{LVDLVCORL}$ from 1.5V to 1.15V. In the “Program and erase specifications” table, replaced “T_{eslat}” with “T_{esus}”. In the “FMPLL electrical characteristics” table, changed the parameter classification tag for f_{VCO}.