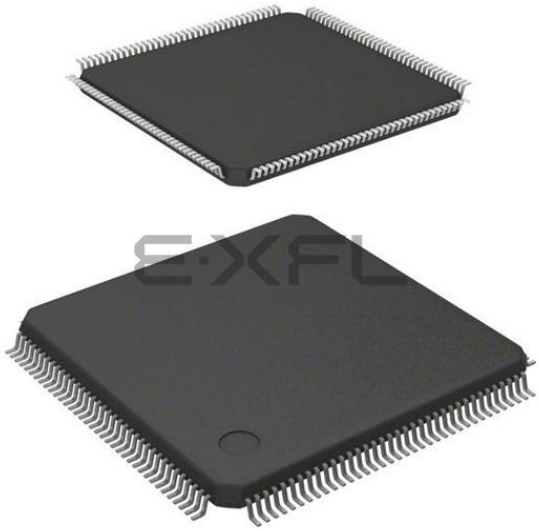


Welcome to E-XFL.COM

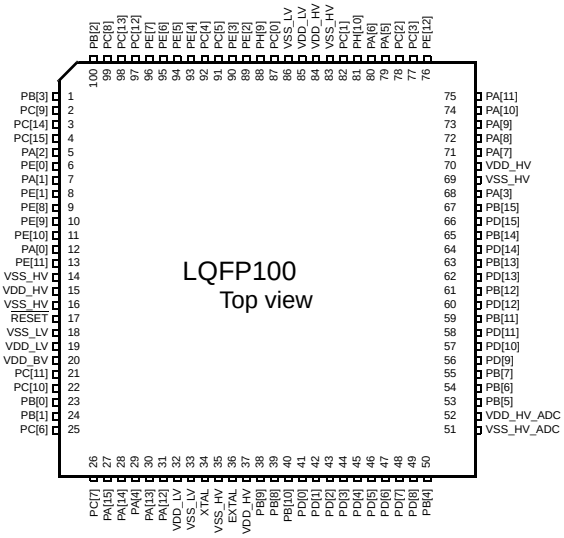
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	123
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 36x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560b40l5b6e0y

Figure 3. LQFP 100-pin configuration



Note:
Availability of port pin alternate functions depends on product selection.

Table 6. Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT — WKPU[19][4]	SIUL eMIOS_0 CGL — WKPU	I/O I/O O — I	M	Tristate	5	12	16	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — —	GPIO[1] E0UC[1] — — NMI[5] WKPU[2][4]	SIUL eMIOS_0 — — WKPU WKPU	I/O I/O — — I I	S	Tristate	4	7	11	F3
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — — WKPU[3][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	3	5	9	F2
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 —	GPIO[3] E0UC[3] — — EIRQ[0]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	43	68	90	K15
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — — WKPU[9][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	20	29	43	N6
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	51	79	118	C11
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — — EIRQ[1]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	52	80	119	D11

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PB[11] [8]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ANS[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	59	81	N13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ANX[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	61	83	M16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ANX[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	63	85	M13
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ANX[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	65	87	L16
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ANX[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	67	89	L13
PC[0][9]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	87	126	A8
PC[1][9]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO[10] —	SIUL — JTAGC —	I/O — O —	M	Tristate	54	82	121	C9

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

Equation 2 $P_D = K / (T_J + 273\ °C)$

Therefore, solving equations *Equation 1* and *Equation 2*:

Equation 3 $K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2$

Where:

K is a constant for the particular part, which may be determined from *Equation 3* by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations *Equation 1* and *Equation 2* iteratively for any value of T_A.

3.15 I/O pad electrical characteristics

3.15.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—These pads provide maximum speed. There are used for improved Nexus debugging capability.
- Input only pads—These pads are associated to ADC channels and the external 32 kHz crystal oscillator (SXOSC) providing low input leakage.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

3.15.2 I/O input DC characteristics

Table 16 provides input DC electrical characteristics as described in *Figure 6*.

Figure 6. I/O input DC electrical characteristics definition

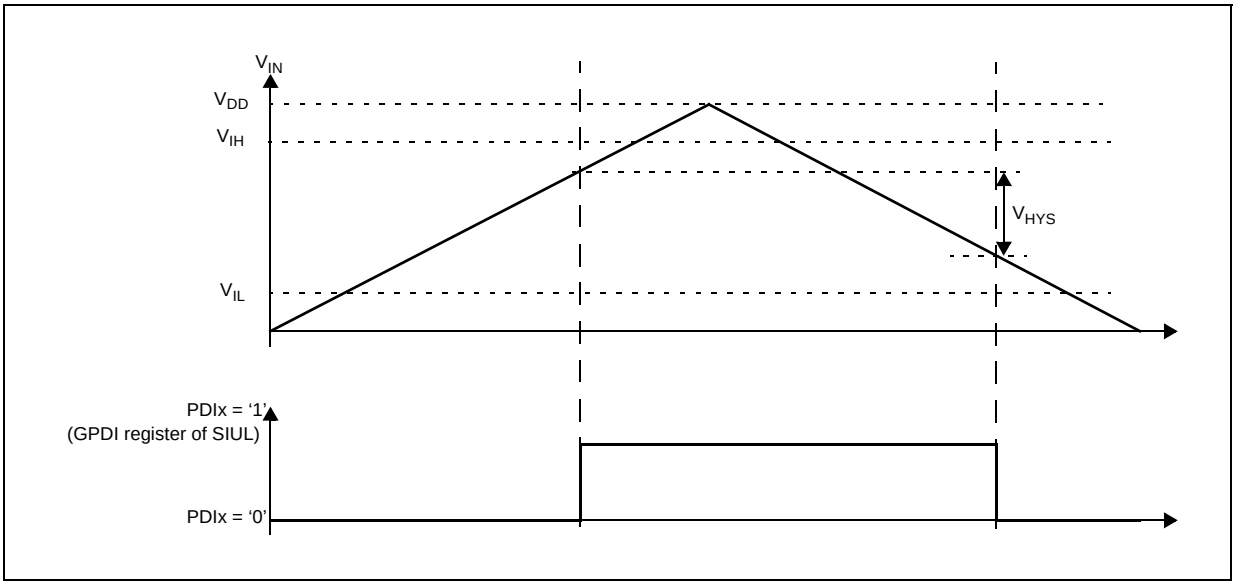


Table 16. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		–0.4	—	$0.35V_{DD}$	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	
I_{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	200	nA
		D			T_A = 25 °C	—	2	200	
		D			T_A = 85 °C	—	5	300	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}[2]	SR	P	Wakeup input filtered pulse	—		—	—	40	ns
W_{NFI}[2]	SR	P	Wakeup input not filtered pulse	—		1000	—	—	ns

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

Table 18. SLOW configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 19. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD}–0.8	—	—	
		C			I_{OH} = –100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		P			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
		C			I_{OL} = 100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 20. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull	I_{OH} = –14mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –7mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –11mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD}–0.8	—	—	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull	I_{OL} = 14mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 7mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 11mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.15.4 Output pin transition times

Table 21. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	

Table 21. Output pin transition times (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
t_{tr}	CC	D	Output transition time output pin[2] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).

3.15.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 22*.

Table 22. I/O supply segment

Package	Supply segment					
	1	2	3	4	5	6
LBGA208[1]	Equivalent to LQFP144 segment pad distribution				MCKO	MDOn/MSEO
LQFP144	pin20–pin49	pin51–pin99	pin100–pin122	pin 123–pin19	—	—
LQFP100	pin16–pin35	pin37–pin69	pin70–pin83	pin 84–pin15	—	—
LQFP64[2]	pin8–pin26	pin28–pin55	pin56–pin7	—	—	—

1. LBGA208 available only as development package for Nexus2+
2. All LQFP64 information is indicative and must be confirmed during silicon validation.

Table 23 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 24. I/O weight[1] (continued)

Supply segment			Pad	LQFP144/LQFP100				LQFP64[2]			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
LQFP 144	LQFP 100	LQFP 64		SRC[3] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
	2	2	PB[9]	1%	—	1%	—	1%	—	1%	—
			PB[8]	1%	—	1%	—	1%	—	1%	—
			PB[10]	6%	—	7%	—	6%	—	7%	—
	—	—	PF[0]	6%	—	7%	—	—	—	—	—
	—	—	PF[1]	7%	—	8%	—	—	—	—	—
	—	—	PF[2]	7%	—	8%	—	—	—	—	—
	—	—	PF[3]	7%	—	9%	—	—	—	—	—
	—	—	PF[4]	8%	—	9%	—	—	—	—	—
	—	—	PF[5]	8%	—	10%	—	—	—	—	—
	—	—	PF[6]	8%	—	10%	—	—	—	—	—
	—	—	PF[7]	9%	—	10%	—	—	—	—	—
	2	—	PD[0]	1%	—	1%	—	—	—	—	—
		—	PD[1]	1%	—	1%	—	—	—	—	—
		—	PD[2]	1%	—	1%	—	—	—	—	—
		—	PD[3]	1%	—	1%	—	—	—	—	—
2		—	PD[4]	1%	—	1%	—	—	—	—	—
		—	PD[5]	1%	—	1%	—	—	—	—	—
		—	PD[6]	1%	—	1%	—	—	—	—	—
		—	PD[7]	1%	—	1%	—	—	—	—	—
		—	PD[8]	1%	—	1%	—	—	—	—	—
		2	PB[4]	1%	—	1%	—	1%	—	1%	—
			PB[5]	1%	—	1%	—	1%	—	2%	—
			PB[6]	1%	—	1%	—	1%	—	2%	—
			PB[7]	1%	—	1%	—	1%	—	2%	—
		—	PD[9]	1%	—	1%	—	—	—	—	—
		—	PD[10]	1%	—	1%	—	—	—	—	—
		—	PD[11]	1%	—	1%	—	—	—	—	—
		2	PB[11]	11%	—	13%	—	17%	—	21%	—
		—	PD[12]	11%	—	13%	—	—	—	—	—
		2	PB[12]	11%	—	13%	—	18%	—	21%	—
		—	PD[13]	10%	—	12%	—	—	—	—	—

Table 26. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	W
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100 [3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
$\left\|\frac{d}{dt}VDD\right\|$	SR	—	Maximum slope on V_{DD}		—	—	250	mV/µs
$\|\Delta_{VDD(STDBY)}\|$	SR	—	Maximum instant variation on V_{DD} during standby exit		—	—	30	mV
$\left\|\frac{d}{dt}VDD(STDBY)\right\|$	SR	—	Maximum slope on V_{DD} during standby exit		—	—	15	mV/µs
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.16	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V

$ESR_{STDBY}(MAX) = |\Delta_{VDD(STDBY)}|/(I_{DD\_BV} - 200\ mA) = (30\ mV)/(100\ mA) = 0.3\ \Omega$

$C_{STDBY}(MIN) = (I_{DD\_BV} - 200\ mA)/dVDD(STDBY)/dt = (300\ mA - 200\ mA)/(15\ mV/\mu s) = 6.7\ \mu F$

In case optimization is required, $C_{STDBY}(MIN)$ and $ESR_{STDBY}(MAX)$ should be calculated based on the regulator characteristics as well as the board V_{DD} plane characteristics.

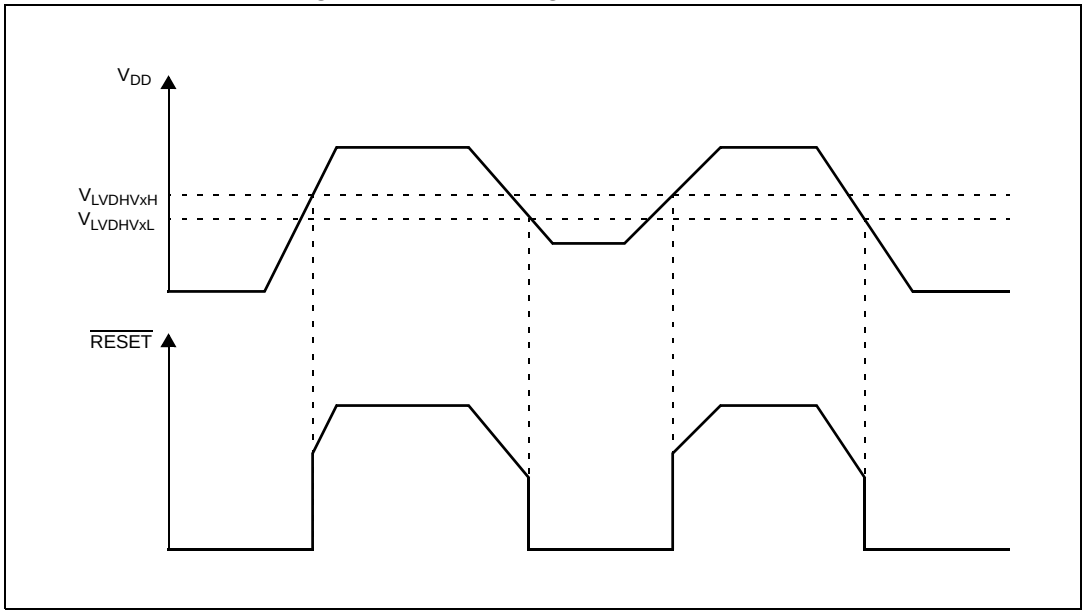
3.17.2 Low voltage detector electrical characteristics

The device implements a Power-on Reset (POR) module to ensure correct power-up initialization, as well as four low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state (refer to RGM Destructive Event Status (RGM_DES) Register flag F_POR in device reference manual)
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27 in device reference manual)
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range (refer to RGM Functional Event Status (RGM_FES) Register flag F_LVD45 in device reference manual)
- LVDLVCOR monitors power domain No. 1 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD1 in device reference manual
- LVDLVBKP monitors power domain No. 0 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD0 in device reference manual)

Note: When enabled, power domain No. 2 is monitored through LVDLVBKP.

Figure 12. Low voltage detector vs reset



Note: Figure 12: Low voltage detector vs reset does not apply to LVDHV5 low voltage detector because LVDHV5 is automatically disabled during reset and it must be enabled by software again. Once the device is forced to reset by LVDHV5, the LVDHV5 is disabled and reset is

Table 31. Flash read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.19.2 Flash power supply DC characteristics

Table 32 shows the power supply DC characteristics on external supply.

Table 32. Flash memory power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{FREAD} (2)	CC	D	Sum of the current consumption on VDD_HV and VDD_BV on read access	Code flash memory module read f_{CPU} = 64 MHz(3)	—	15	33	mA
				Data flash memory module read f_{CPU} = 64 MHz(3)	—	15	33	
I_{FMOD}(2)	CC	D	Sum of the current consumption on VDD_HV and VDD_BV on matrix modification (program/erase)	Program/Erase ongoing while reading code flash memory registers f_{CPU} = 64 MHz(3)	—	15	33	mA
				Program/Erase ongoing while reading data flash memory registers f_{CPU} = 64 MHz(3)	—	15	33	
I_{FLPW}	CC	D	Sum of the current consumption on VDD_HV and VDD_BV	During code flash memory low-power mode	—	—	900	µA
				During data flash memory low-power mode	—	—	900	
I_{FPWD}	CC	D	Sum of the current consumption on VDD_HV and VDD_BV	During code flash memory power-down mode	—	—	150	µA
				During data flash memory power-down mode	—	—	150	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. This value is only relative to the actual duration of the read cycle
3. f_{CPU} 64 MHz can be achieved only at up to 105 °C

2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.20.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 36. Latch-up results

Symbol		C	Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.21 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. *Figure 13* describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 37 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{p2} substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{p2} equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_c \times (C_S+C_{p2}))$, where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{p2}) and the sum of $R_S + R_F$, the external circuit must be designed to respect the *Equation 4*:

Equation 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on a resistive path.

4.2.2 LQFP100

Figure 35. LQFP100 package mechanical drawing

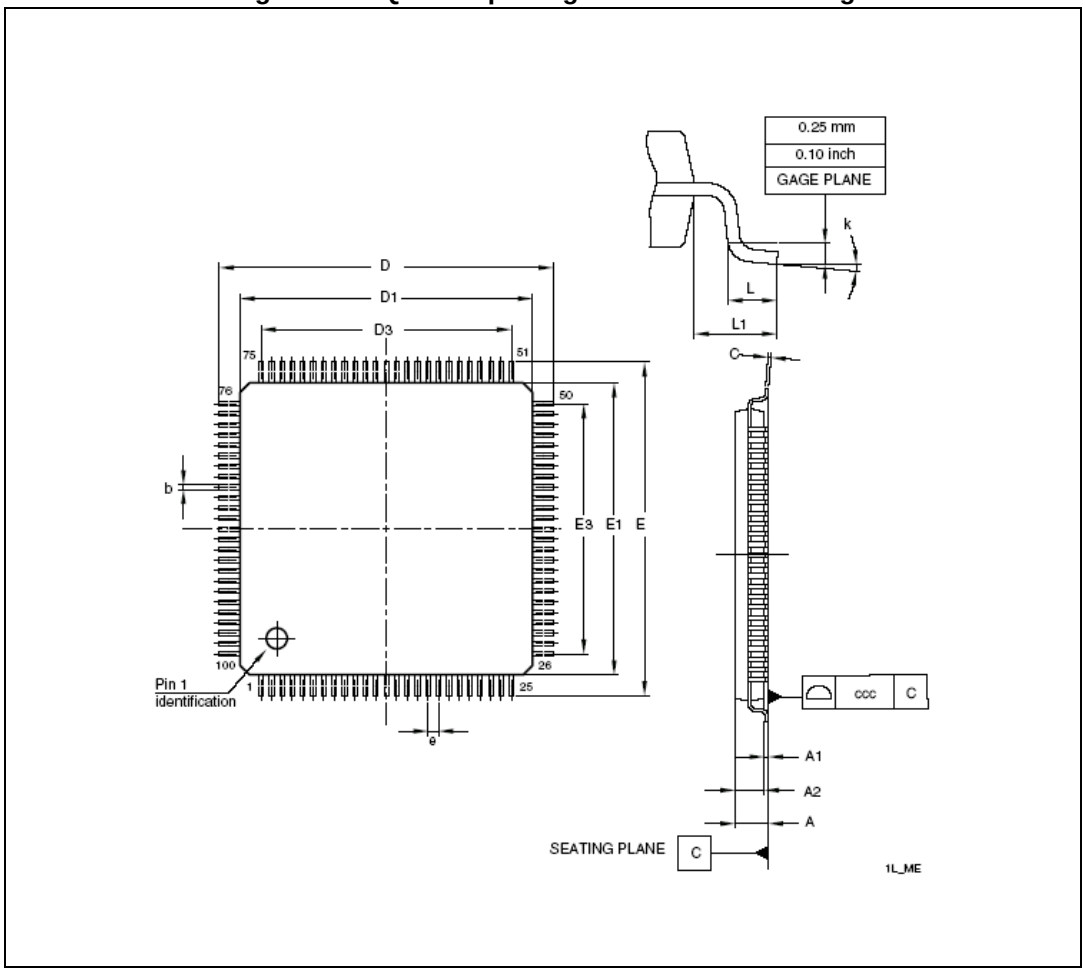
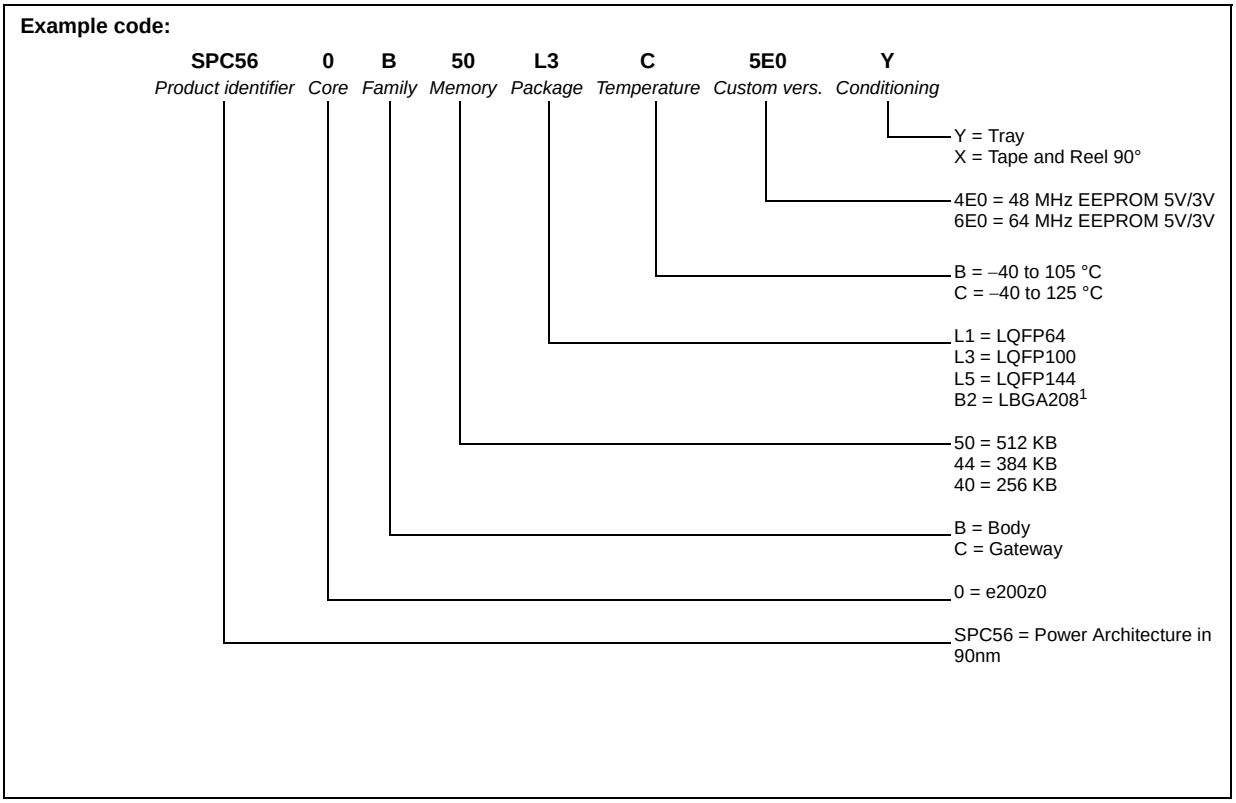


Table 51. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

5 Ordering information

Figure 38. Commercial product code structure



1. LBGA208 available only as development package for Nexus2+

Appendix A Abbreviations

Table 54 lists abbreviations used but not defined elsewhere in this document.

Table 54. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

Table 55. Document revision history (continued)

Date	Revision	Changes
22-Jul-2010	7	**Changes between revisions 5 and 7** Added LQFP64 package information Updated the “Features“ section. Section “Introduction” – Relocated a note Table: “SPC560B40x/50x and SPC560C40x/50x device comparison“ – Added footnote regarding SCI and CAN Added eDMA block in the “SPC560B40x/50x and SPC560C40x/50x series block diagram” figure Removed alternate function information from “LQFP 100-pin configuration” and “LQFP 100-pin configuration” figures. Added “Functional port pin descriptions” table Deleted the “NVUSRO[WATCHDOG_EN] field description“ section Table: “Absolute maximum ratings“ – Removed the min value of V_{IN} relative tio V_{DD} Table ”Recommended operating conditions (3.3 V)” – TV_{DD}: made single row ”Recommended operating conditions (5.0 V)” – deleted $T_{A\ C\text{-}Grade\ Part}$, $T_{J\ C\text{-}Grade\ Part}$, $T_{A\ V\text{-}Grade\ Part}$, $T_{J\ V\text{-}Grade\ Part}$, $T_{A\ M\text{-}Grade\ Part}$, $T_{J\ M\text{-}Grade\ Part}$ rows Table: “LQFP thermal characteristics” – Added more rows – Rounded the values Removed table “LBGA208 thermal characteristics” Table “I/O input DC electrical characteristics” – W_{FI}: insered a footnote – W_{NFI}: insered a footnote Table “I/O consuption“ – Removed I_{DYNSEG} row – Added “I/O weight “ table Replaced “$\overline{\text{nRSTIN}}$” with “$\overline{\text{RESET}}$” in the “$\overline{\text{RESET}}$ electrical characteristics” section. Table “Voltage regulator electrical characteristics“ – Updated the values – Removed $I_{VREGREF}$ and $I_{VREDLVD12}$ – Added a note about I_{DD_BC} Table: “Low voltage monitor electrical characteristics“ – changed min value$V_{LVDHV3L}$, from 2.7 to 2.6 – Inserted max value of $V_{LVDLVCORL}$ – Updated V_{PORH} values – Updated $V_{LVDLVCORL}$ value Table “Low voltage power domain electrical characteristics“ – Entirely updated Table “Program and erase specifications“ – Inserted T_{eslat} row Table “Flash power supply DC electrical characteristics“ – Entirely updated

Table 55. Document revision history (continued)

Date	Revision	Changes
01-Oct-2011	9	Formatting and minor editorial changes throughout Harmonized oscillator nomenclature Device summary table: removed 384 KB code flash device versions Device comparison table: changed temperature value in footnote 2 from 105 °C to 125 °C; removed 384 KB code flash device versions LQFP 64-pin configuration: renamed pin 6 from VPP_TEST to VSS_HV Removed “Pin Muxing” section; added sections “Pad configuration during reset phases”, “Voltage supply pins”, “Pad types”, “System pins,” “Functional ports”, and “Nexus 2+ pins” Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality; updated footnote describing default value of ‘1’ in field descriptions NVUSRO[PAD3V5V] and NVUSRO[OSCILLATOR_MARGIN] Added section “NVUSRO[WATCHDOG_EN] field description” Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V): updated conditions for ambient and junction temperature characteristics I/O input DC electrical characteristics: updated I_{LKG} characteristics Section “I/O pad current specification”: removed content referencing the I_{DYNSEG} maximum value I/O consumption: replaced instances of “Root medium square” with “Root mean square” I/O weight: replaced instances of bit “SRE” with “SRC”; added pads PH[9] and PH[10]; added supply segments; removed weight values in 64-pin LQFP for pads that do not exist in that package Reset electrical characteristics: updated parameter classification for $\|I_{WPU}\|$ Updated Voltage regulator electrical characteristics Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$; replaced “LVD_DIGBKP” with “LVDLVBKP” in note Updated section “Power consumption” Fast external crystal oscillator (4 to 16 MHz) electrical characteristics: updated parameter classification for $V_{FXOSCOP}$ Crystal oscillator and resonator connection scheme: added footnote about possibility of adding a series resistor Slow external crystal oscillator (32 kHz) electrical characteristics: updated footnote 1 FMPLL electrical characteristics: added short term jitter characteristics; inserted “—” in empty min value cell of t_{lock} row Section “Input impedance and ADC accuracy”: changed “V_A/V_{A2}” to “V_{A2}/V_A” in Equation 11 ADC input leakage current: updated I_{LKG} characteristics ADC conversion characteristics: updated symbols On-chip peripherals current consumption: changed “supply current on “$V_{DD\_HV\_ADC}$” to “supply current on” V_{DD_HV}” in $I_{DD\_HV(FLASH)}$ row; updated $I_{DD\_HV(PLL)}$ value—was 3 * f_{periph}, is 30 * f_{periph}; updated footnotes DSPI characteristics: added rows t_{PCSC} and t_{PASC} Added DSPI PCS strobe (PCSS) timing diagram Updated order codes.
17-Jan-2013	10	Internal review.