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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	45
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560b50l1b4e0y

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Table 2. SPC560B40x/50x and SPC560C40x/50x device comparison⁽¹⁾

Feature	Device										
	SPC560B 40L1	SPC560B 40L3	SPC560B 40L5	SPC560C 40L1	SPC560C 40L3	SPC560B 50L1	SPC560B 50L3	SPC560B 50L5	SPC560C 50L1	SPC560C 50L3	SPC560B 50B2
CPU	e200z0h										
Execution speed ⁽²⁾	Static – up to 64 MHz										
Code Flash	256 KB					512 KB					
Data Flash	64 KB (4 × 16 KB)										
RAM	24 KB			32 KB		32 KB			48 KB		
MPU	8-entry										
ADC (10-bit)	12 ch	28 ch	36 ch	8 ch	28 ch	12 ch	28 ch	36 ch	8 ch	28 ch	36 ch
CTU	Yes										
Total timer I/O ⁽³⁾ eMIOS	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit
– PWM + MC + IC/OC ⁽⁴⁾	2 ch	5 ch	10 ch	2 ch	5 ch	2 ch	5 ch	10 ch	2 ch	5 ch	10 ch
– PWM + IC/OC ⁽⁴⁾	10 ch	20 ch	40 ch	10 ch	20 ch	10 ch	20 ch	40 ch	10 ch	20 ch	40 ch
– IC/OC ⁽⁴⁾	—	3 ch	6 ch	—	3 ch	—	3 ch	6 ch	—	3 ch	6 ch
SCI (LINFlex)	3 ⁽⁵⁾			4							
SPI (DSPI)	2	3		2	3	2	3		2	3	
CAN (FlexCAN)	2 ⁽⁶⁾			5	6	3 ⁽⁷⁾			5	6	
I ² C	1										
32 kHz oscillator	Yes										
GPIO ⁽⁸⁾	45	79	123	45	79	45	79	123	45	79	123

Figure 1. SPC560B40x/50x and SPC560C40x/50x block diagram

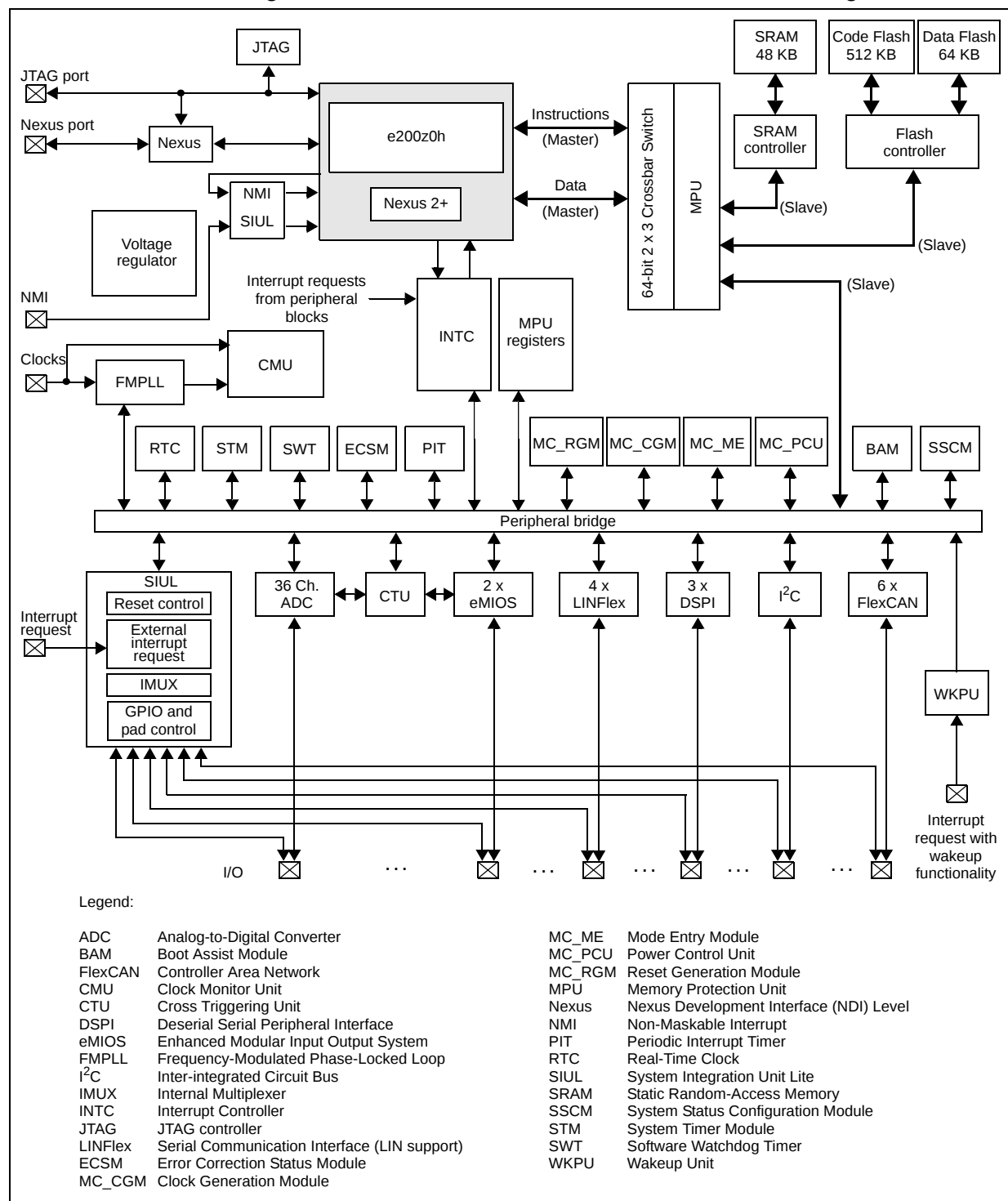


Table 3 summarizes the functions of all blocks present in the SPC560B40x/50x and SPC560C40x/50x series of microcontrollers. Please note that the presence and number of blocks vary by device and package.

Figure 5. LBGA208 configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[8]	PC[13]	NC	NC	PH[8]	PH[4]	PC[5]	PC[0]	NC	NC	PC[2]	NC	PE[15]	NC	NC	NC	A
B	PC[9]	PB[2]	NC	PC[12]	PE[6]	PH[5]	PC[4]	PH[9]	PH[10]	NC	PC[3]	PG[11]	PG[15]	PG[14]	PA[11]	PA[10]	B
C	PC[14]	VDD_HV	PB[3]	PE[7]	PH[7]	PE[5]	PE[3]	VSS_LV	PC[1]	NC	PA[5]	NC	PE[14]	PE[12]	PA[9]	PA[8]	C
D	NC	NC	PC[15]	NC	PH[6]	PE[4]	PE[2]	VDD_LV	VDD_HV	NC	PA[6]	NC	PG[10]	PF[14]	PE[13]	PA[7]	D
E	PG[4]	PG[5]	PG[3]	PG[2]									PG[1]	PG[0]	PF[15]	VDD_HV	E
F	PE[0]	PA[2]	PA[1]	PE[1]									PH[0]	PH[1]	PH[3]	PH[2]	F
G	PE[9]	PE[8]	PE[10]	PA[0]									VDD_HV	NC	NC	MSEO	G
H	VSS_HV	PE[11]	VDD_HV	NC									MDO3	MDO2	MDO0	MDO1	H
J	RESET	VSS_LV	NC	NC									NC	NC	NC	NC	J
K	EVTI	NC	VDD_BV	VDD_LV									NC	PG[12]	PA[3]	PG[13]	K
L	PG[9]	PG[8]	NC	EVTO									PB[15]	PD[15]	PD[14]	PB[14]	L
M	PG[7]	PG[6]	PC[10]	PC[11]									PB[13]	PD[13]	PD[12]	PB[12]	M
N	PB[1]	PF[9]	PB[0]	NC	NC	PA[4]	VSS_LV	EXTAL	VDD_HV	PF[0]	PF[4]	NC	PB[11]	PD[10]	PD[9]	PD[11]	N
P	PF[8]	NC	PC[7]	NC	NC	PA[14]	VDD_LV	XTAL	PB[10]	PF[1]	PF[5]	PD[0]	PD[3]	VDD_HV_ADC	PB[6]	PB[7]	P
R	PF[12]	PC[6]	PF[10]	PF[11]	VDD_HV	PA[15]	PA[13]	NC	OSC32K_XTAL	PF[3]	PF[7]	PD[2]	PD[4]	PD[7]	VSS_HV_ADC	PB[5]	R
T	NC	NC	NC	MCKO	NC	PF[13]	PA[12]	NC	OSC32K_EXTAL	PF[2]	PF[6]	PD[1]	PD[5]	PD[6]	PD[8]	PB[4]	T

1. Note: LBGA208 available only as development package for Nexus 2+.

NC = Not connected

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are forced to tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS[0]) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS and TDI) are pull-up whilst TDO remains tristate.
- Precise ADC pads (PB[7:4] and PD[11:0]) are tristate (no output buffer available).
- Main oscillator pads (EXTAL, XTAL) are tristate.
- Nexus output pads (MDO[n], MCKO, EVTO, MSEO) are forced to output.

3.5 System pins

The system pins are listed in [Table 5](#).

Table 5. System pin descriptions

System pin	Function	I/O direction	Pad type	RESET configuration	Pin number			
					LQFP64	LQFP100	LQFP144	LBGA208 ⁽¹⁾
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	9	17	21	J1
EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode. ⁽²⁾	I/O	X	Tristate	27	36	50	N8
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode. ⁽²⁾	I	X	Tristate	25	34	48	P8

1. LBGA208 available only as development package for Nexus2+

2. See the relevant section of the datasheet

3.6 Functional ports

The functional port pins are listed in [Table 6](#).

- c. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium (see PCR.SRC in section Pad Configuration Registers (PCR0–PCR122) in the device reference manual).

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208 ⁽³⁾
PB[11] (8)	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ANS[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	59	81	N13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ANX[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	61	83	M16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ANX[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	63	85	M13
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ANX[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	65	87	L16
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ANX[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	67	89	L13
PC[0] ⁽⁹⁾	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	87	126	A8
PC[1] ⁽⁹⁾	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO ⁽¹⁰⁾ —	SIUL — JTAGC —	I/O — O —	M	Tristate	54	82	121	C9

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208 ⁽³⁾
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX — —	SIUL LINFlex_2 — —	I/O O — —	S	Tristate	63	99	143	A1
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — — — LIN2RX WKPU[13] ⁽⁴⁾	SIUL — — — LINFlex_2 WKPU	I/O — — — I I	S	Tristate	2	2	2	B1
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX ⁽¹¹⁾ MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC	I/O O O O	M	Tristate	13	22	28	M3
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — — CAN1RX CAN4RX ⁽¹¹⁾ WKPU[5] ⁽⁴⁾	SIUL — — — FlexCAN_1 FlexCAN_4 WKPU	I/O — — — I I I	S	Tristate	—	21	27	M4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — SIN_2	SIUL eMIOS_0 — — DSPI_2	I/O I/O — — I	M	Tristate	—	97	141	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	—	98	142	A2
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	—	3	3	C1

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208 ⁽³⁾
PC[15]	PCR[47]	AF0 AF1 AF2 AF3	GPIO[47] E0UC[15] CS0_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O I/O —	M	Tristate	—	4	4	D3
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 —	GPIO[48] — — — GPI[4]	SIUL — — — ADC	I — — — I	I	Tristate	—	41	63	P12
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 —	GPIO[49] — — — GPI[5]	SIUL — — — ADC	I — — — I	I	Tristate	—	42	64	T12
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 —	GPIO[50] — — — GPI[6]	SIUL — — — ADC	I — — — I	I	Tristate	—	43	65	R12
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 —	GPIO[51] — — — GPI[7]	SIUL — — — ADC	I — — — I	I	Tristate	—	44	66	P13
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 —	GPIO[52] — — — GPI[8]	SIUL — — — ADC	I — — — I	I	Tristate	—	45	67	R13
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 —	GPIO[53] — — — GPI[9]	SIUL — — — ADC	I — — — I	I	Tristate	—	46	68	T13

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208 ⁽³⁾
PG[7]	PCR[103]	AF0 AF1 AF2 AF3	GPIO[103] E1UC[16] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	29	M1
PG[8]	PCR[104]	AF0 AF1 AF2 AF3 —	GPIO[104] E1UC[17] — CS0_2 EIRQ[15]	SIUL eMIOS_1 — DSPI_2 SIUL	I/O I/O — I/O I	S	Tristate	—	—	26	L2
PG[9]	PCR[105]	AF0 AF1 AF2 AF3	GPIO[105] E1UC[18] — SCK_2	SIUL eMIOS_1 — DSPI_2	I/O I/O — I/O	S	Tristate	—	—	25	L1
PG[10]	PCR[106]	AF0 AF1 AF2 AF3	GPIO[106] E0UC[24] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	—	114	D13
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	115	B12
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	92	K14
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	91	K16
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	—	110	B14

Table 12. Absolute maximum ratings (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	−0.3	6.0	V
			Relative to V_{DD}	—	$V_{DD}+0.3$	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	−10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	−50	50	
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment	$V_{DD} = 5.0\text{ V} \pm 10\%$, $PAD3V5V = 0$	—	70	mA
			$V_{DD} = 3.3\text{ V} \pm 10\%$, $PAD3V5V = 1$	—	64	
I_{CORELV}	SR	Low voltage static current sink through VDD_BV	—	—	150	mA
$T_{STORAGE}$	SR	Storage temperature	—	−55	150	°C

Note: Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

3.13 Recommended operating conditions

Table 13. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD}^{(1)}$	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
$V_{SS_LV}^{(2)}$	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	$V_{SS}-0.1$	$V_{SS}+0.1$	V
$V_{DD_BV}^{(3)}$	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V_{DD}	$V_{DD}-0.1$	$V_{DD}+0.1$	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	$V_{SS}-0.1$	$V_{SS}+0.1$	V
$V_{DD_ADC}^{(4)}$	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	3.0 ⁽⁵⁾	3.6	V
			Relative to V_{DD}	$V_{DD}-0.1$	$V_{DD}+0.1$	

Table 15. LQFP thermal characteristics⁽¹⁾ (continued)

Symbol		C	Parameter	Conditions ⁽²⁾	Pin count	Value	Unit
$R_{\theta JC}$	CC	D	Thermal resistance, junction-to-case ⁽⁵⁾	Single-layer board - 1s	64	11	°C/W
					100	22	
					144	22	
				Four-layer board - 2s2p	64	11	
					100	22	
					144	22	
Ψ_{JB}	CC	D	Junction-to-board thermal characterization parameter, natural convection	Single-layer board - 1s	64	TBD	°C/W
					100	33	
					144	34	
				Four-layer board - 2s2p	64	TBD	
					100	34	
					144	35	
Ψ_{JC}	CC	D	Junction-to-case thermal characterization parameter, natural convection	Single-layer board - 1s	64	TBD	°C/W
					100	9	
					144	10	
				Four-layer board - 2s2p	64	TBD	
					100	9	
					144	10	

1. Thermal characteristics are based on simulation.
2. $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to $125\text{ }^{\circ}\text{C}$
3. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
4. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
5. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

3.14.2 Power considerations

The average chip-junction temperature, T_J , in degrees Celsius, may be calculated using [Equation 1](#):

$$\text{Equation 1 } T_J = T_A + (P_D \times R_{\theta JA})$$

Where:

T_A is the ambient temperature in $^{\circ}\text{C}$.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in $^{\circ}\text{C/W}$.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD} , expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Figure 6. I/O input DC electrical characteristics definition

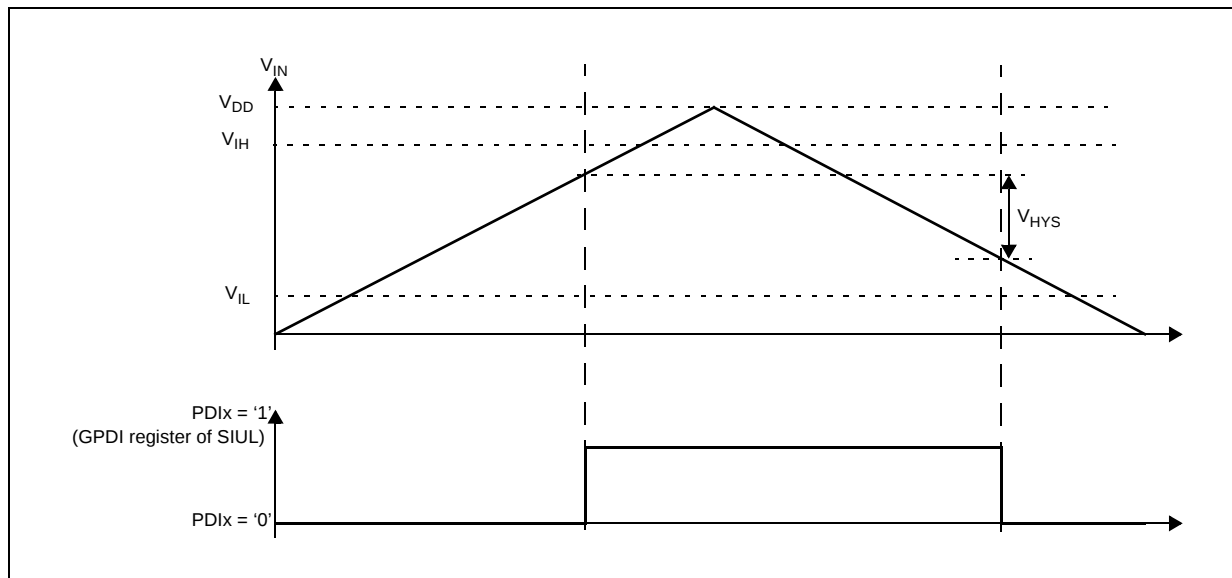


Table 16. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions ⁽¹⁾		Value			Unit
						Min	Typ	Max	
V _{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		0.65V _{DD}	—	V _{DD} +0.4	V
V _{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		−0.4	—	0.35V _{DD}	
V _{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		0.1V _{DD}	—	—	
I _{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T _A = −40 °C	—	2	200	nA
		D			T _A = 25 °C	—	2	200	
		D			T _A = 85 °C	—	5	300	
		D			T _A = 105 °C	—	12	500	
		P			T _A = 125 °C	—	70	1000	
W _{FI} ⁽²⁾	SR	P	Wakeup input filtered pulse	—		—	—	40	ns
W _{NFI} ⁽²⁾	SR	P	Wakeup input not filtered pulse	—		1000	—	—	ns

1. $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40\text{ to }125\text{ °C}$, unless otherwise specified

2. In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

2. The configuration PAD3V5 = 1 when $V_{DD} = 5\text{ V}$ is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 20. FAST configuration output buffer electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit
				Min	Typ	Max	
V_{OH}	CC	Output high level FAST configuration	Push Pull	$I_{OH} = -14\text{mA}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	V
				$I_{OH} = -7\text{mA}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, PAD3V5V = 1 ⁽²⁾	$0.8V_{DD}$	—	
				$I_{OH} = -11\text{mA}$, $V_{DD} = 3.3\text{ V} \pm 10\%$, PAD3V5V = 1 (recommended)	$V_{DD}-0.8$	—	
V_{OL}	CC	Output low level FAST configuration	Push Pull	$I_{OL} = 14\text{mA}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, PAD3V5V = 0 (recommended)	—	$0.1V_{DD}$	V
				$I_{OL} = 7\text{mA}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, PAD3V5V = 1 ⁽²⁾	—	$0.1V_{DD}$	
				$I_{OL} = 11\text{mA}$, $V_{DD} = 3.3\text{ V} \pm 10\%$, PAD3V5V = 1 (recommended)	—	0.5	

1. $V_{DD} = 3.3\text{ V} \pm 10\%$ / $5.0\text{ V} \pm 10\%$, $T_A = -40$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified

2. The configuration PAD3V5 = 1 when $V_{DD} = 5\text{ V}$ is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.15.4 Output pin transition times

Table 21. Output pin transition times

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit
				Min	Typ	Max	
t_{tr}	CC	Output transition time output pin ⁽²⁾ SLOW configuration	$C_L = 25\text{ pF}$	$V_{DD} = 5.0\text{ V} \pm 10\%$, PAD3V5V = 0	—	50	ns
			$C_L = 50\text{ pF}$		—	100	
			$C_L = 100\text{ pF}$		—	125	
			$C_L = 25\text{ pF}$	$V_{DD} = 3.3\text{ V} \pm 10\%$, PAD3V5V = 1	—	50	
			$C_L = 50\text{ pF}$		—	100	
			$C_L = 100\text{ pF}$		—	125	

$$ESR_{STDBY}(MAX) = |\Delta V_{DD}(STDBY)| / (I_{DD_BV} - 200 \text{ mA}) = (30 \text{ mV}) / (100 \text{ mA}) = 0.3 \Omega$$

$$C_{STDBY}(MIN) = (I_{DD_BV} - 200 \text{ mA}) / dV_{DD}(STDBY) / dt = (300 \text{ mA} - 200 \text{ mA}) / (15 \text{ mV}/\mu\text{s}) = 6.7 \mu\text{F}$$

In case optimization is required, $C_{STDBY}(MIN)$ and $ESR_{STDBY}(MAX)$ should be calculated based on the regulator characteristics as well as the board V_{DD} plane characteristics.

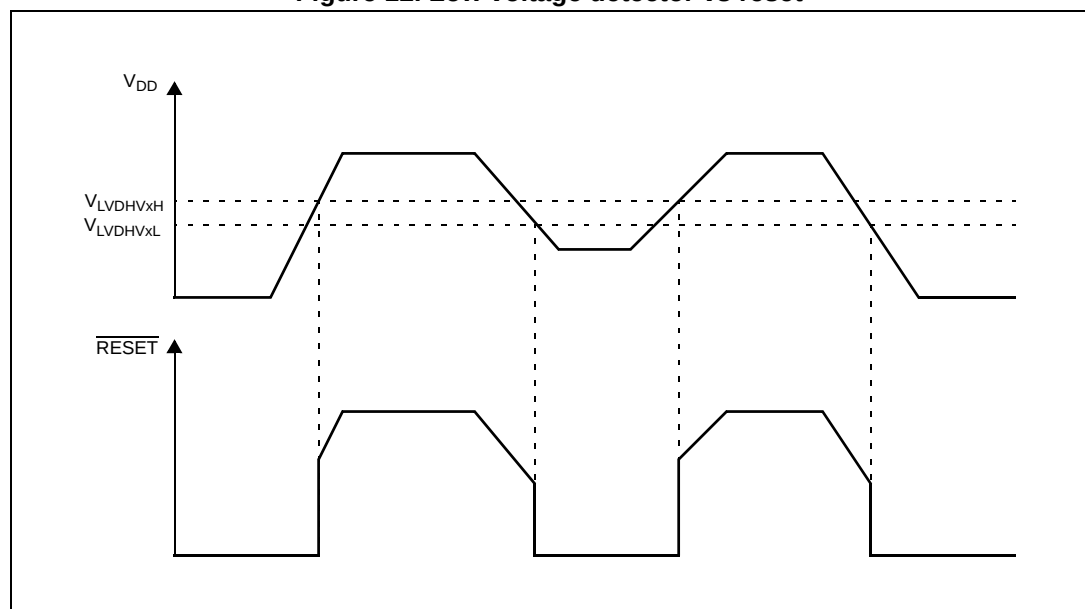
3.17.2 Low voltage detector electrical characteristics

The device implements a Power-on Reset (POR) module to ensure correct power-up initialization, as well as four low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state (refer to RGM Destructive Event Status (RGM_DES) Register flag F_POR in device reference manual)
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27 in device reference manual)
- LVDHV5 monitors V_{DD} when application uses device in the $5.0 \text{ V} \pm 10\%$ range (refer to RGM Functional Event Status (RGM_FES) Register flag F_LVD45 in device reference manual)
- LVDLVCOR monitors power domain No. 1 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD1 in device reference manual)
- LVDLVBKP monitors power domain No. 0 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD0 in device reference manual)

Note: When enabled, power domain No. 2 is monitored through LVDLVBKP.

Figure 12. Low voltage detector vs reset



Note: [Figure 12: Low voltage detector vs reset](#) does not apply to LVDHV5 low voltage detector because LVDHV5 is automatically disabled during reset and it must be enabled by software again. Once the device is forced to reset by LVDHV5, the LVDHV5 is disabled and reset is

Figure 14. Fast external crystal oscillator (4 to 16 MHz) timing diagram

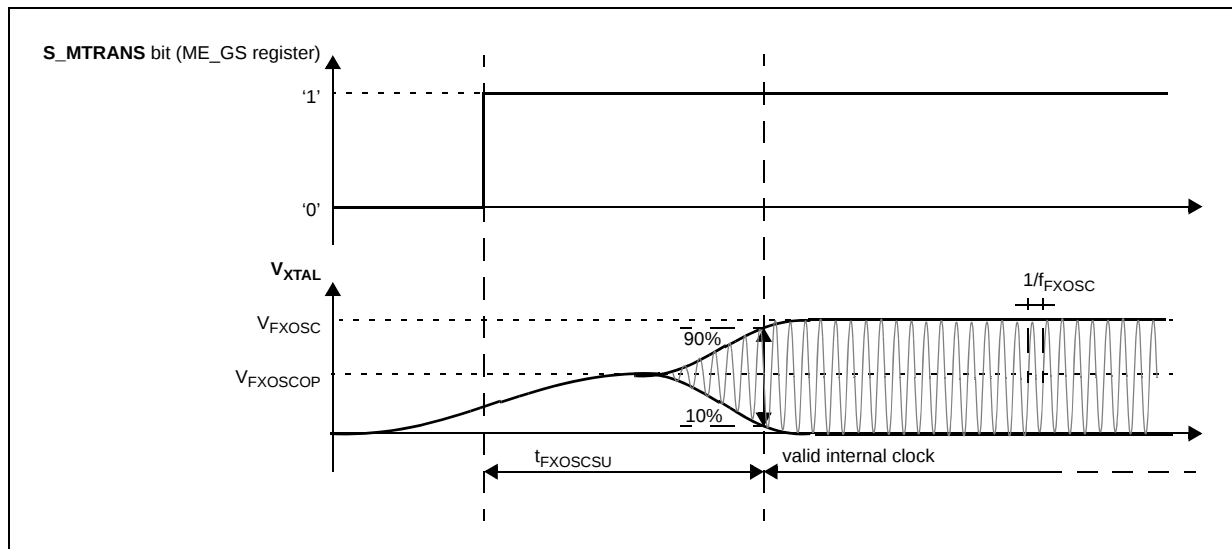


Table 38. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit
				Min	Typ	Max	
f _{FXOSC}	SR	—	Fast external crystal oscillator frequency	4.0	—	16.0	MHz
g _{mFXOSC}	CC	C	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	—	8.2	mA/V
	CC	P	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	—	7.4	
	CC	C	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	—	9.7	
	CC	C	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	—	9.2	
V _{FXOSC}	CC	T	Oscillation amplitude at EXTAL				V
			f _{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	1.3	—	—	
			f _{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	1.3	—	—	
V _{FXOSCOP}	CC	C	Oscillation operating point	—	0.95	—	V
I _{FXOSC} ⁽²⁾	CC	T	Fast external crystal oscillator consumption	—	2	3	mA
t _{FXOSCSU}	CC	T	Fast external crystal oscillator start-up time				ms
			f _{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	
			f _{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	

Figure 26. DSPI classic SPI timing – slave, CPHA = 1

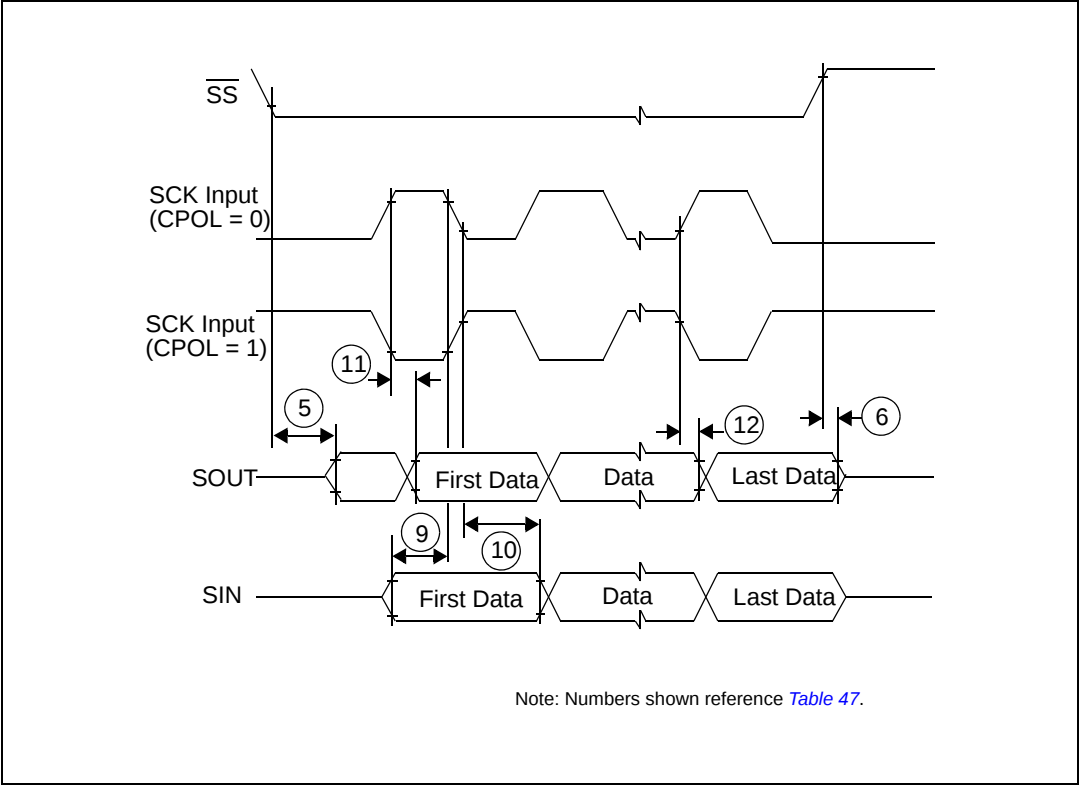


Figure 27. DSPI modified transfer format timing – master, CPHA = 0

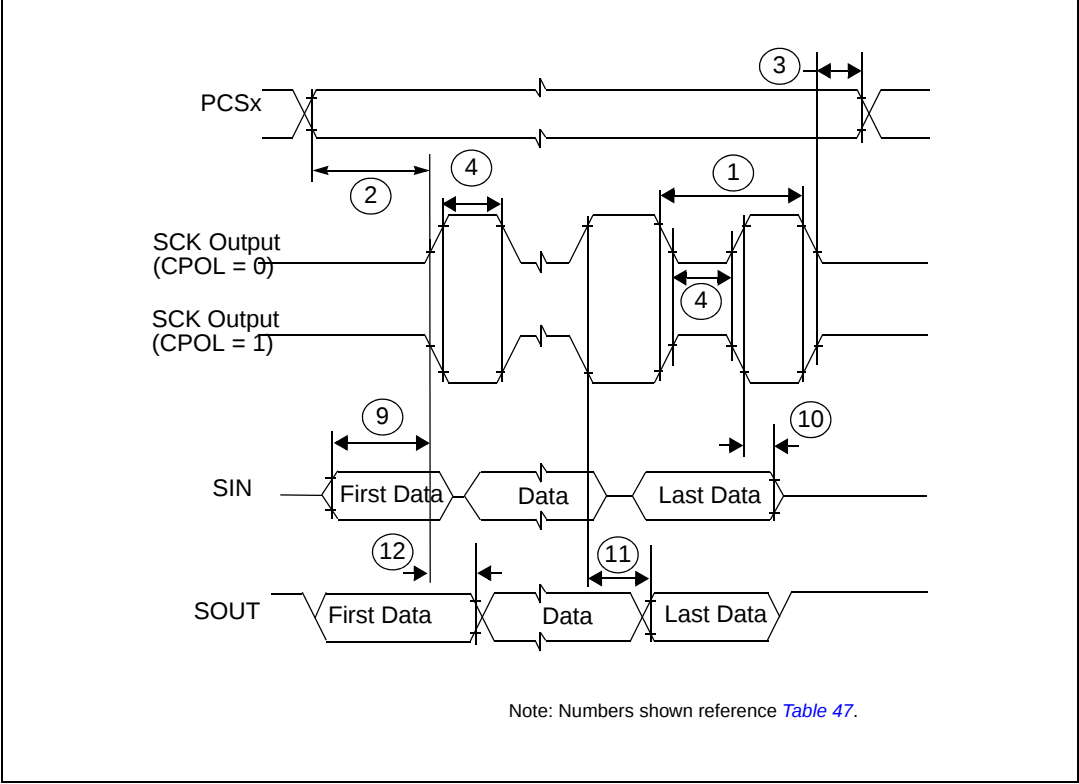
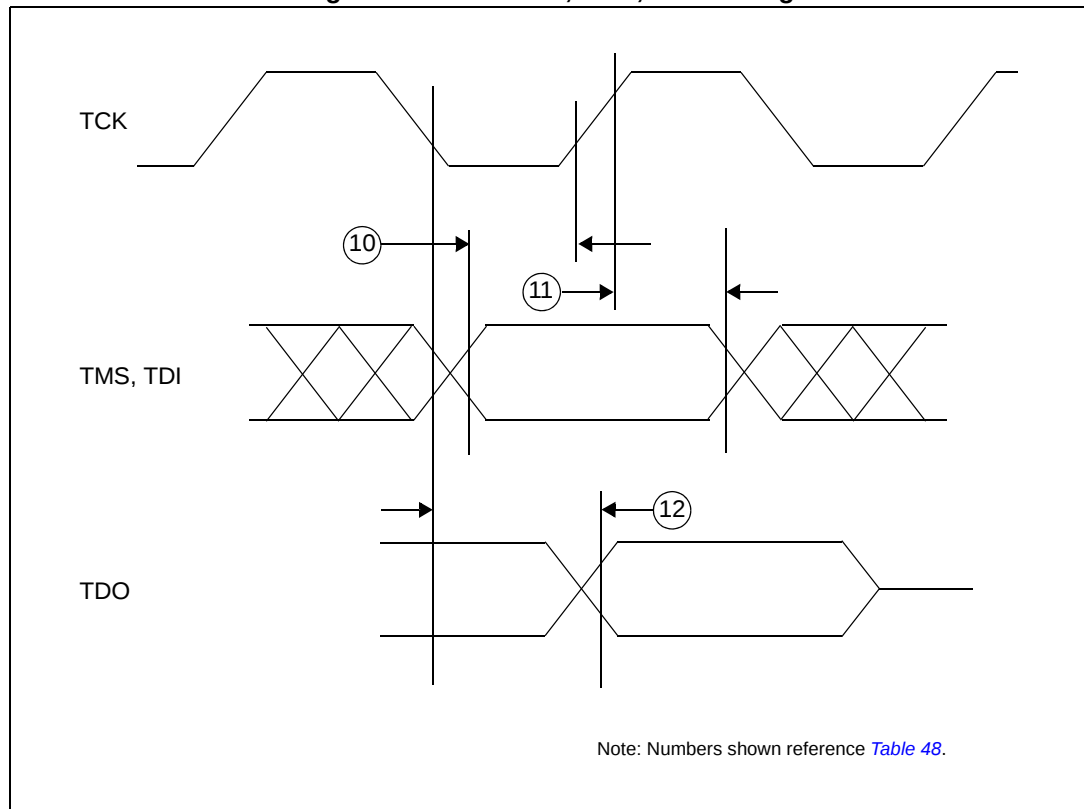


Table 48. Nexus characteristics (continued)

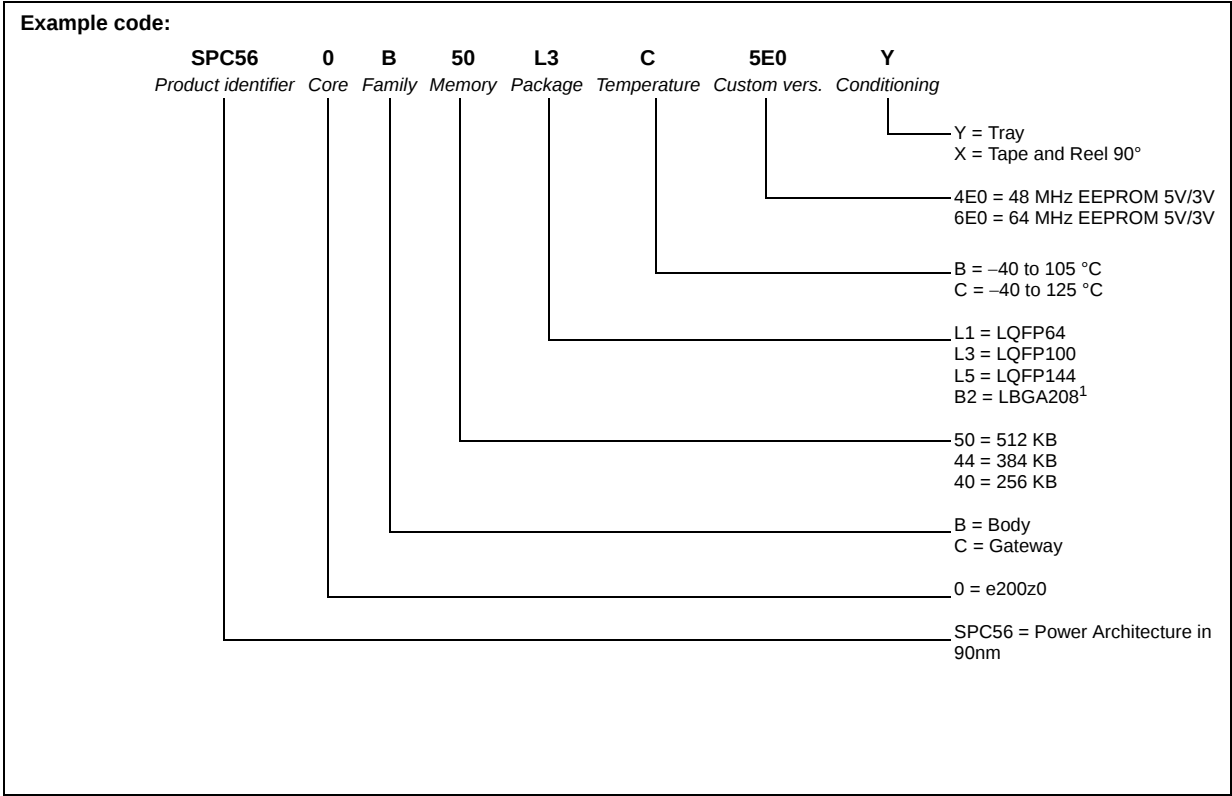
No.	Symbol	C	Parameter	Value			Unit
				Min	Typ	Max	
4	t_{MSEOV}	CC	D MCKO low to MSEO_b data valid	—	—	8	ns
5	t_{EVTOV}	CC	D MCKO low to EVTO data valid	—	—	8	ns
10	t_{NTDIS}	CC	D TDI data setup time	15	—	—	ns
	t_{NTMSS}	CC	D TMS data setup time	15	—	—	ns
11	t_{NTDIH}	CC	D TDI data hold time	5	—	—	ns
	t_{NTMSH}	CC	D TMS data hold time	5	—	—	ns
12	t_{TDOV}	CC	D TCK low to TDO data valid	35	—	—	ns
13	t_{TDOI}	CC	D TCK low to TDO data invalid	6	—	—	ns

Figure 32. Nexus TDI, TMS, TDO timing



5 Ordering information

Figure 38. Commercial product code structure



1. LBGA208 available only as development package for Nexus2+

Table 55. Document revision history (continued)

Date	Revision	Changes
06-Mar-2009	2 (continued)	Updated tables: – “I/O input DC electrical characteristics” – “I/O pull-up/pull-down DC electrical characteristics” – “SLOW configuration output buffer electrical characteristics” – “MEDIUM configuration output buffer electrical characteristics” – “FAST configuration output buffer electrical characteristics” Added “Output pin transition times” section Updated “I/O consumption” table Updated “Start-up reset requirements” figure Updated “Reset electrical characteristics” table “Voltage regulator electrical characteristics” section: – Amended description of LV_PLL “Voltage regulator capacitance connection” figure: – Exchanged position of symbols C_{DEC1} and C_{DEC2} Updated tables” – “Voltage regulator electrical characteristics” – “Low voltage monitor electrical characteristics” – “Low voltage power domain electrical characteristics” Added “Low voltage monitor vs reset” figure Updated “Flash memory electrical characteristics” section Added “Electromagnetic compatibility (EMC) characteristics” section Updated “Fast external crystal oscillator (4 to 16 MHz) electrical characteristics” section Updated “Slow external crystal oscillator (32 kHz) electrical characteristics” section Updated tables: – “FMPLL electrical characteristics” – “Fast internal RC oscillator (16 MHz) electrical characteristics” – “Slow internal RC oscillator (128 kHz) electrical characteristics” Added “On-chip peripherals” section Added “ADC input leakage current” table Updated “ADC conversion characteristics” table Updated “ECOPACK®” section Corrected inverted column headings for typical and minimum dimensions in “LQFP64 mechanical data” and “LQFP100 mechanical data” tables Added “Abbreviation” appendix
03-Jun-2009	3	Corrected “Commercial product code structure” figure