Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560c50l3b4e0x

1 Introduction

1.1 Document overview

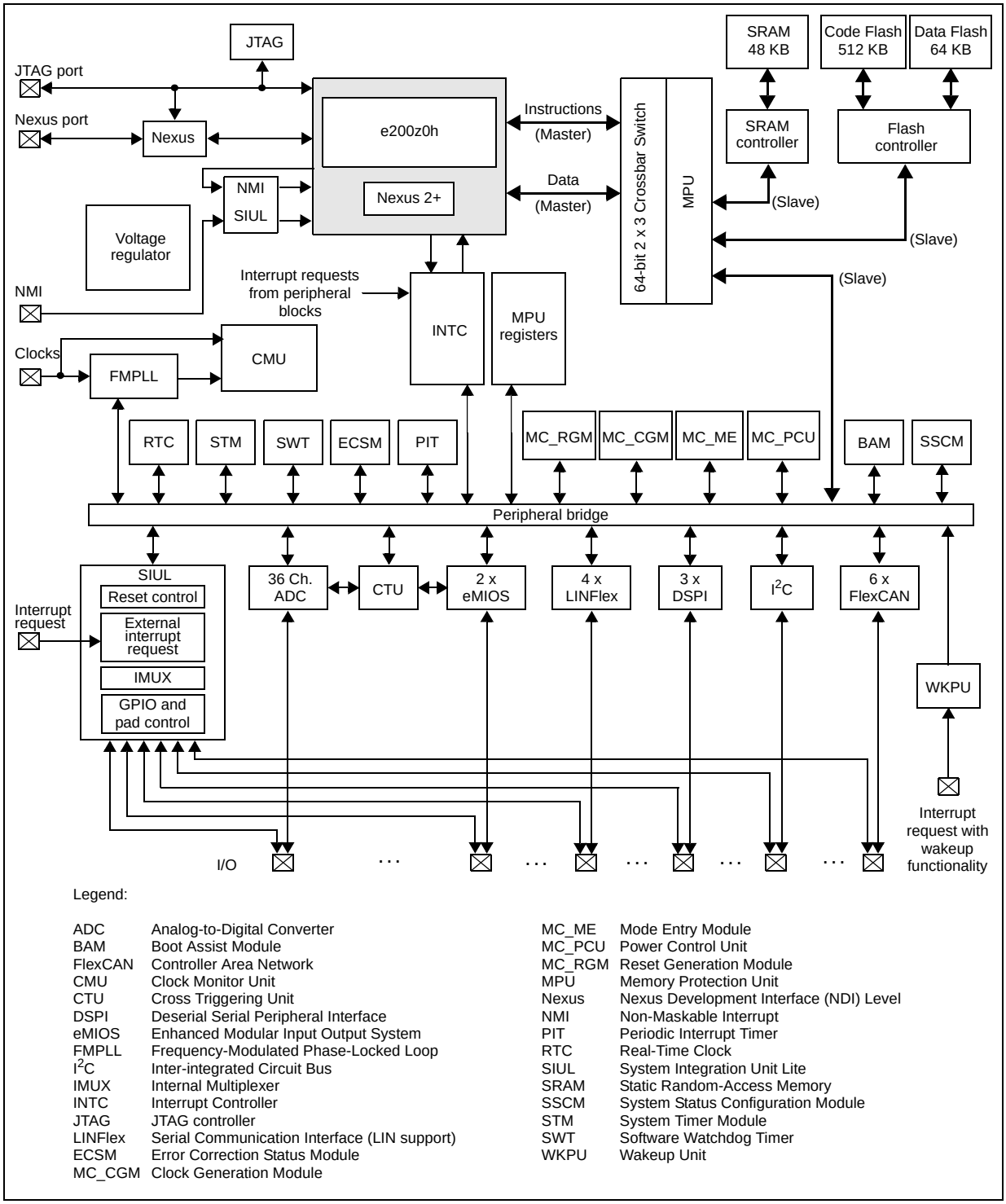
This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

1.2 Description

The SPC560B40x/50x and SPC560C40x/50x is a family of next generation microcontrollers built on the Power Architecture embedded category.

The SPC560B40x/50x and SPC560C40x/50x family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Figure 1. SPC560B40x/50x and SPC560C40x/50x block diagram



Legend:

ADC	Analog-to-Digital Converter
BAM	Boot Assist Module
FlexCAN	Controller Area Network
CMU	Clock Monitor Unit
CTU	Cross Triggering Unit
DSPI	Deserial Serial Peripheral Interface
eMIOS	Enhanced Modular Input Output System
FMPLL	Frequency-Modulated Phase-Locked Loop
I^2C	Inter-integrated Circuit Bus
IMUX	Internal Multiplexer
INTC	Interrupt Controller
JTAG	JTAG controller
LINFlex	Serial Communication Interface (LIN support)
ECSM	Error Correction Status Module
MC_CGM	Clock Generation Module
MC_ME	Mode Entry Module
MC_PCU	Power Control Unit
MC_RGM	Reset Generation Module
MPU	Memory Protection Unit
Nexus	Nexus Development Interface (NDI) Level
NMI	Non-Maskable Interrupt
PIT	Periodic Interrupt Timer
RTC	Real-Time Clock
SIUL	System Integration Unit Lite
SRAM	Static Random-Access Memory
SSCM	System Status Configuration Module
STM	System Timer Module
SWT	Software Watchdog Timer
WKPU	Wakeup Unit

Table 3 summarizes the functions of all blocks present in the SPC560B40x/50x and SPC560C40x/50x series of microcontrollers. Please note that the presence and number of blocks vary by device and package.

Table 3. SPC560B40x/50x and SPC560C40x/50x series block summary

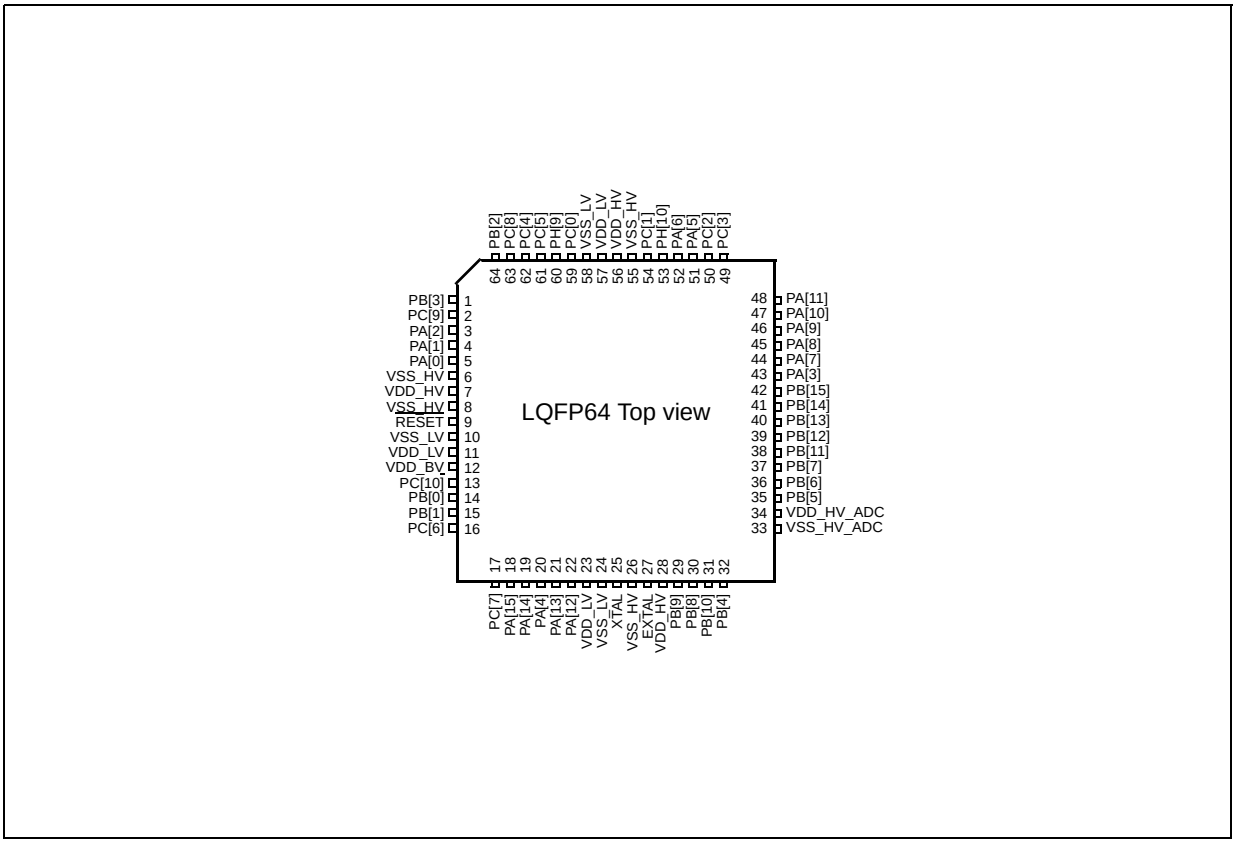
Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Error Correction Status Module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Inter-integrated circuit (I^2C™) bus	A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device

3 Package pinouts and signal descriptions

3.1 Package pinouts

The available LQFP pinouts and the LBGA208 ballmap are provided in the following figures. For pin signal descriptions, please refer to the device reference manual (RM0017).

Figure 2. LQFP 64-pin configuration(a)



a. All LQFP64 information is indicative and must be confirmed during silicon validation.

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PC[15]	PCR[47]	AF0 AF1 AF2 AF3	GPIO[47] E0UC[15] CS0_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O I/O —	M	Tristate	—	4	4	D3
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 —	GPIO[48] — — — GPI[4]	SIUL — — — ADC	I — — — I	I	Tristate	—	41	63	P12
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 —	GPIO[49] — — — GPI[5]	SIUL — — — ADC	I — — — I	I	Tristate	—	42	64	T12
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 —	GPIO[50] — — — GPI[6]	SIUL — — — ADC	I — — — I	I	Tristate	—	43	65	R12
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 —	GPIO[51] — — — GPI[7]	SIUL — — — ADC	I — — — I	I	Tristate	—	44	66	P13
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 —	GPIO[52] — — — GPI[8]	SIUL — — — ADC	I — — — I	I	Tristate	—	45	67	R13
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 —	GPIO[53] — — — GPI[9]	SIUL — — — ADC	I — — — I	I	Tristate	—	46	68	T13

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PG[0]	PCR[96]	AF0 AF1 AF2 AF3	GPIO[96] CAN5TX[11] E1UC[23] —	SIUL FlexCAN_5 eMIOS_1 —	I/O O I/O —	M	Tristate	—	—	98	E14
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — —	GPIO[97] — E1UC[24] — CAN5RX[11] EIRQ[14]	SIUL — eMIOS_1 — FlexCAN_5 SIUL	I/O — I/O — I I	S	Tristate	—	—	97	E13
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	8	E4
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] — — WKPU[17][4]	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	S	Tristate	—	—	7	E3
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	6	E1
PG[5]	PCR[101]	AF0 AF1 AF2 AF3 —	GPIO[101] E1UC[14] — — WKPU[18][4]	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	S	Tristate	—	—	5	E2
PG[6]	PCR[102]	AF0 AF1 AF2 AF3	GPIO[102] E1UC[15] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	30	M2

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PG[7]	PCR[103]	AF0 AF1 AF2 AF3	GPIO[103] E1UC[16] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	29	M1
PG[8]	PCR[104]	AF0 AF1 AF2 AF3 —	GPIO[104] E1UC[17] — CS0_2 EIRQ[15]	SIUL eMIOS_1 — DSPI_2 SIUL	I/O I/O — I/O I	S	Tristate	—	—	26	L2
PG[9]	PCR[105]	AF0 AF1 AF2 AF3	GPIO[105] E1UC[18] — SCK_2	SIUL eMIOS_1 — DSPI_2	I/O I/O — I/O	S	Tristate	—	—	25	L1
PG[10]	PCR[106]	AF0 AF1 AF2 AF3	GPIO[106] E0UC[24] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	—	114	D13
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	115	B12
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	92	K14
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	91	K16
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	—	110	B14

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PH[7]	PCR[119]	AF0 AF1 AF2 AF3	GPIO[119] E1UC[9] CS3_2 MA[1]	SIUL eMIOS_1 DSPI_2 ADC	I/O I/O O O	M	Tristate	—	—	137	C5
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC	I/O I/O O O	M	Tristate	—	—	138	A5
PH[9][9]	PCR[121]	AF0 AF1 AF2 AF3	GPIO[121] — TCK —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	60	88	127	B8
PH[10][9]	PCR[122]	AF0 AF1 AF2 AF3	GPIO[122] — TMS —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	53	81	120	B9

1. Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 → AF0; PCR.PA = 01 → AF1; PCR.PA = 10 → AF2; PCR.PA = 11 → AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".
2. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.
3. LBGA208 available only as development package for Nexus2+
4. All WKPU pins also support external interrupt capability. See wakeup unit chapter for further details.
5. NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.
6. "Not applicable" because these functions are available only while the device is booting. Refer to BAM chapter of the reference manual for details.
7. Value of PCR.IBE bit must be 0
8. Be aware that this pad is used on the SPC560B64L3 and SPC560B64L5 to provide VDD_HV_ADC and VSS_HV_ADC1. Therefore, you should be careful in ensuring compatibility between SPC560B40x/50x and SPC560C40x/50x and SPC560B64.
9. Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
   PC[0:1] are available as JTAG pins (TDI and TDO respectively).
   PH[9:10] are available as JTAG pins (TCK and TMS respectively).
   If the user configures these JTAG pins in GPIO mode the device is no longer compliant with IEEE 1149.1-2001.
10. The TDO pad has been moved into the STANDBY domain in order to allow low-power debug handshaking in STANDBY mode. However, no pull-resistor is active on the TDO pad while in STANDBY mode. At this time the pad is configured as an input. When no debugger is connected the TDO pad is floating causing additional current consumption. To avoid the extra consumption TDO must be connected. An external pull-up resistor in the range of 47–100 kΩ should be added between the TDO pin and VDD_HV. Only in case the TDO pin is used as application pin and a pull-up cannot be used then a pull-down resistor with the same value should be used between TDO pin and GND instead.

Table 12. Absolute maximum ratings (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	—	V_{DD}+0.3	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	64	
I_{CORELV}	SR	Low voltage static current sink through VDD_BV	—	—	150	mA
$T_{STORAGE}$	SR	Storage temperature	—	–55	150	°C

Note: Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

3.13 Recommended operating conditions

Table 13. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}(1)	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}(2)	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_BV}(3)	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V_{DD}	V_{DD}–0.1	V_{DD}+0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_ADC}(4)	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	3.0(5)	3.6	V
			Relative to V_{DD}	V_{DD}–0.1	V_{DD}+0.1	

Table 13. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS}–0.1	—	V
			Relative to V_{DD}	—	V_{DD}+0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up(6)	—	3.0(7)	250×10^3 (0.25 [V/µs])	V/s

1. 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair
2. 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.
3. 400 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).
4. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.
6. Guaranteed by device validation.
7. Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH}).

Table 14. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}(1)	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
V_{SS_LV}(3)	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_BV}(4)	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to V_{DD}	V_{DD}–0.1	V_{DD}+0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS}	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_ADC}(5)	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to V_{DD}	V_{DD}–0.1	V_{DD}+0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS}–0.1	—	V
			Relative to V_{DD}	—	V_{DD}+0.1	

3.15.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- *Table 17* provides weak pull figures. Both pull-up and pull-down resistances are supported.
- *Table 18* provides output driver characteristics for I/O pads when in SLOW configuration.
- *Table 19* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 20* provides output driver characteristics for I/O pads when in FAST configuration.

Table 17. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[2]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 18. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD}–0.8	—	—	

Table 21. Output pin transition times (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
t_{tr}	CC	D	Output transition time output pin[2] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).

3.15.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 22*.

Table 22. I/O supply segment

Package	Supply segment					
	1	2	3	4	5	6
LBGA208[1]	Equivalent to LQFP144 segment pad distribution				MCKO	MDOn/MSEO
LQFP144	pin20–pin49	pin51–pin99	pin100–pin122	pin 123–pin19	—	—
LQFP100	pin16–pin35	pin37–pin69	pin70–pin83	pin 84–pin15	—	—
LQFP64[2]	pin8–pin26	pin28–pin55	pin56–pin7	—	—	—

1. LBGA208 available only as development package for Nexus2+
2. All LQFP64 information is indicative and must be confirmed during silicon validation.

Table 23 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 26. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	—	
I_{DD_BV}	CC	D	In-rush average current on V_{DD_BV} during power-up(5)	—	—	—	300 (6)	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.
3. This value is acceptable to guarantee operation from 4.5 V to 5.5 V
4. External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.
5. In-rush average current is seen only for short time (maximum 20 µs) during power-up and on standby exit. It is dependant on the sum of the C_{REGn} capacitances.
6. The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

The $|\Delta_{VDD(STDBY)}|$ and dVDD(STDBY)/dt system requirement can be used to define the component used for the V_{DD} supply generation. The following two examples describe how to calculate capacitance size:

Example 1 No regulator (worst case)

The $|\Delta_{VDD(STDBY)}|$ parameter can be seen as the V_{DD} voltage drop through the ESR resistance of the regulator stability capacitor when the I_{DD_BV} current required to load V_{DD_LV} domain during the standby exit. It is thus possible to define the maximum equivalent resistance ESR_{STDBY}(MAX) of the total capacitance on the V_{DD} supply:

$ESR_{STDBY}(MAX) = |\Delta_{VDD(STDBY)}|/I_{DD\_BV}$ = (30 mV)/(300 mA) = 0.1Ω [d]

The dVDD(STDBY)/dt parameter can be seen as the V_{DD} voltage drop at the capacitance pin (excluding ESR drop) while providing the I_{DD_BV} supply required to load V_{DD_LV} domain during the standby exit. It is thus possible to define the minimum equivalent capacitance C_{STDBY}(MIN) of the total capacitance on the V_{DD} supply:

$C_{STDBY}(MIN) = I_{DD\_BV}/dVDD(STDBY)/dt$ = (300 mA)/(15 mV/µs) = 20 µF

This configuration is a worst case, with the assumption no regulator is available.

Example 2 Simplified regulator

The regulator should be able to provide significant amount of the current during the standby exit process. For example, in case of an ideal voltage regulator providing 200 mA current, it is possible to recalculate the equivalent ESR_{STDBY}(MAX) and C_{STDBY}(MIN) as follows:

d. Based on typical time for standby exit sequence of 20 µs, ESR(MIN) can actually be considered at ~50 kHz.

3.19.3 Start-up/Switch-off timings

Table 33. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$T_{FLARSTEXIT}$	CC	T	Delay for Flash module to exit reset mode	Code Flash	—	—	125	µs
		T		Data Flash	—	—	125	
$T_{FLALPEXIT}$	CC	T	Delay for Flash module to exit low-power mode	Code Flash	—	—	0.5	
		T		Data Flash	—	—	0.5	
$T_{FLAPDEXIT}$	CC	T	Delay for Flash module to exit power-down mode	Code Flash	—	—	30	
		T		Data Flash	—	—	30	
$T_{FLALPENTRY}$	CC	T	Delay for Flash module to enter low-power mode	Code Flash	—	—	0.5	
		T		Data Flash	—	—	0.5	
$T_{FLAPDENTRY}$	CC	T	Delay for Flash module to enter power-down mode	Code Flash	—	—	1.5	
		T		Data Flash	—	—	1.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.20 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.20.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations: The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers...)
- Prequalification trials: Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note *Software Techniques For Improving Microcontroller EMC Performance* (AN1015)).

Table 42. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
t_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	V_{DD} = 5.0 V ± 10%	—	1.1	2.0	µs
$\Delta_{FIRCPRE}$	CC	T	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C	–1	—	+1	%
$\Delta_{FIRCTRIM}$	CC	T	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6		%
$\Delta_{FIRCVAR}$	CC	P	Fast internal RC oscillator variation in over temperature and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration	—	–5	—	+5	%

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

3.25 Slow internal RC oscillator (128 kHz) electrical characteristics

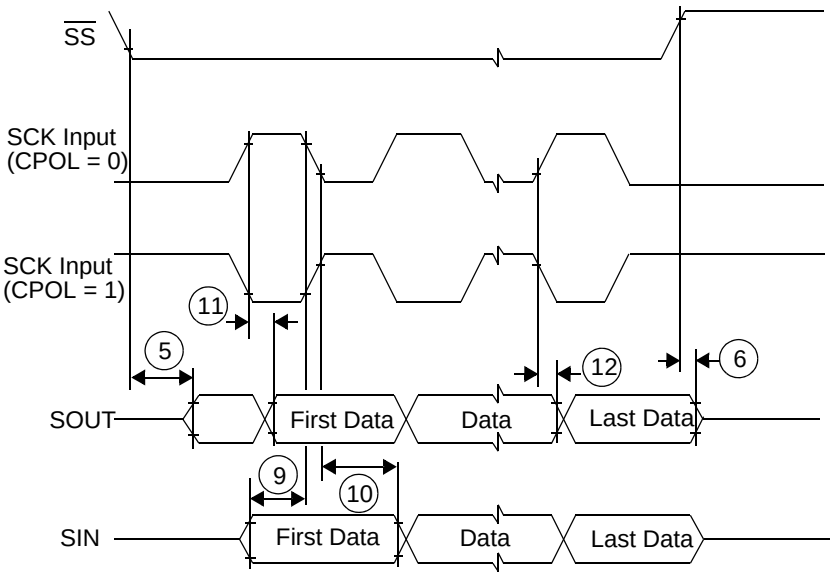
The device provides a 128 kHz slow internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 43. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		—	100	—	150	
I_{SIRC}[2]	CC	C	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA
t_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	+2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at T_A = 55 °C in high frequency configuration	High frequency configuration	–10	—	+10	%

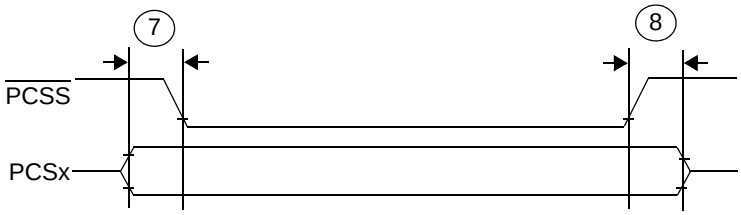
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

Figure 30. DSPI modified transfer format timing – slave, CPHA = 1



Note: Numbers shown reference *Table 47*.

Figure 31. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing



Note: Numbers shown reference *Table 47*.

3.27.3 Nexus characteristics

Table 48. Nexus characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{TCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
3	t_{MDOV}	CC	D	MCKO low to MDO data valid	—	—	8	ns

Table 51. LQFP100 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

4.2.3 LQFP144

Figure 36. LQFP144 package mechanical drawing

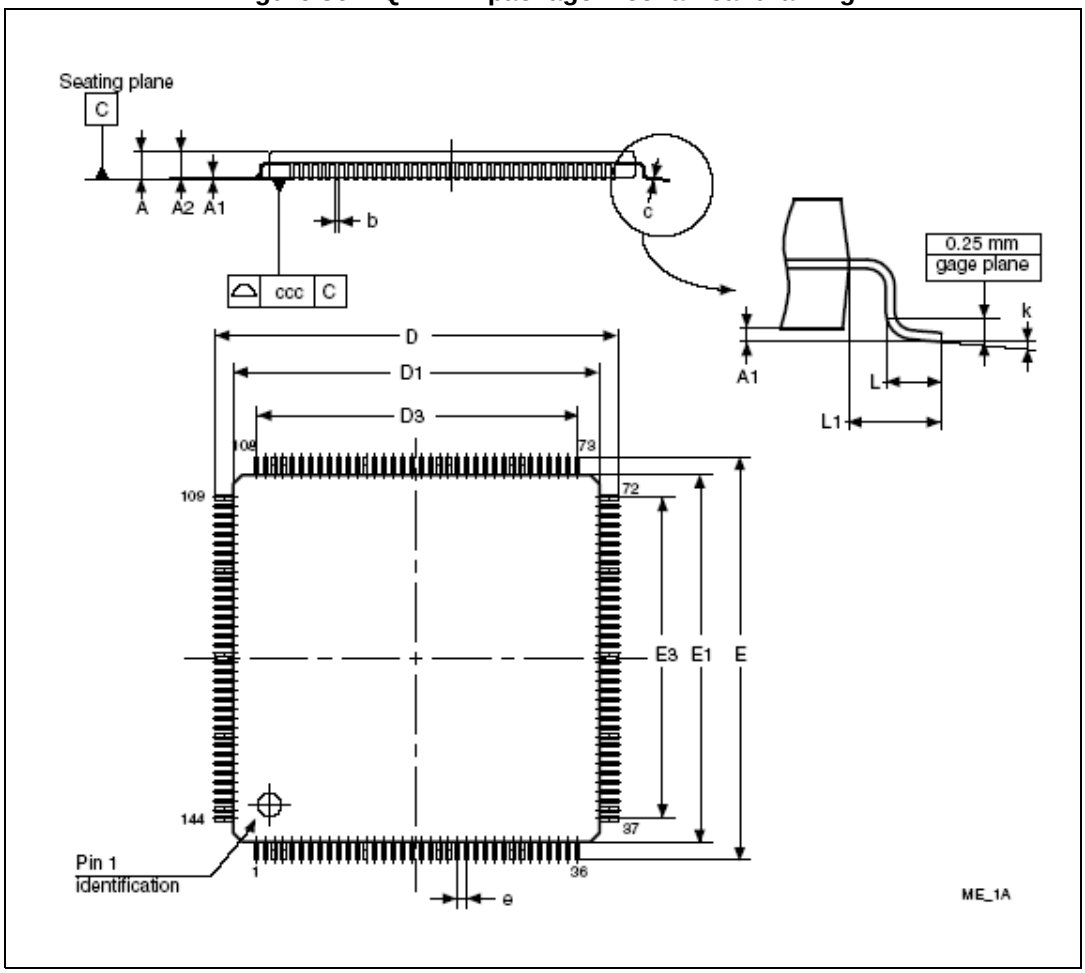


Table 55. Document revision history (continued)

Date	Revision	Changes
20-Jan-2010	5	Table: “Absolute maximum ratings” – V_{DD_BV}, V_{DD_ADC}, V_{IN}: changed max value Table: ”Recommended operating conditions (3.3 V)” – TV_{DD}: deleted min value Table: “Reset electrical characteristics“ – Changed footnotes 2 and 5 Table: “Voltage regulator electrical characteristics“ – C_{REGn}: changed max value – C_{DEC1}: split into 2 rows – Updated voltage values in footnote 3 Table: “Low voltage monitor electrical characteristics“ – Updated column Conditions – $V_{LVDLVCORL}$, $V_{LVDLVBKPL}$: changed min/max value Table: “Program and erase specifications“ – $T_{dwprogram}$: added initial max value Table: “Flash module life“ – Retention: changed min value for blocks with 100K P/E cycles Table: “Flash power supply DC electrical characteristics“ – I_{FREAD}, I_{FMOD}: added typ value – Added a footnote Added Section: “ NVUSRO[WATCHDOG_EN] field description“ Section 4.18: “ADC electrical characteristics“ has been moved up in hierarchy (it was Section 4.18.5). Table: “ ADC conversion characteristics“ – R_{AD}: changed initial max value Table: “On-chip peripherals current consumption“ – Removed min/max from the heading – Changed unit of measurement and consequently rounded the values
15-Mar-2010	6	Internal release.

Table 55. Document revision history (continued)

Date	Revision	Changes
01-Oct-2011	9	Formatting and minor editorial changes throughout Harmonized oscillator nomenclature Device summary table: removed 384 KB code flash device versions Device comparison table: changed temperature value in footnote 2 from 105 °C to 125 °C; removed 384 KB code flash device versions LQFP 64-pin configuration: renamed pin 6 from VPP_TEST to VSS_HV Removed “Pin Muxing” section; added sections “Pad configuration during reset phases”, “Voltage supply pins”, “Pad types”, “System pins,” “Functional ports”, and “Nexus 2+ pins” Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality; updated footnote describing default value of ‘1’ in field descriptions NVUSRO[PAD3V5V] and NVUSRO[OSCILLATOR_MARGIN] Added section “NVUSRO[WATCHDOG_EN] field description” Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V): updated conditions for ambient and junction temperature characteristics I/O input DC electrical characteristics: updated I_{LKG} characteristics Section “I/O pad current specification”: removed content referencing the I_{DYNSEG} maximum value I/O consumption: replaced instances of “Root medium square” with “Root mean square” I/O weight: replaced instances of bit “SRE” with “SRC”; added pads PH[9] and PH[10]; added supply segments; removed weight values in 64-pin LQFP for pads that do not exist in that package Reset electrical characteristics: updated parameter classification for $\|I_{WPU}\|$ Updated Voltage regulator electrical characteristics Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$; replaced “LVD_DIGBKP” with “LVDLVBKP” in note Updated section “Power consumption” Fast external crystal oscillator (4 to 16 MHz) electrical characteristics: updated parameter classification for $V_{FXOSCOP}$ Crystal oscillator and resonator connection scheme: added footnote about possibility of adding a series resistor Slow external crystal oscillator (32 kHz) electrical characteristics: updated footnote 1 FMPLL electrical characteristics: added short term jitter characteristics; inserted “—” in empty min value cell of t_{lock} row Section “Input impedance and ADC accuracy”: changed “V_A/V_{A2}” to “V_{A2}/V_A” in Equation 11 ADC input leakage current: updated I_{LKG} characteristics ADC conversion characteristics: updated symbols On-chip peripherals current consumption: changed “supply current on “$V_{DD\_HV\_ADC}$” to “supply current on” V_{DD_HV}” in $I_{DD\_HV(FLASH)}$ row; updated $I_{DD\_HV(PLL)}$ value—was 3 * f_{periph}, is 30 * f_{periph}; updated footnotes DSPI characteristics: added rows t_{PCSC} and t_{PASC} Added DSPI PCS strobe (PCSS) timing diagram Updated order codes.
17-Jan-2013	10	Internal review.