Infineon Technologies - MB96F636RBPMC-GSE1 Datasheet

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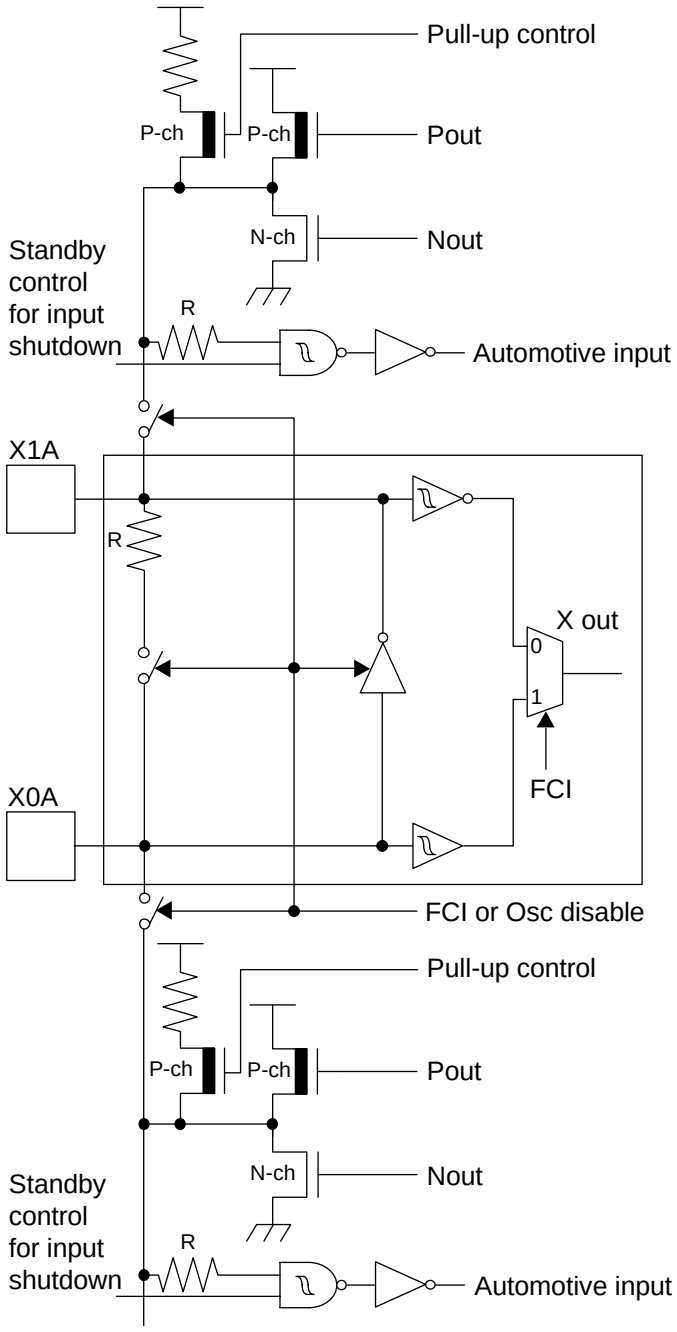
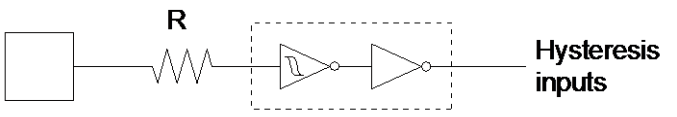
What is "Embedded - Microcontrollers"?

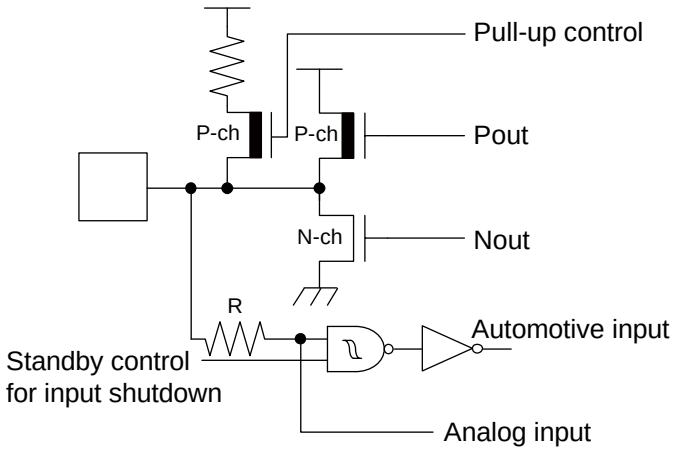
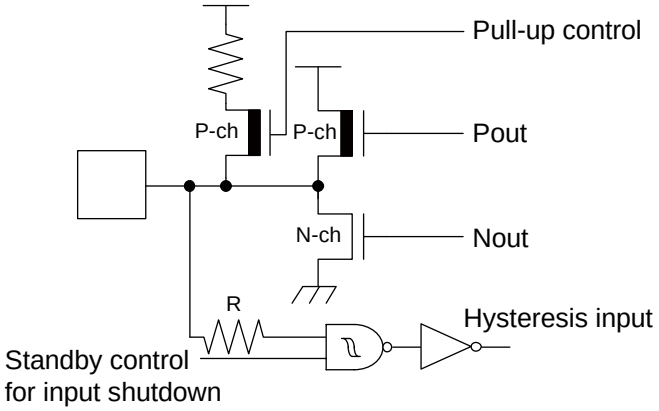
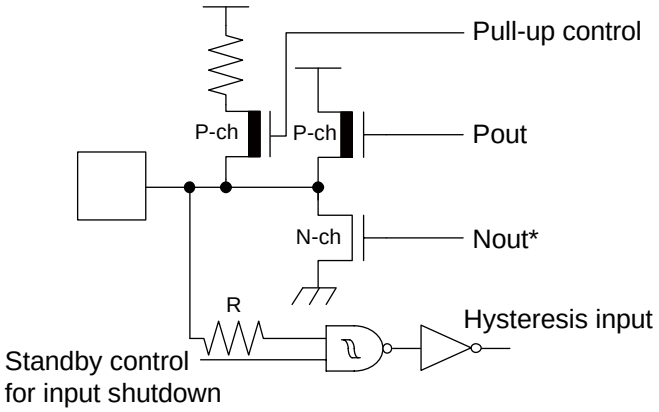
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 21x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f636rbpmc-gse1

Contents

Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: • Feedback resistor = approx. 5.0MΩ • GPIO functionality selectable (CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA), Automotive input with input shutdown function and programmable pull-up resistor)
C		CMOS hysteresis input pin

Type	Circuit	Remarks
K		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor • Analog input
M		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor
N		• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor *: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage.

9. User ROM Memory Map For Flash Devices

CPU mode address	Flash memory mode address	MB96F633 Flash size 64.5KB + 32KB	MB96F635 Flash size 128.5KB + 32KB	MB96F636 Flash size 256.5KB + 32KB	MB96F637 Flash size 384.5KB + 32KB	
$FF:FFFF_H$ $FF:0000_H$	$3F:FFFF_H$ $3F:0000_H$	SA39 - 64KB	SA39 - 64KB	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A
$FE:FFFF_H$ $FE:0000_H$	$3E:FFFF_H$ $3E:0000_H$	Reserved	SA38 - 64KB	SA38 - 64KB	SA38 - 64KB	
$FD:FFFF_H$ $FD:0000_H$	$3D:FFFF_H$ $3D:0000_H$		Reserved	SA37 - 64KB	SA37 - 64KB	
$FC:FFFF_H$ $FC:0000_H$	$3C:FFFF_H$ $3C:0000_H$			SA36 - 64KB	SA36 - 64KB	
$FB:FFFF_H$ $FB:0000_H$	$3B:FFFF_H$ $3B:0000_H$			Reserved	SA35 - 64KB	
$FA:FFFF_H$ $FA:0000_H$	$3A:FFFF_H$ $3A:0000_H$				SA34 - 64KB	
$F9:FFFF_H$ $DF:A000_H$					Reserved	
$DF:9FFF_H$ $DF:8000_H$	$1F:9FFF_H$ $1F:8000_H$	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	Bank B of Flash A
$DF:7FFF_H$ $DF:6000_H$	$1F:7FFF_H$ $1F:6000_H$	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB	
$DF:5FFF_H$ $DF:4000_H$	$1F:5FFF_H$ $1F:4000_H$	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB	
$DF:3FFF_H$ $DF:2000_H$	$1F:3FFF_H$ $1F:2000_H$	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB	
$DF:1FFF_H$ $DF:0000_H$	$1F:1FFF_H$ $1F:0000_H$	SAS - 512B*	SAS - 512B*	SAS - 512B*	SAS - 512B*	Bank A of Flash A
$DE:FFFF_H$ $DE:0000_H$		Reserved	Reserved	Reserved	Reserved	

*: Physical address area of SAS-512B is from $DF:0000_H$ to $DF:01FF_H$.
Others (from $DF:0200_H$ to $DF:1FFF_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address $DF:0000_H$ -$DF:01FF_H$.
SAS can not be used for E^2PROM emulation.

11. Interrupt Vector Table

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	$3FC_H$	CALLV0	No	-	CALLV instruction
1	$3F8_H$	CALLV1	No	-	CALLV instruction
2	$3F4_H$	CALLV2	No	-	CALLV instruction
3	$3F0_H$	CALLV3	No	-	CALLV instruction
4	$3EC_H$	CALLV4	No	-	CALLV instruction
5	$3E8_H$	CALLV5	No	-	CALLV instruction
6	$3E4_H$	CALLV6	No	-	CALLV instruction
7	$3E0_H$	CALLV7	No	-	CALLV instruction
8	$3DC_H$	RESET	No	-	Reset vector
9	$3D8_H$	INT9	No	-	INT9 instruction
10	$3D4_H$	EXCEPTION	No	-	Undefined instruction execution
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Clock Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	LVDI	No	16	Low Voltage Detector
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	EXTINT1	Yes	18	External Interrupt 1
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	EXTINT5	Yes	22	External Interrupt 5
23	$3A0_H$	EXTINT6	Yes	23	External Interrupt 6
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	EXTINT8	Yes	25	External Interrupt 8
26	394_H	EXTINT9	Yes	26	External Interrupt 9
27	390_H	EXTINT10	Yes	27	External Interrupt 10
28	$38C_H$	EXTINT11	Yes	28	External Interrupt 11
29	388_H	EXTINT12	Yes	29	External Interrupt 12
30	384_H	EXTINT13	Yes	30	External Interrupt 13
31	380_H	-	-	31	Reserved
32	$37C_H$	EXTINT15	Yes	32	External Interrupt 15
33	378_H	CAN0	No	33	CAN Controller 0
34	374_H	-	-	34	Reserved
35	370_H	-	-	35	Reserved
36	$36C_H$	-	-	36	Reserved
37	368_H	-	-	37	Reserved
38	364_H	PPG0	Yes	38	Programmable Pulse Generator 0
39	360_H	PPG1	Yes	39	Programmable Pulse Generator 1

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
124	20CH	-	-	124	Reserved
125	208H	-	-	125	Reserved
126	204H	-	-	126	Reserved
127	200H	-	-	127	Reserved
128	1FCH	-	-	128	Reserved
129	1F8H	-	-	129	Reserved
130	1F4H	-	-	130	Reserved
131	1F0H	-	-	131	Reserved
132	1ECH	-	-	132	Reserved
133	1E8H	FLASHA	Yes	133	Flash memory A interrupt
134	1E4H	-	-	134	Reserved
135	1E0H	-	-	135	Reserved
136	1DCH	-	-	136	Reserved
137	1D8H	QPRC0	Yes	137	Quadrature Position/Revolution counter 0
138	1D4H	QPRC1	Yes	138	Quadrature Position/Revolution counter 1
139	1D0H	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	1CCH	-	-	140	Reserved
141	1C8H	-	-	141	Reserved
142	1C4H	-	-	142	Reserved
143	1C0H	-	-	143	Reserved

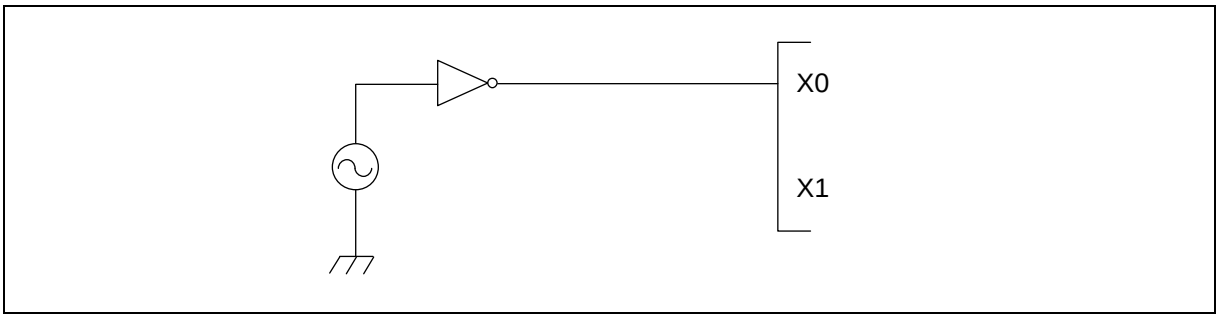
13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration.

See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

13.3.1 Single phase external clock for Main oscillator

When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open.
And supply 1.8V power to the external clock.



13.3.2 Single phase external clock for Sub oscillator

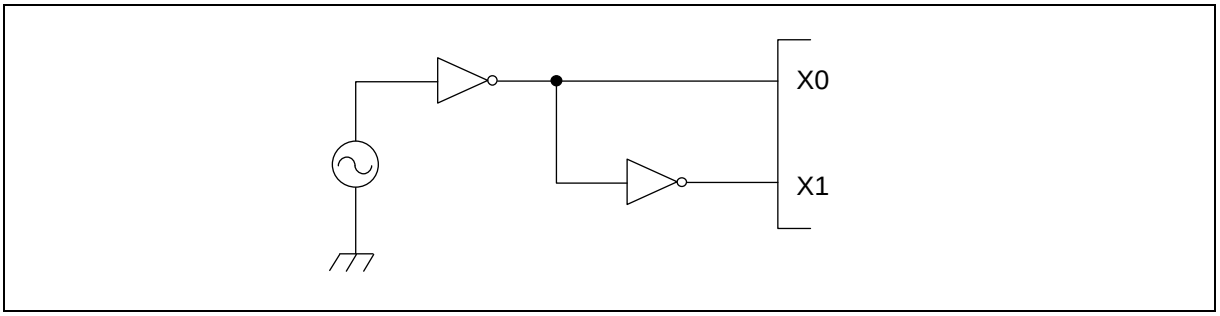
When using a single phase external clock for the Sub oscillator, “External clock mode” must be selected and

X0A/P04_0 pin must be driven. X1A/P04_1 pin can be configured as GPIO.

13.3.3 Opposite phase external clock

When using an opposite phase external clock, X1 (X1A) pins must be supplied with a clock signal which has

the opposite phase to the X0 (X0A) pins. Supply level on X0 and X1 pins must be 1.8V.



13.4 Notes on PLL clock mode operation

If the microcontroller is operated with PLL clock mode and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.5 Power supply pins (V_{cc}/V_{ss})

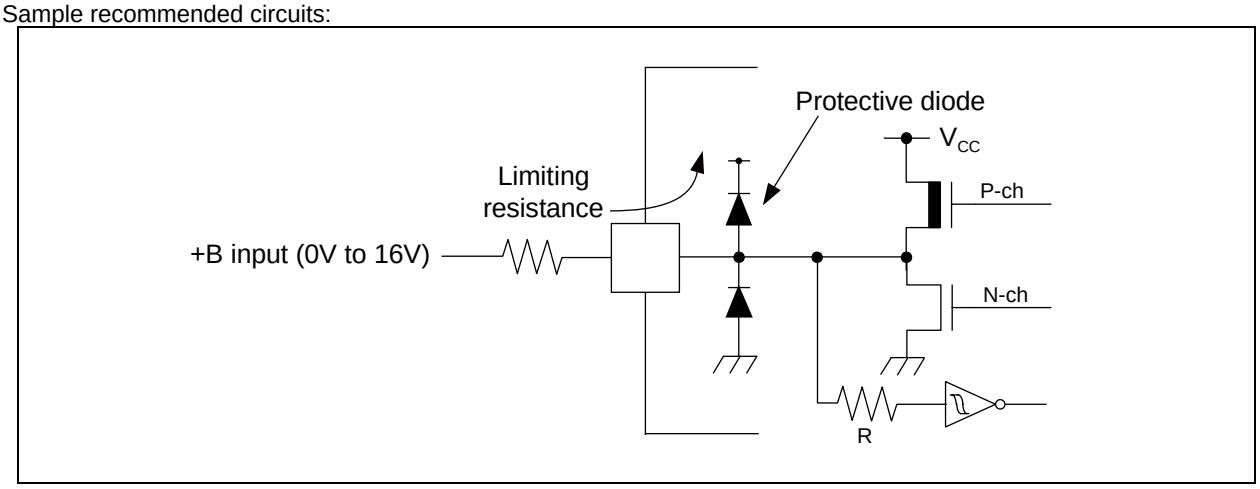
It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{cc} and V_{ss} pins must be connected to the device from the power supply with lowest possible impedance.

The smoothing capacitor at V_{cc} pin must use the one of a capacity value that is larger than C_s.

Besides this, as a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1μF between V_{cc} and V_{ss} pins as close as possible to V_{cc} and V_{ss} pins.

- The DEBUG I/F pin has only a protective diode against V_{SS}. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.
- Sample recommended circuits:



*5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
I_A is the analog current consumption into AV_{CC}.

*6: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*7: Write/erase to a large sector in flash memory is warranted with TA ≤ + 105°C.

WARNING
Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.3 DC Characteristics

14.3.1 Current Rating

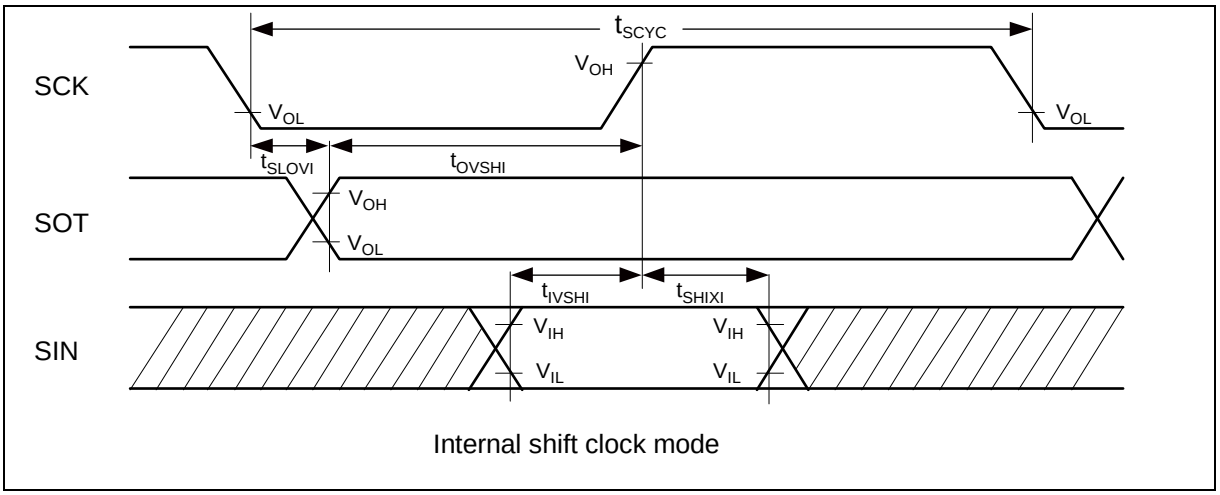
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes[*1]	I_{CCPLL}	Vcc	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz Flash 0 wait (CLKRC and CLKSC stopped)	-	27	-	mA	T_A = +25°C
				-	-	37	mA	T_A = +105°C
				-	-	38.5	mA	T_A = +125°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait (CLKPLL, CLKSC and CLKRC stopped)	-	3.5	-	mA	T_A = +25°C
				-	-	8	mA	T_A = +105°C
				-	-	9.5	mA	T_A = +125°C
	I_{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	1.8	-	mA	T_A = +25°C
				-	-	6	mA	T_A = +105°C
				-	-	7.5	mA	T_A = +125°C
	I_{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	0.16	-	mA	T_A = +25°C
				-	-	3.5	mA	T_A = +105°C
				-	-	5	mA	T_A = +125°C
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz Flash 0 wait (CLKMC, CLKPLL and CLKRC stopped)	-	0.1	-	mA	T_A = +25°C
				-	-	3.3	mA	T_A = +105°C
				-	-	4.8	mA	T_A = +125°C

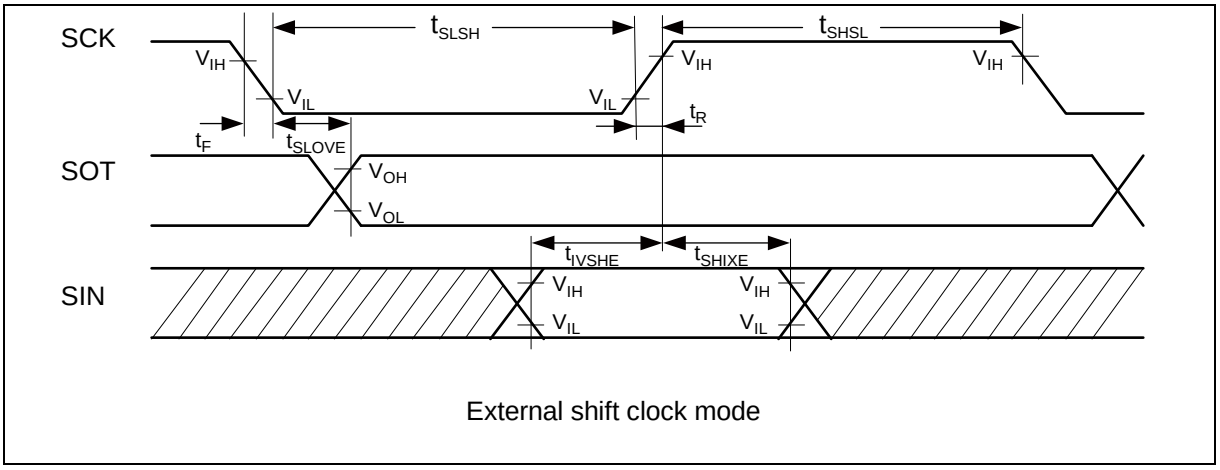
14.3.2 Pin Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port inputs Pnn_m	-	V_{CC} × 0.7	-	V_{CC} + 0.3	V	CMOS Hysteresis input
			-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	AUTOMOTIVE Hysteresis input
	V_{IHX0S}	X0	External clock in "Fast Clock Input mode"	VD × 0.8	-	VD	V	VD=1.8V±0.15V
	V_{IHX0AS}	X0A	External clock in "Oscillation mode"	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHD}	DEBUG I/F	-	2.0	-	V_{CC} + 0.3	V	TTL Input
"L" level input voltage	V_{IL}	Port inputs Pnn_m	-	V_{SS} - 0.3	-	V_{CC} × 0.3	V	CMOS Hysteresis input
			-	V_{SS} - 0.3	-	V_{CC} × 0.5	V	AUTOMOTIVE Hysteresis input
	V_{ILX0S}	X0	External clock in "Fast Clock Input mode"	V_{SS}	-	VD × 0.2	V	VD=1.8V±0.15V
	V_{ILX0AS}	X0A	External clock in "Oscillation mode"	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	CMOS Hysteresis input
	V_{ILM}	MD	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	CMOS Hysteresis input
	V_{ILD}	DEBUG I/F	-	V_{SS} - 0.3	-	0.8	V	TTL Input
"H" level output voltage	V_{OH4}	4mA type	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -4mA 2.7V ≤ V_{CC} < 4.5V I_{OH} = -1.5mA	V_{CC} - 0.5	-	V_{CC}	V	
	V_{OH3}	3mA type	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -3mA 2.7V ≤ V_{CC} < 4.5V I_{OH} = -1.5mA	V_{CC} - 0.5	-	V_{CC}	V	
"L" level output voltage	V_{OL4}	4mA type	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +4mA 2.7V ≤ V_{CC} < 4.5V I_{OL} = +1.7mA	-	-	0.4	V	
	V_{OL3}	3mA type	2.7V ≤ V_{CC} < 5.5V I_{OL} = +3mA	-	-	0.4	V	
	V_{OLD}	DEBUG I/F	V_{CC} = 2.7V I_{OL} = +25mA	0	-	0.25	V	



Internal shift clock mode



External shift clock mode

14.5 A/D Converter

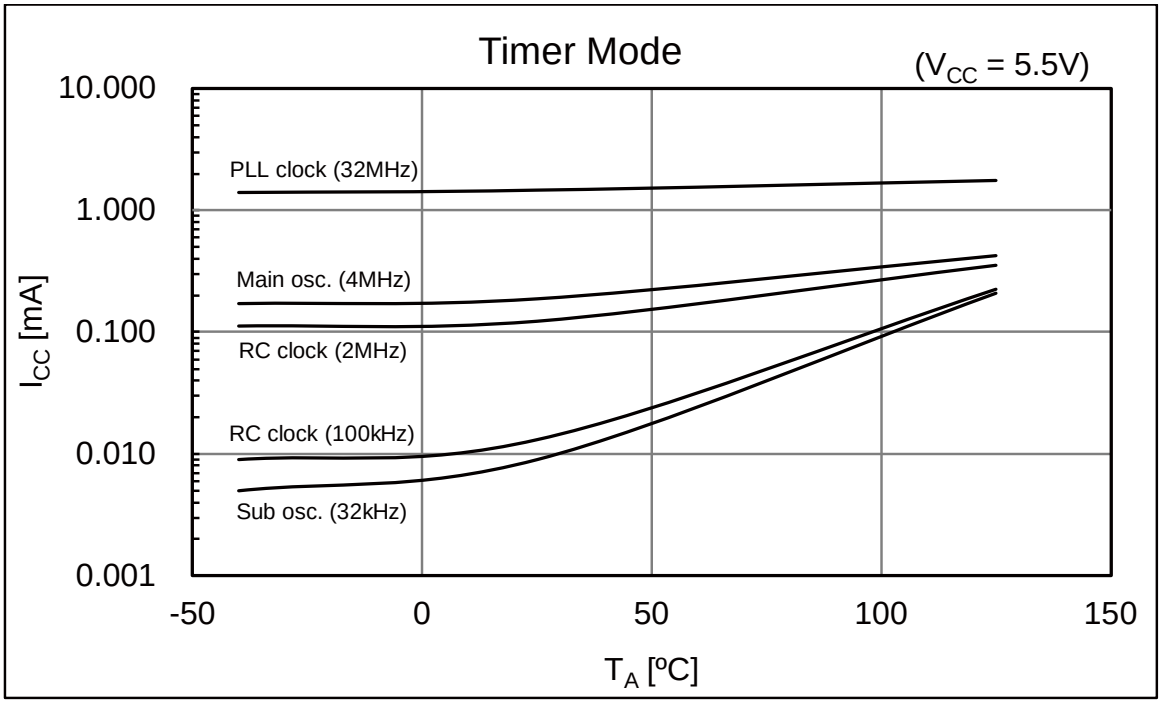
14.5.1 Electrical Characteristics for the A/D Converter

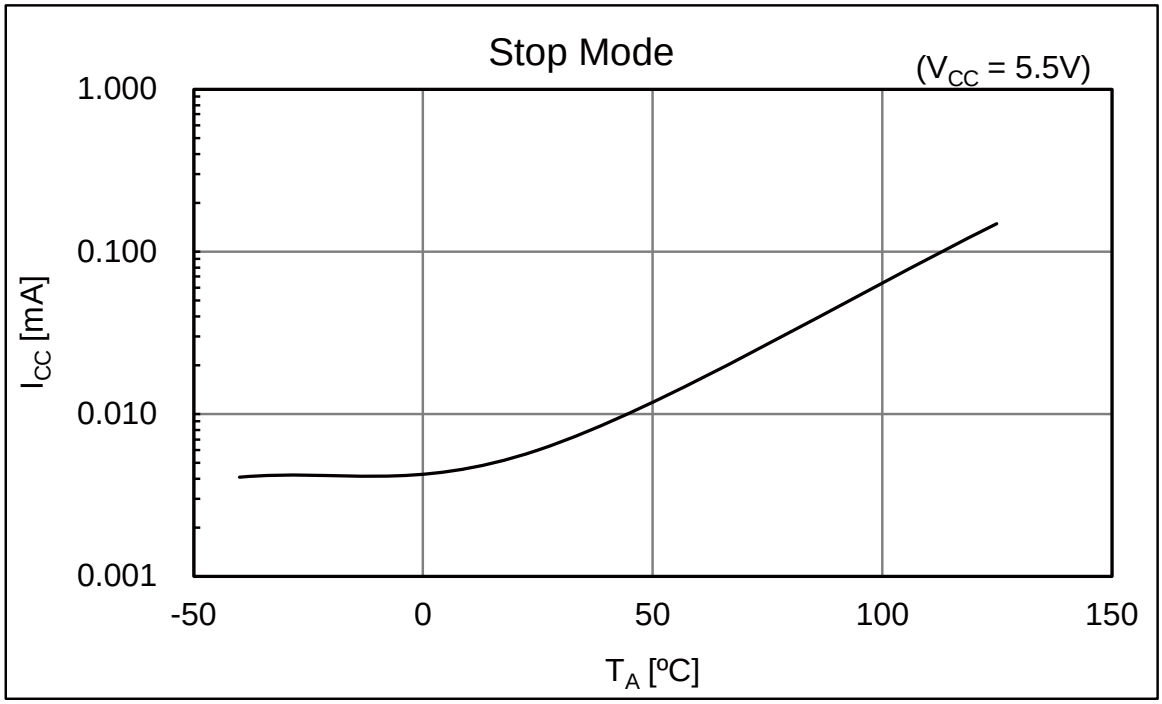
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	Typ - 20	AV_{SS} +0.5LSB	Typ + 20	mV	
Full scale transition voltage	V_{FST}	ANn	Typ - 20	AVRH - 1.5LSB	Typ + 20	mV	
Compare time*	-	-	1.0	-	5.0	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.2	-	8.0	µs	2.7V ≤ AV_{CC} < 4.5V
Sampling time*	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	2.7V ≤ AV_{CC} < 4.5V
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	µA	A/D Converter not operated
Reference power supply current (between AVRH and AV_{SS})	I_R	AVRH	-	520	810	µA	A/D Converter active
	I_{RH}		-	-	1.0	µA	A/D Converter not operated
Analog input capacity	C_{VIN}	ANn	-	-	15.9	pF	
Analog impedance	R_{VIN}	ANn	-	-	2050	Ω	4.5V ≤ AV_{CC} ≤ 5.5V
			-	-	3600	Ω	2.7V ≤ AV_{CC} < 4.5V
Analog port input current (during conversion)	I_{AIN}	ANn	- 0.3	-	+ 0.3	µA	AV_{SS} < V_{AIN} < AV_{CC}, AVRH
Analog input voltage	V_{AIN}	ANn	AV_{SS}	-	AVRH	V	
Reference voltage range	-	AVRH	AV_{CC} - 0.1	-	AV_{CC}	V	
Variation between channels	-	ANn	-	-	4.0	LSB	

*: Time for each channel.

■MB96F637


Timer Mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
I_{CC} [mA]
PLL clock (32MHz)
Main osc. (4MHz)
RC clock (2MHz)
RC clock (100kHz)
Sub osc. (32kHz)
-50
0
50
100
150
T_A [ºC]


Stop Mode
(V_{CC} = 5.5V)
1.000
0.100
0.010
0.001
I_{CC} [mA]
-50
0
50
100
150
T_A [ºC]

■Used setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

16. Ordering Information

MCU with CAN controller

Part number	Flash memory	Package*
MB96F633RBPMC-GSE1	Flash A (96.5KB)	80-pin plastic LQFP (FPT-80P-M21)
MB96F633RBPMC-GSE2		
MB96F635RBPMC-GSE1	Flash A (160.5KB)	80-pin plastic LQFP (FPT-80P-M21)
MB96F635RBPMC-GSE2		
MB96F636RBPMC-GSE1	Flash A (288.5KB)	80-pin plastic LQFP (FPT-80P-M21)
MB96F636RBPMC-GSE2		
MB96F637RBPMC-GSE1	Flash A (416.5KB)	80-pin plastic LQFP (FPT-80P-M21)
MB96F637RBPMC-GSE2		

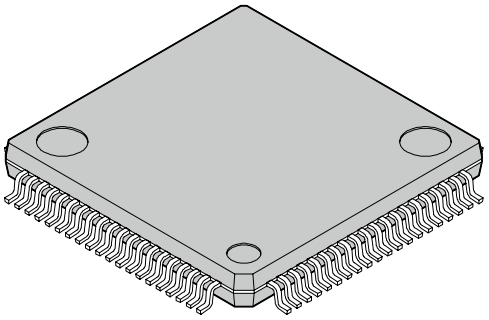
*: For details about package, see "Package Dimension".

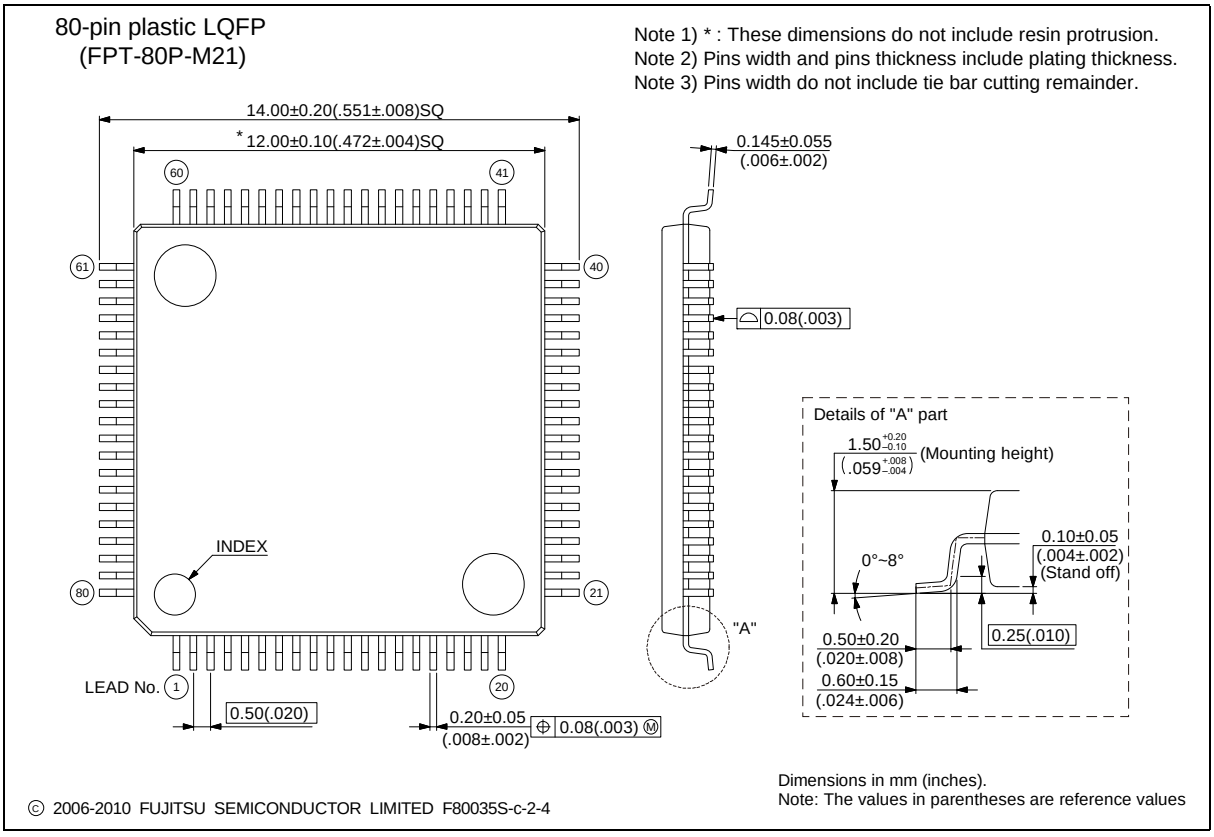
MCU without CAN controller

Part number	Flash memory	Package*
MB96F633ABPMC-GSE1	Flash A (96.5KB)	80-pin plastic LQFP (FPT-80P-M21)
MB96F633ABPMC-GSE2		
MB96F635ABPMC-GSE1	Flash A (160.5KB)	80-pin plastic LQFP (FPT-80P-M21)
MB96F635ABPMC-GSE2		

*: For details about package, see "Package Dimension".

17. Package Dimension

80-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	12 mm × 12 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.47 g
(FPT-80P-M21)	Code (Reference)	P-LFQFP80-12×12-0.50



Page	Section	Change Results
21	Interrupt Vector Table	Changed the Description of CALLV0 to CALLV7 Reserved → CALLV instruction
		Changed the Description of RESET Reserved → Reset vector
		Changed the Description of INT9 Reserved → INT9 instruction
		Changed the Description of EXCEPTION Reserved → Undefined instruction execution
22		Changed the Vector name of Vector number 64 PPGRLT → RLT6
		Changed the Description of Vector number 64 Reload Timer 6 can be used as PPG clock source → Reload Timer 6
25 to 28	Handling Precautions	Added a section
30	Handling Devices	Added the description to “3. External clock usage” (3) Opposite phase external clock
		Changed the description in “7. Turn on sequence of power supply to A/D converter and analog inputs” In this case, the voltage must not exceed AVRH or AV_{CC} → In this case, AVRH must not exceed AV_{CC}. Input voltage for ports shared with analog input ports also must not exceed AV_{CC}
31		Added the description “12. Mode Pin (MD)”
33	Electrical Characteristics 1. Absolute Maximum Ratings	Changed the annotation *4 Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode). → Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
33	1. Absolute Maximum Ratings	Added the annotation *4 The DEBUG I/F pin has only a protective diode against V_{SS}. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.
35	2. Recommended Operating Conditions	Added the Value and Remarks to “Power supply voltage” Min: 2.0V Typ: - Max: 5.5V Remarks: Maintains RAM data in stop mode
		Changed the Value of “Smoothing capacitor at C pin” Typ: 1.0µF → 1.0µF to 3.9µF Max: 1.5µF → 4.7µF
		Changed the Remarks of “Smoothing capacitor at C pin” Deleted “(Target value)” Added “3.9µF (Allowance within ± 20%)”

Page	Section	Change Results
57	7. Flash Memory Write/Erase Characteristics	Changed the Value of “Sector erase time”
		Added “Security Sector” to “Sector erase time”
		Changed the Parameter “Half word (16 bit) write time” → “Word (16-bit) write time”
		Changed the Value of “Chip erase time”
		Changed the Remarks of “Sector erase time” Excludes write time prior to internal erase → Includes write time prior to internal erase
		Added the Note and annotation *1
		Deleted “(targeted value)” from title “ Write/Erase cycles and data hold time”
58 to 60	Example Characteristics	Added a section
61	Ordering Information	Changed part number MCU with CAN controller MB96F636RAPMC-GSE1* → MB96F636RBPMC-GSE1 MB96F636RAPMC-GSE2* → MB96F636RBPMC-GSE2 MB96F637RAPMC-GSE1* → MB96F637RBPMC-GSE1 MB96F637RAPMC-GSE2* → MB96F637RBPMC-GSE2
61	Ordering Information	Added part number MCU with CAN controller MB96F633RBPMC-GSE1 MB96F633RBPMC-GSE2 MB96F635RBPMC-GSE1 MB96F635RBPMC-GSE2 MCU without CAN controller MB96F633ABPMC-GSE1 MB96F633ABPMC-GSE2 MB96F635ABPMC-GSE1 MB96F635ABPMC-GSE2
Revision 1.1		
-	-	Company name and layout design change

NOTE: Please see “Document History” about later revised information.

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