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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32zg222f16-qfp48

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32ZG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32ZG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32ZG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Inter-Integrated Circuit Interface (I2C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.21 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.22 General Purpose Input/Output (GPIO)

In the EFM32ZG222, there are 37 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32ZG222 is a subset of the feature set described in the EFM32ZG Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

Table 2.1. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO,
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART1	Full configuration with I2S and IrDA	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[4:0], ACMP0_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[3:0]
IDAC0	Full configuration	IDAC0_OUT
AES	Full configuration	NA

3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}\text{C}$ and $V_{DD}=3.0\text{ V}$, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8).

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150 ¹	$^{\circ}\text{C}$
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	$^{\circ}\text{C}$
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		$V_{DD}+0.3$	V

¹Based on programmed devices tested for 10000 hours at 150°C . Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	$^{\circ}\text{C}$
V_{DDOP}	Operating supply voltage	1.98		3.8	V
f_{APB}	Internal APB clock frequency			24	MHz
f_{AHB}	Internal AHB clock frequency			24	MHz

3.4.1 EM0 Current Consumption

Figure 3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 24 MHz

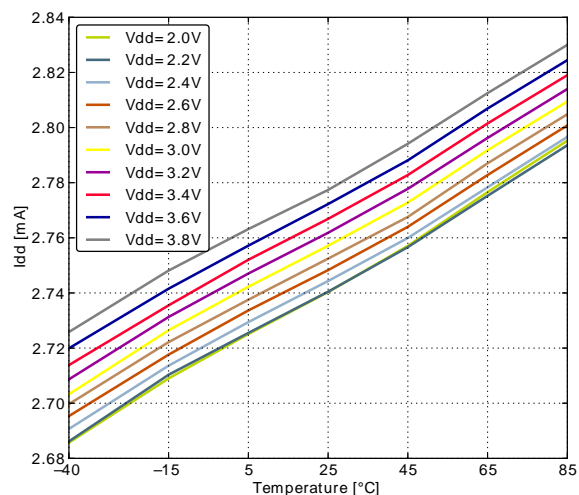
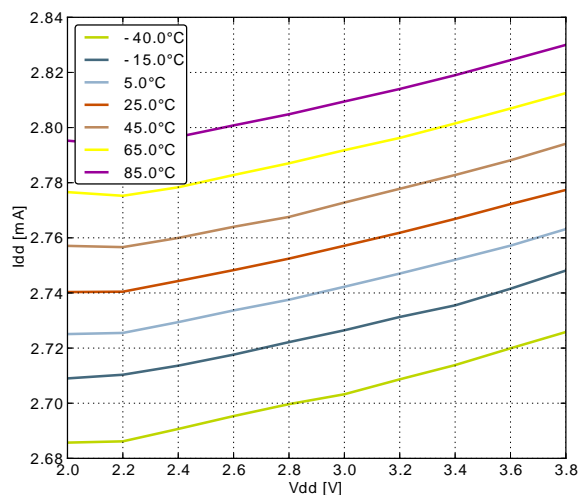
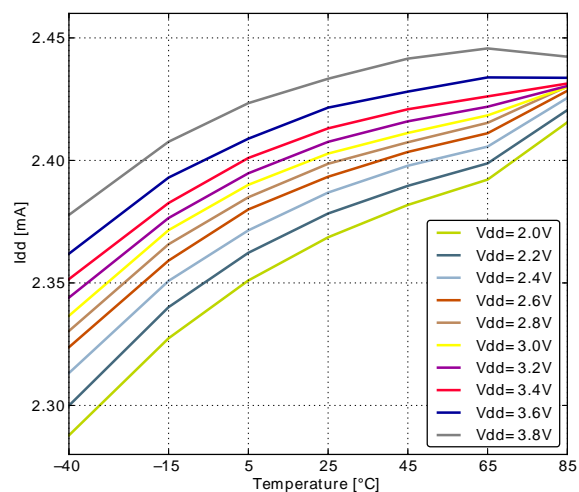
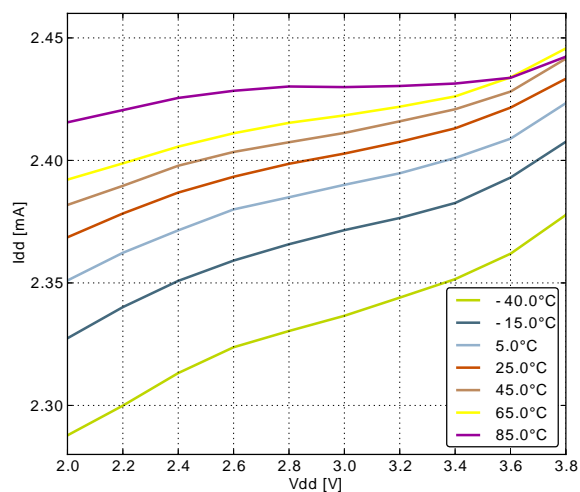
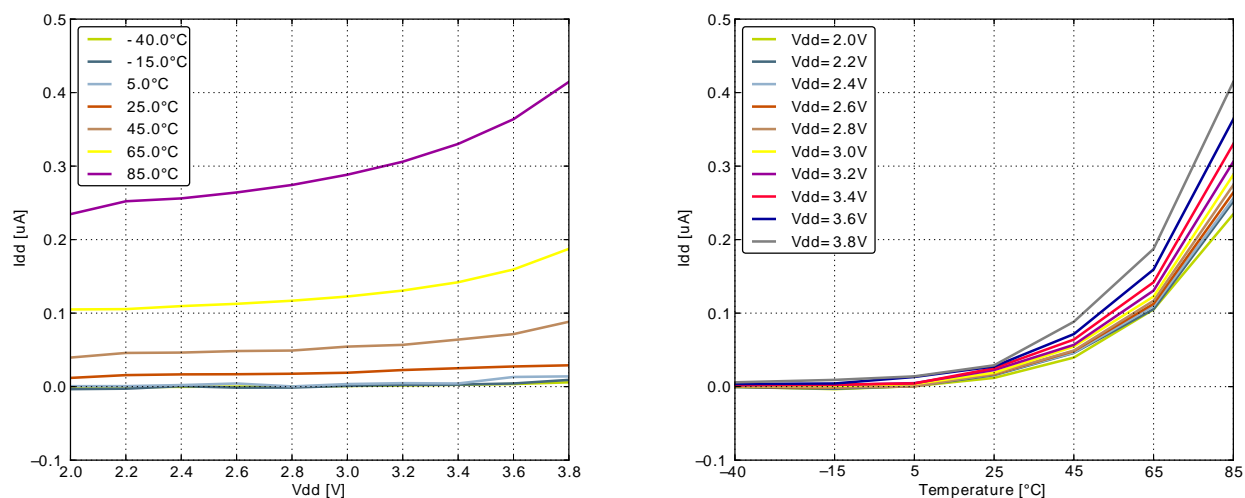


Figure 3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz



3.4.5 EM4 Current Consumption

Figure 3.13. EM4 current consumption.



3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

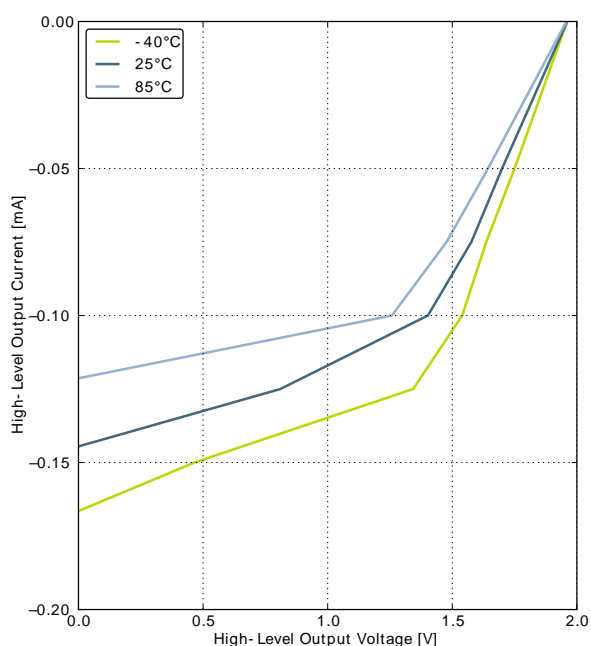
Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		μs
t_{EM30}	Transition time from EM3 to EM0		2		μs
t_{EM40}	Transition time from EM4 to EM0		163		μs

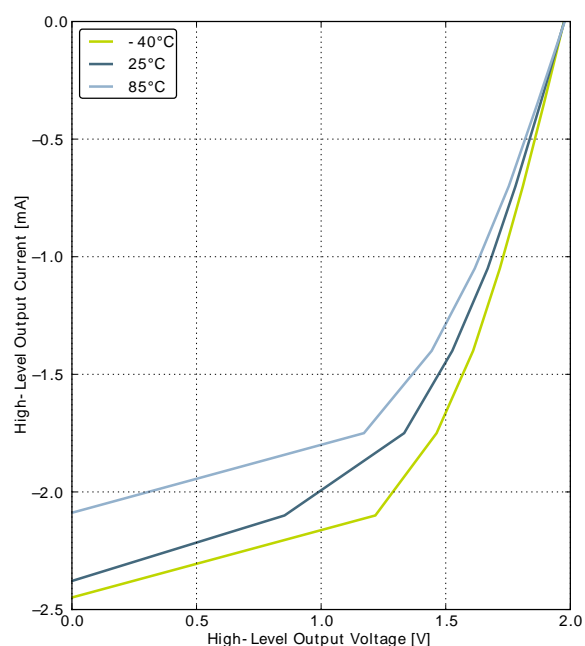
3.6 Power Management

The EFM32ZG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

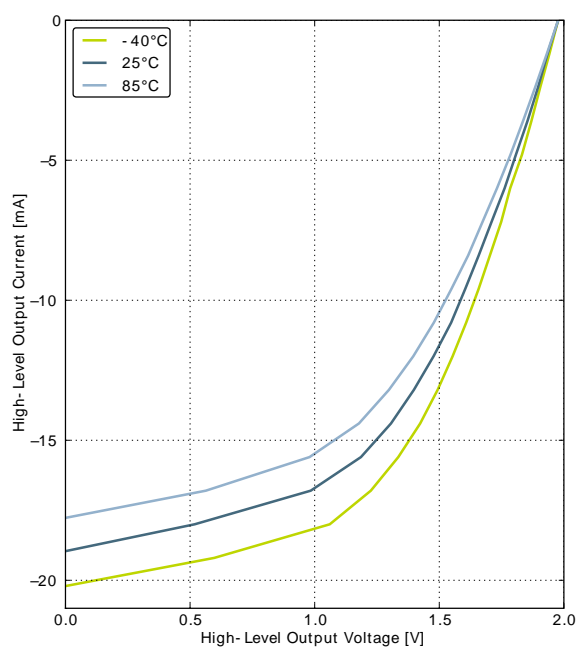
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sourcing 1 mA, $V_{DD}=1.98\text{ V}$, GPIO_Px_CTRL DRIVEMODE = LOW		$0.85V_{DD}$		V
		Sourcing 1 mA, $V_{DD}=3.0\text{ V}$, GPIO_Px_CTRL DRIVEMODE = LOW		$0.90V_{DD}$		V
		Sourcing 6 mA, $V_{DD}=1.98\text{ V}$, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.75V_{DD}$			V
		Sourcing 6 mA, $V_{DD}=3.0\text{ V}$, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.85V_{DD}$			V
		Sourcing 20 mA, $V_{DD}=1.98\text{ V}$, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.60V_{DD}$			V
		Sourcing 20 mA, $V_{DD}=3.0\text{ V}$, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80V_{DD}$			V
V_{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, $V_{DD}=1.98\text{ V}$, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.20V_{DD}$		V
		Sinking 0.1 mA, $V_{DD}=3.0\text{ V}$, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.10V_{DD}$		V
		Sinking 1 mA, $V_{DD}=1.98\text{ V}$, GPIO_Px_CTRL DRIVEMODE = LOW		$0.10V_{DD}$		V
		Sinking 1 mA, $V_{DD}=3.0\text{ V}$, GPIO_Px_CTRL DRIVEMODE = LOW		$0.05V_{DD}$		V
		Sinking 6 mA, $V_{DD}=1.98\text{ V}$, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.30V_{DD}$	V
		Sinking 6 mA, $V_{DD}=3.0\text{ V}$, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.20V_{DD}$	V
		Sinking 20 mA, $V_{DD}=1.98\text{ V}$, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.35V_{DD}$	V
		Sinking 20 mA, $V_{DD}=3.0\text{ V}$, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.25V_{DD}$	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or Vdd		± 0.1	± 100	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed		10		50	ns

Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage

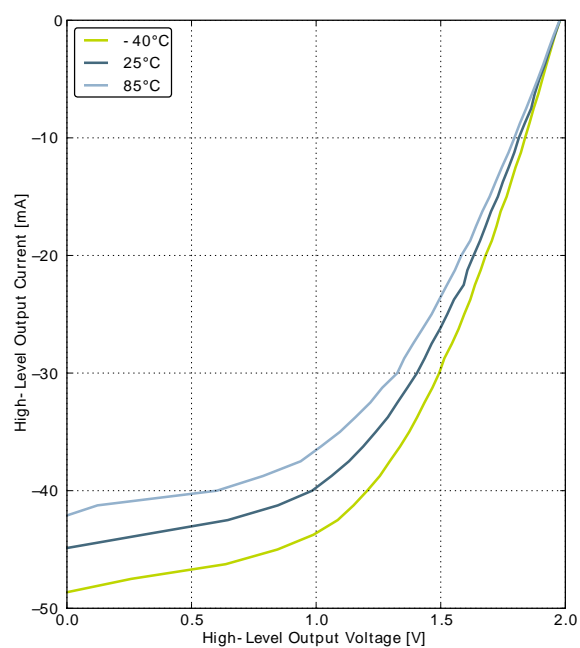
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

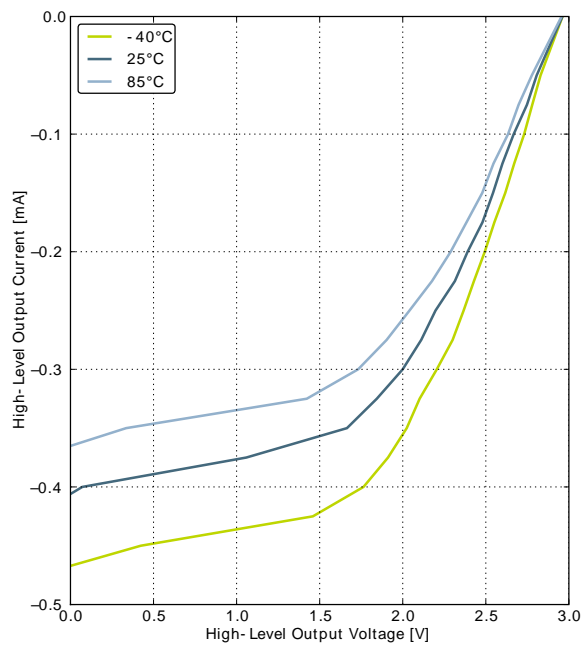


GPIO_Px_CTRL DRIVEMODE = STANDARD

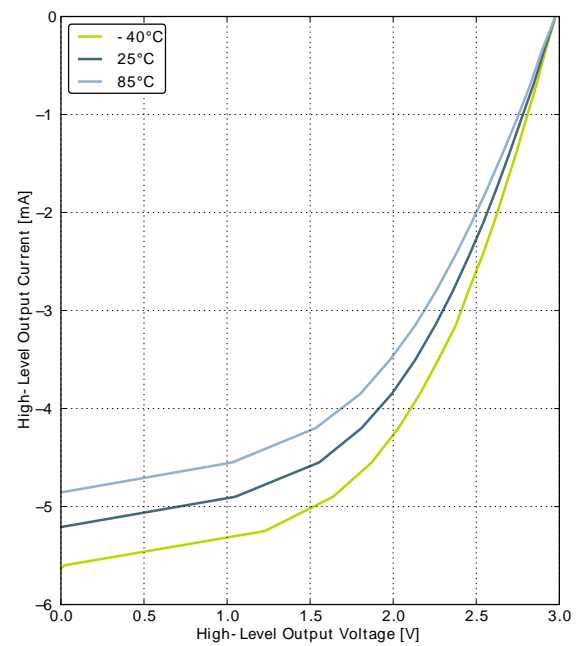


GPIO_Px_CTRL DRIVEMODE = HIGH

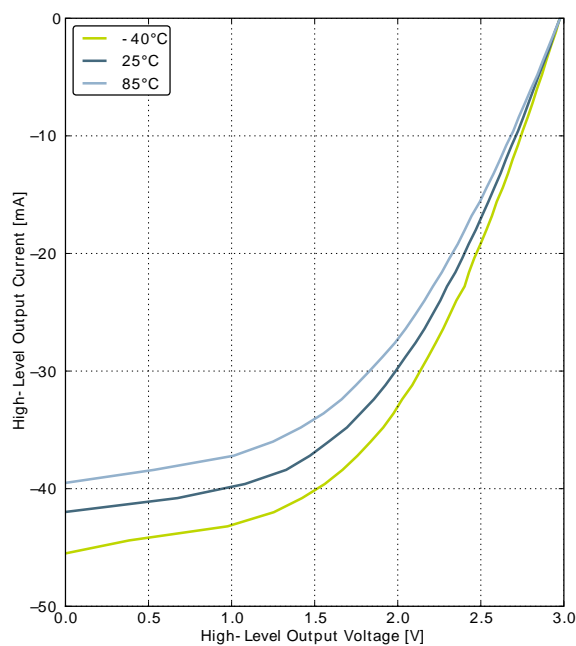
Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage



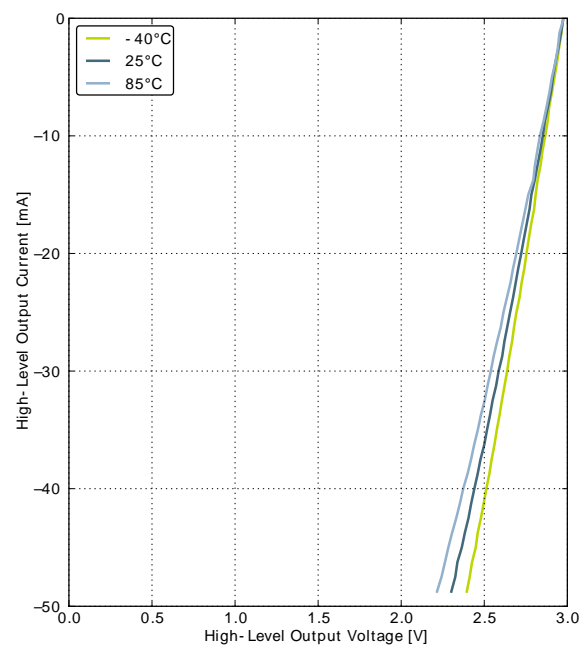
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

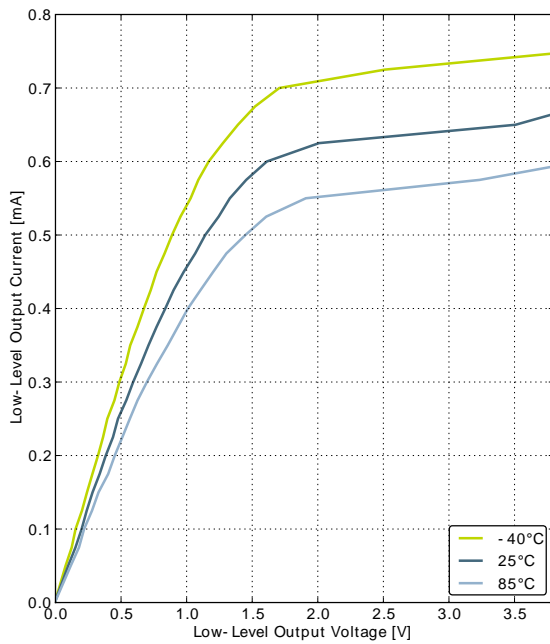


GPIO_Px_CTRL DRIVEMODE = STANDARD

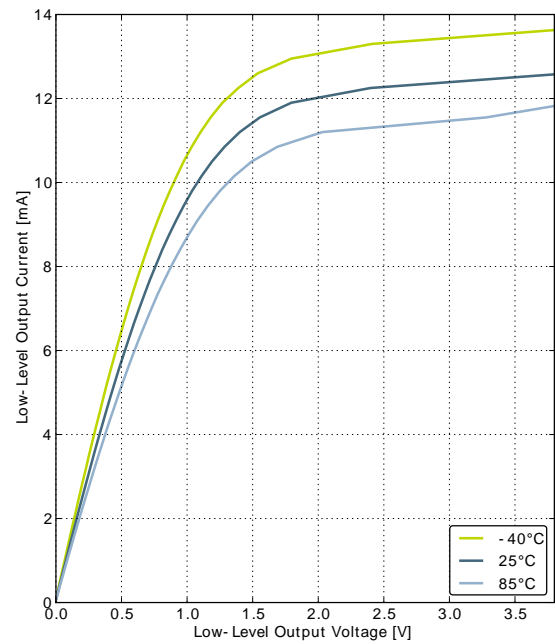


GPIO_Px_CTRL DRIVEMODE = HIGH

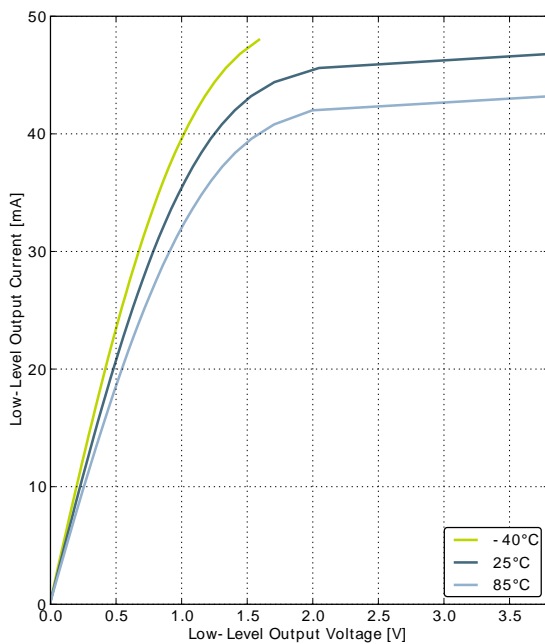
Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage



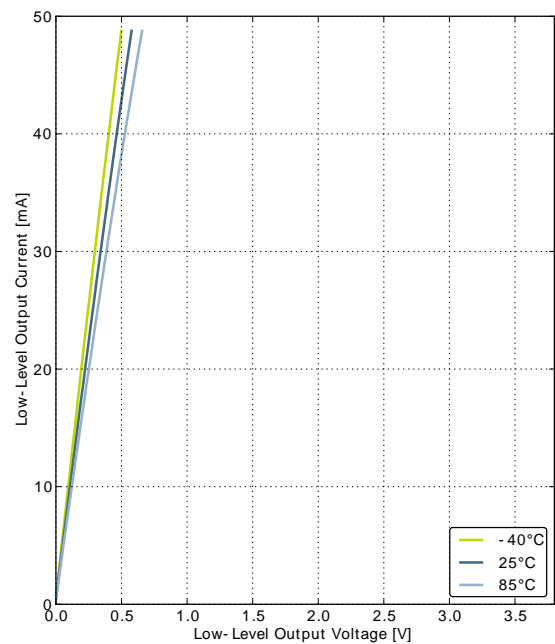
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		5		25	pF
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L =10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		1100		ms

For safe startup of a given crystal, the energyAware Designer in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.9. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		24	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 24 MHz		30	100	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L =20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		μ A
		24 MHz: ESR=30 Ohm, C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		μ A
t_{HFXO}	Startup time	24 MHz: ESR=30 Ohm, C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		785		μ s

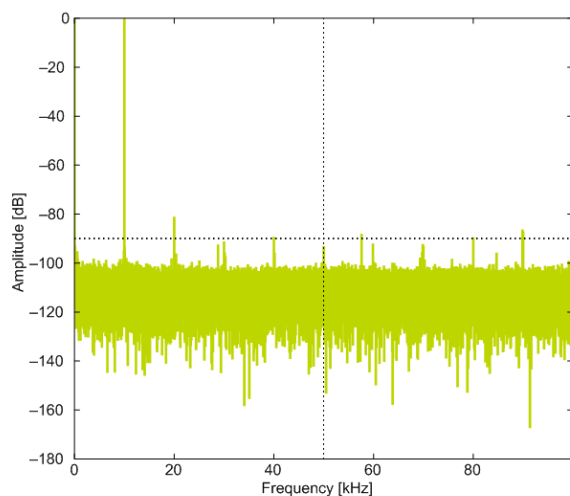
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		76		dBc
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, V_{DD} reference	68	79		dBc
		200 kSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		79		dBc
$V_{ADCOFFSET}$	Offset voltage	After calibration, single ended	-4	0.3	4	mV
		After calibration, differential		0.3		mV
$TGRAD_{ADCTH}$	Thermometer output gradient			-1.92		mV/°C
				-6.3		ADC Codes/°C
DNL_{ADC}	Differential non-linearity (DNL)	$V_{DD} = 3.0$ V, external 2.5V reference	-1	± 0.7	4	LSB
INL_{ADC}	Integral non-linearity (INL), End point method	$V_{DD} = 3.0$ V, external 2.5V reference		± 1.2	± 3	LSB
MC_{ADC}	No missing codes		11.999 ¹	12		bits

¹On the average every ADC will have one missing code, most likely to appear around $2048 \pm n \times 512$ where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

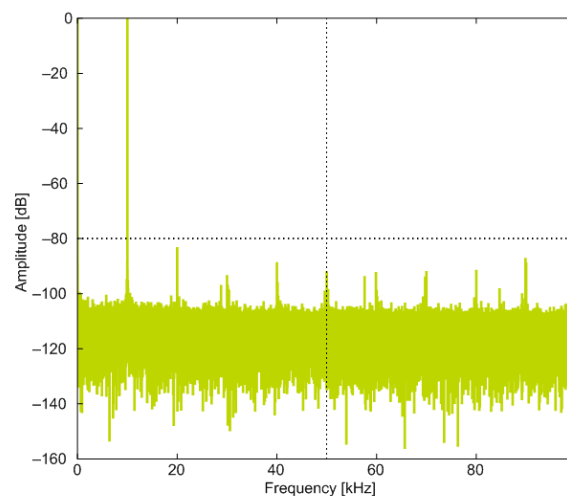
The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.26 (p. 36) and Figure 3.27 (p. 36) , respectively.

3.10.1 Typical performance

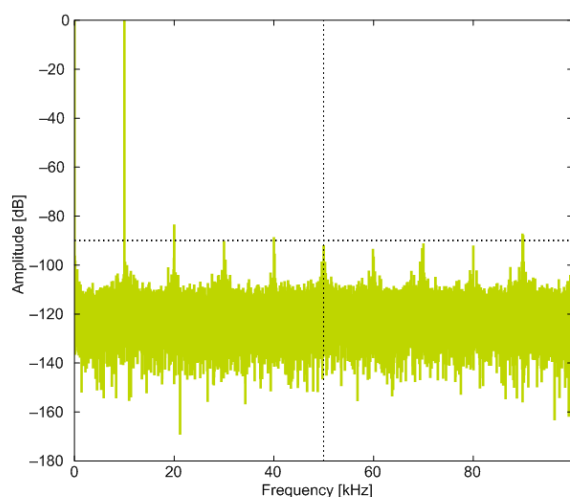
Figure 3.28. ADC Frequency Spectrum, $V_{dd} = 3V$, Temp = 25°C



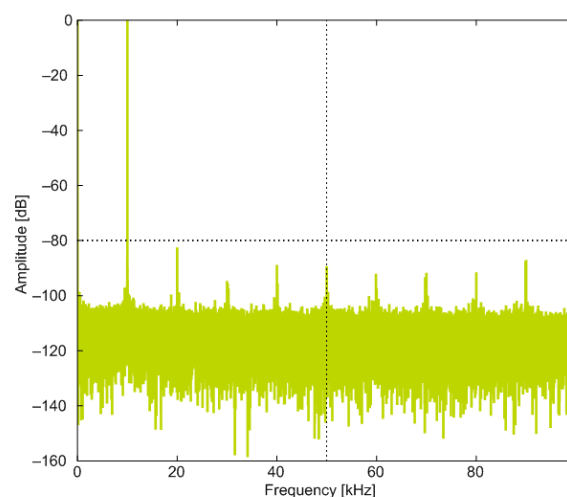
1.25V Reference



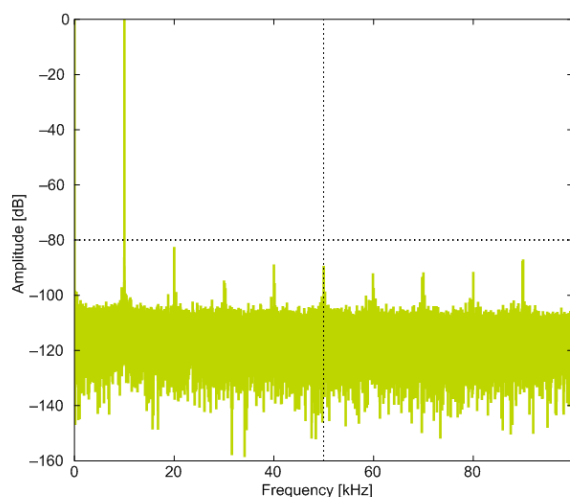
2.5V Reference



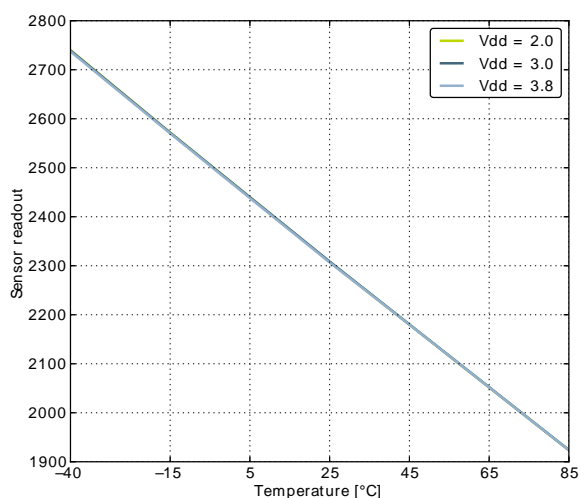
2XVDDVSS Reference



5VDIFF Reference



VDD Reference

Figure 3.33. ADC Temperature sensor readout

3.11 Current Digital Analog Converter (IDAC)

Table 3.15. IDAC Range 0 Source

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		11.7		μA
		Duty-cycled		10		nA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			0.84		μA
I_{STEP}	Step size			0.049		μA
I_D	Current drop at high impedance load	$V_{IDAC_OUT} = V_{DD} - 100mV$		0.73		%
TC_{IDAC}	Temperature coefficient	$V_{DD} = 3.0V$, STEPSEL=0x10		0.3		nA/°C
VC_{IDAC}	Voltage coefficient	$T = 25\text{ }^{\circ}C$, STEPSEL=0x10		11.7		nA/V

Table 3.16. IDAC Range 0 Sink

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		13.7		μA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			0.84		μA
I_{STEP}	Step size			0.050		μA
I_D	Current drop at high impedance load	$V_{IDAC_OUT} = 200\text{ mV}$		0.16		%
TC_{IDAC}	Temperature coefficient	$V_{DD} = 3.0\text{ V}$, STEPSEL=0x10		0.2		nA/°C
VC_{IDAC}	Voltage coefficient	$T = 25\text{ }^{\circ}C$, STEPSEL=0x10		12.5		nA/V

3.13 Voltage Comparator (VCMP)

Table 3.25. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{VCMPIN}	Input voltage range			V _{DD}		V
V _{VCMP_{CM}}	VCMP Common Mode voltage range			V _{DD}		V
I _{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.1	0.8	μA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		14.7	35	μA
t _{VCMPREF}	Startup time reference generator	NORMAL		10		μs
V _{VCMP_{OFFSET}}	Offset voltage	Single ended		10		mV
		Differential		10		mV
V _{VCMPHYST}	VCMP hysteresis			17		mV
t _{VCMPSTART}	Startup time				10	μs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD} \text{ Trigger Level} = 1.667V + 0.034 \times \text{TRIGLEVEL} \quad (3.2)$$

3.14 I2C

Table 3.26. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		100 ¹	kHz
t _{LOW}	SCL clock low time	4.7			μs
t _{HIGH}	SCL clock high time	4.0			μs
t _{SU,DAT}	SDA set-up time	250			ns
t _{HD,DAT}	SDA hold time	8		3450 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	4.7			μs
t _{HD,STA}	(Repeated) START condition hold time	4.0			μs
t _{SU,STO}	STOP condition set-up time	4.0			μs
t _{BUF}	Bus free time between a STOP and START condition	4.7			μs

¹For the minimum HPPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32ZG Reference Manual.

²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10⁻⁹ [s] * f_{HPPERCLK} [Hz]) - 5).

Table 3.27. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		400 ¹	kHz
t _{LOW}	SCL clock low time	1.3			μs
t _{HIGH}	SCL clock high time	0.6			μs
t _{SU,DAT}	SDA set-up time	100			ns
t _{HD,DAT}	SDA hold time	8		900 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	0.6			μs
t _{HD,STA}	(Repeated) START condition hold time	0.6			μs
t _{SU,STO}	STOP condition set-up time	0.6			μs
t _{BUF}	Bus free time between a STOP and START condition	1.3			μs

¹For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32ZG Reference Manual.

²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*10⁻⁹ [s] * f_{HFPERCLK} [Hz]) - 5).

Table 3.28. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		1000 ¹	kHz
t _{LOW}	SCL clock low time	0.5			μs
t _{HIGH}	SCL clock high time	0.26			μs
t _{SU,DAT}	SDA set-up time	50			ns
t _{HD,DAT}	SDA hold time	8			ns
t _{SU,STA}	Repeated START condition set-up time	0.26			μs
t _{HD,STA}	(Repeated) START condition hold time	0.26			μs
t _{SU,STO}	STOP condition set-up time	0.26			μs
t _{BUF}	Bus free time between a STOP and START condition	0.5			μs

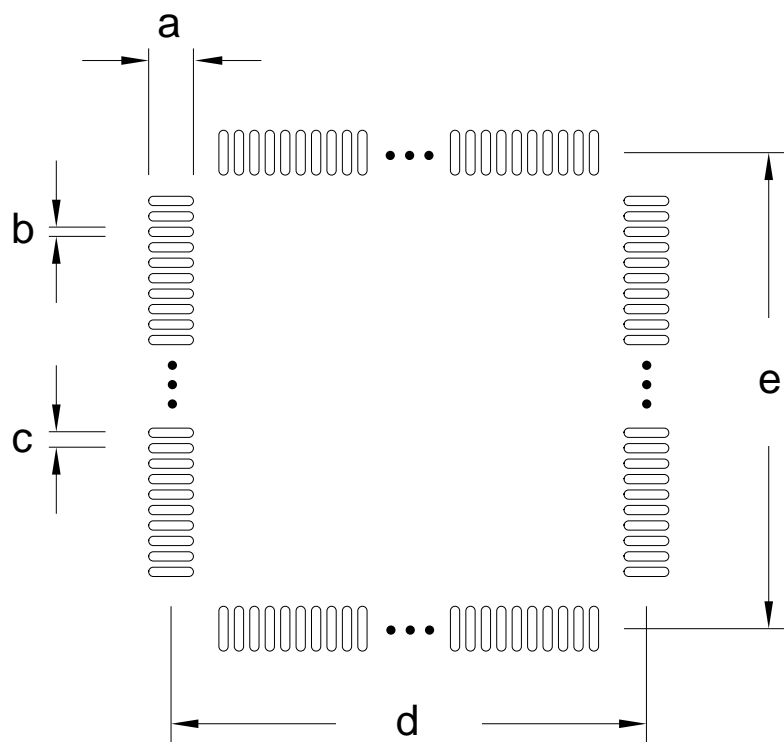
¹For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32ZG Reference Manual.

3.15 Digital Peripherals

Table 3.29. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{USART}	USART current	USART idle current, clock enabled		7.5		μA/ MHz
I _{LEUART}	LEUART current	LEUART idle current, clock enabled		150		nA
I _{I2C}	I2C current	I2C idle current, clock enabled		6.25		μA/ MHz
I _{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		μA/ MHz
I _{PCNT}	PCNT current	PCNT idle current, clock enabled		100		nA
I _{RTC}	RTC current	RTC idle current, clock enabled		100		nA

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
CMU_CLK1	PA1		PE12					Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0							Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1							Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7			PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			PC0	PF0	PE12	I2C0 Serial Data input / output.
IDAC0_OUT	PB11							IDAC0 output.
LEU0_RX	PD5	PB14		PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13		PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7				Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0	PF3	PC14					Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4	PC15					Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5	PE10					Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1		PE11					Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1			PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2			PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM1_CC0	PC13	PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11	PC13			Timer 1 Capture Compare input / output channel 2.
US1_CLK	PB7		PF0	PC15				USART1 clock input / output.
US1_CS	PB8		PF1	PC14				USART1 chip select input / output.
US1_RX	PC1		PD6	PD6				USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0		PD7	PD7				USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

Figure 5.2. TQFP48 PCB Solder Mask**Table 5.2. QFP48 PCB Solder Mask Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)
a	1.72
b	0.42
c	0.50
d	8.50
e	8.50

7 Revision History

7.1 Revision 1.10

March 6th, 2015

Updated ADC data, updated temperature sensor graph and added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

Updated Max ESR_{HFXO} value for Crystal Frequency of 24 MHz.

Updated current consumption.

Updated LFXO and HFXO data.

Updated LFRCO and HFRCO data.

Updated ACMP data.

Updated VCMP data.

Updated Memory Map.

Added DMA current in Digital Peripherals section.

Added AUXHFRCO to block diagram and Electrical Characteristics.

Updated block diagram.

7.2 Revision 1.00

July 2nd, 2014

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Removed "Preliminary" markings.

Updated current consumption.

Updated transition between energy modes.

Updated power management data.

Updated GPIO data.

Updated LFXO, HFXO, HFRCO and ULFRCO data.

Updated LFRCO and HFRCO plots.

Updated ADC data.

Updated ACMP data.

7.3 Revision 0.61

November 21st, 2013

Updated figures.

Updated Cortex M0 related items in the memory map.

7.9 Revision 0.10

June 7th, 2011

Initial preliminary release.

List of Figures

2.1. Block Diagram	3
2.2. EFM32ZG222 Memory Map with largest RAM and Flash sizes	7
3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 24 MHz	11
3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz	11
3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz	12
3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz	12
3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 6.6 MHz	13
3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 24 MHz	13
3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz	14
3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz	14
3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz	15
3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6 MHz	15
3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.	16
3.12. EM3 current consumption.	16
3.13. EM4 current consumption.	17
3.14. Typical Low-Level Output Current, 2V Supply Voltage	21
3.15. Typical High-Level Output Current, 2V Supply Voltage	22
3.16. Typical Low-Level Output Current, 3V Supply Voltage	23
3.17. Typical High-Level Output Current, 3V Supply Voltage	24
3.18. Typical Low-Level Output Current, 3.8V Supply Voltage	25
3.19. Typical High-Level Output Current, 3.8V Supply Voltage	26
3.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage	28
3.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature	29
3.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature	30
3.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature	30
3.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature	30
3.25. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature	31
3.26. Integral Non-Linearity (INL)	36
3.27. Differential Non-Linearity (DNL)	36
3.28. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C	37
3.29. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C	38
3.30. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C	39
3.31. ADC Absolute Offset, Common Mode = Vdd /2	40
3.32. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V	40
3.33. ADC Temperature sensor readout	41
3.34. IDAC Source Current as a function of voltage on IDAC_OUT	44
3.35. IDAC Sink Current as a function of voltage from IDAC_OUT	45
3.36. IDAC linearity	45
3.37. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1	47
4.1. EFM32ZG222 Pinout (top view, not to scale)	51
4.2. TQFP48	55
5.1. TQFP48 PCB Land Pattern	57
5.2. TQFP48 PCB Solder Mask	58
5.3. TQFP48 PCB Stencil Design	59
6.1. Example Chip Marking (top view)	60