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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 24MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 4x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-TQFP |
| Supplier Device Package | 48-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32zg222f32-qfp48t |

### 2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

### 2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32ZG.

### 2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32ZG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

### 2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32ZG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

### 2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

### 2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

### 2.1.10 Inter-Integrated Circuit Interface (I2C)

The $I^2C$ module provides an interface between the MCU and a serial $I^2C$-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the $I^2C$ module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

### 2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

# 3 Electrical Characteristics

## 3.1 Test Conditions

### 3.1.1 Typical Values

The typical data are based on $T_{AMB}$=25°C and $V_{DD}$=3.0 V, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

### 3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

## 3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8) .

***Table 3.1. Absolute Maximum Ratings***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature range | | -40 | | 150[1] | °C |
| $T_S$ | Maximum soldering temperature | Latest IPC/JEDEC J-STD-020 Standard | | | 260 | °C |
| $V_{DDMAX}$ | External main supply voltage | | 0 | | 3.8 | V |
| $V_{IOPIN}$ | Voltage on any I/O pin | | -0.3 | | $V_{DD}$+0.3 | V |

[1]Based on programmed devices tested for 10000 hours at 150ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

## 3.3 General Operating Conditions

### 3.3.1 General Operating Conditions

***Table 3.2. General Operating Conditions***

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{AMB}$ | Ambient temperature range | -40 | | 85 | °C |
| $V_{DDOP}$ | Operating supply voltage | 1.98 | | 3.8 | V |
| $f_{APB}$ | Internal APB clock frequency | | | 24 | MHz |
| $f_{AHB}$ | Internal AHB clock frequency | | | 24 | MHz |

**Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz**

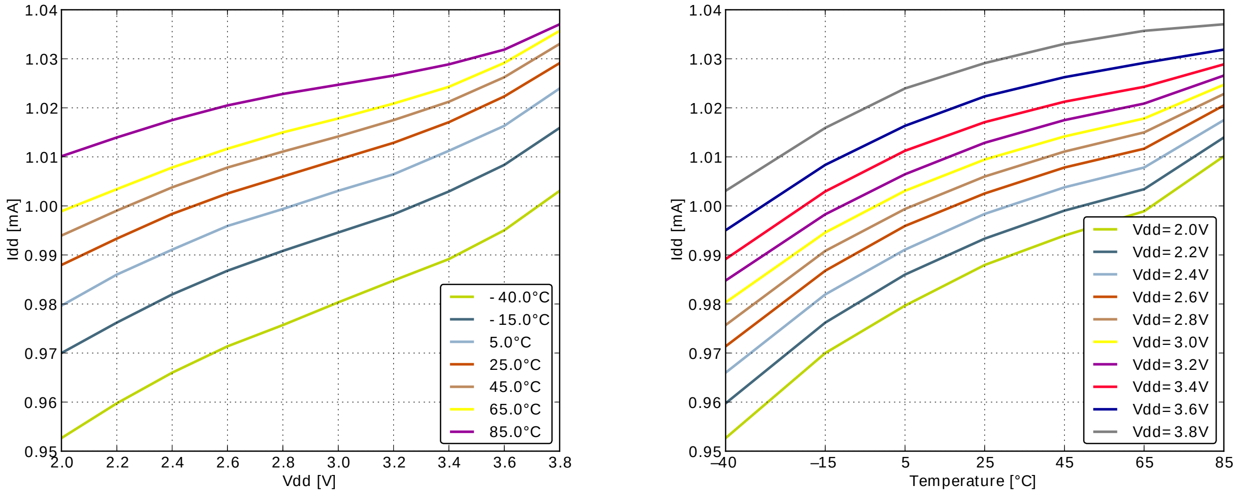



**Figure 3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz**

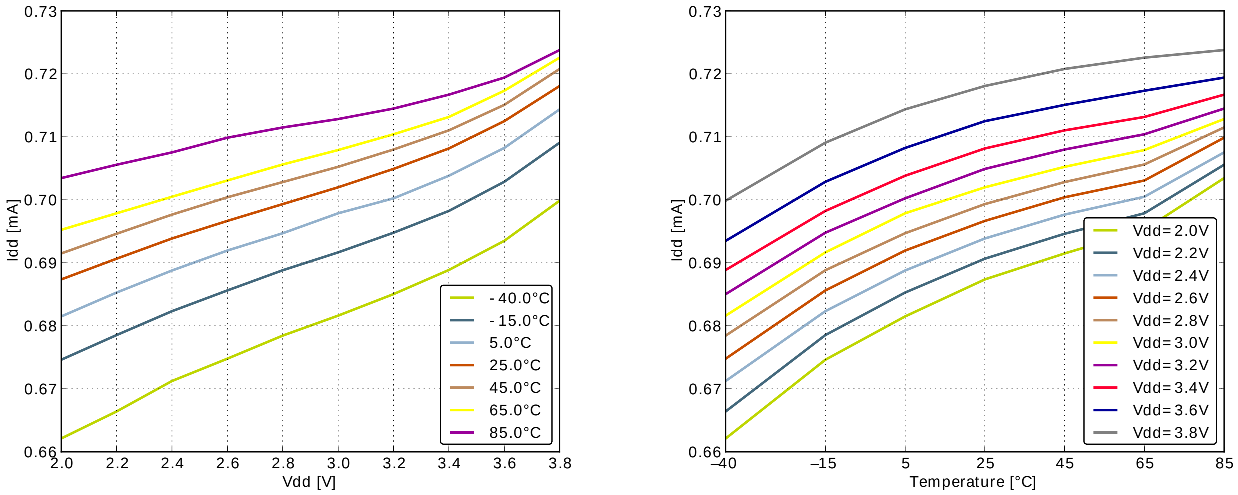


*Table 3.5. Power Management*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BODextthr-}$ | BOD threshold on falling external supply voltage | | 1.74 | | 1.96 | V |
| $V_{BODextthr+}$ | BOD threshold on rising external supply voltage | | | 1.85 | | V |
| $t_{RESET}$ | Delay from reset is released until program execution starts | Applies to Power-on Reset, Brown-out Reset and pin reset. | | 163 | | µs |
| $C_{DECOUPLE}$ | Voltage regulator decoupling capacitor. | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | | 1 | | µF |

# 3.7 Flash

*Table 3.6. Flash*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $EC_{FLASH}$ | Flash erase cycles before failure | | 20000 | | | cycles |
| $RET_{FLASH}$ | Flash data retention | $T_{AMB}$<150°C | 10000 | | | h |
| | | $T_{AMB}$<85°C | 10 | | | years |
| | | $T_{AMB}$<70°C | 20 | | | years |
| $t_{W\_PROG}$ | Word (32-bit) programming time | | 20 | | | µs |
| $t_{P\_ERASE}$ | Page erase time | | 20 | 20.4 | 20.8 | ms |
| $t_{D\_ERASE}$ | Device erase time | | 40 | 40.8 | 41.6 | ms |
| $I_{ERASE}$ | Erase current | | | | 7[1] | mA |
| $I_{WRITE}$ | Write current | | | | 7[1] | mA |
| $V_{FLASH}$ | Supply voltage during flash erase and write | | 1.98 | | 3.8 | V |

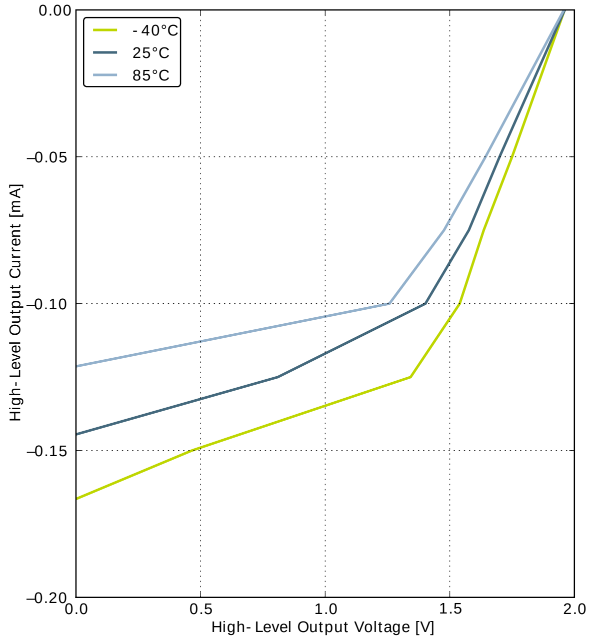
[1]Measured at 25°C

# 3.8 General Purpose Input Output

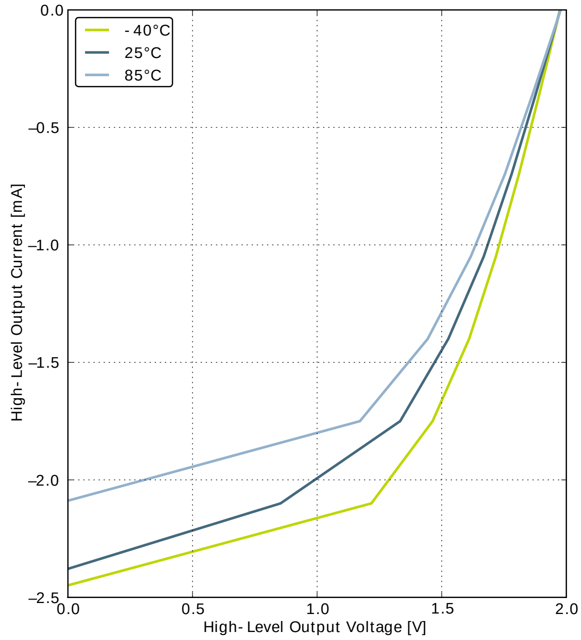
*Table 3.7. GPIO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IOIL}$ | Input low voltage | | | | $0.30V_{DD}$ | V |
| $V_{IOIH}$ | Input high voltage | | $0.70V_{DD}$ | | | V |
| $V_{IOOH}$ | Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | Sourcing 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.80V_{DD}$ | | V |
| | | Sourcing 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.90V_{DD}$ | | V |

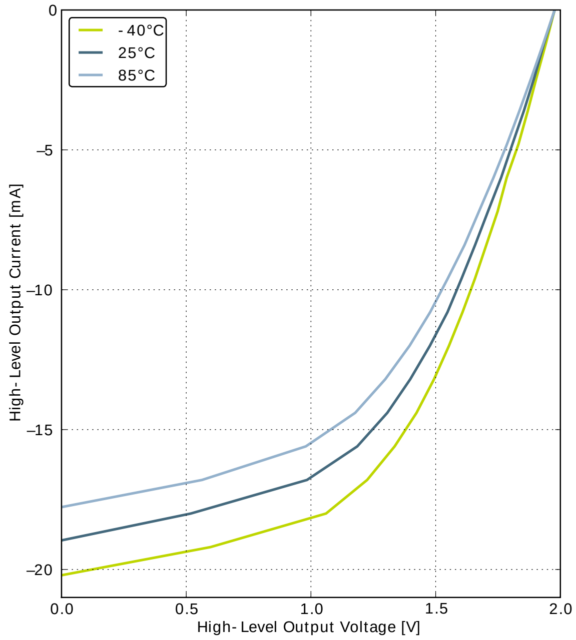
*Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage*



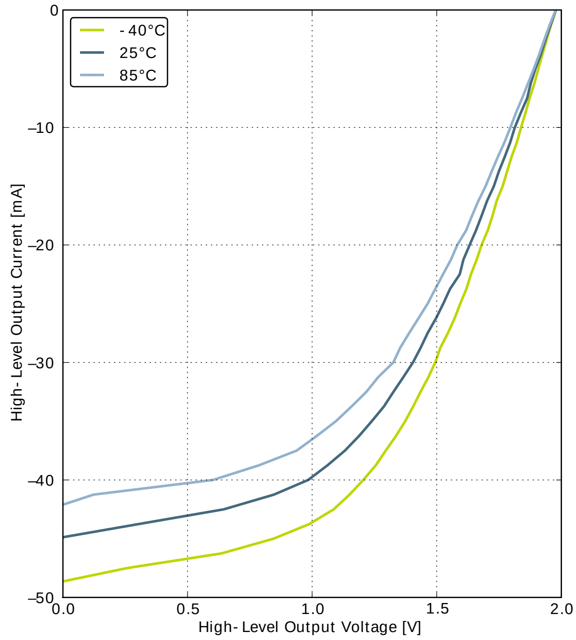

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

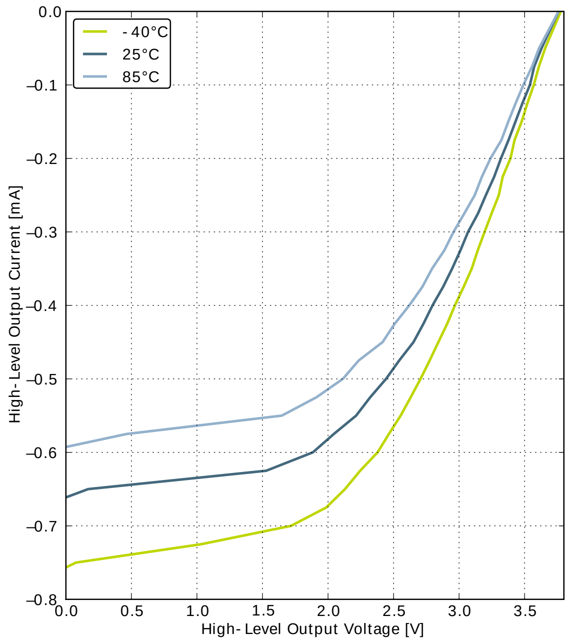



GPIO_Px_CTRL DRIVEMODE = STANDARD

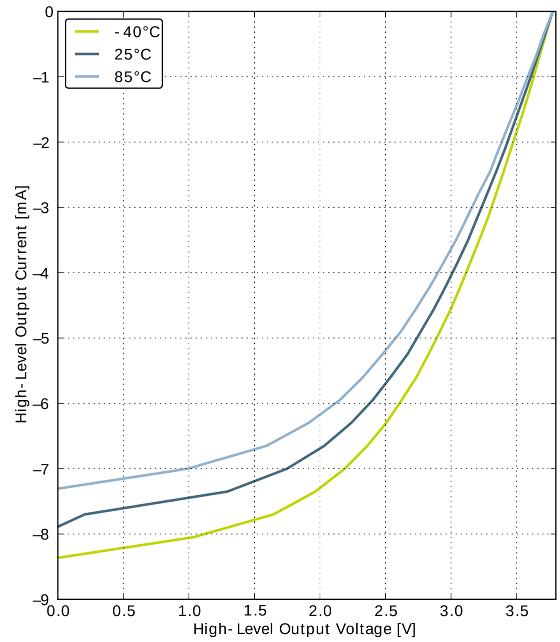



GPIO_Px_CTRL DRIVEMODE = HIGH

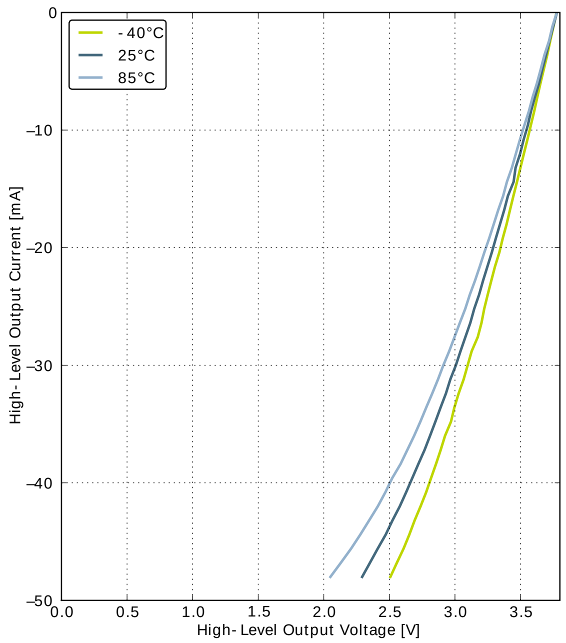
***Figure 3.19. Typical High-Level Output Current, 3.8V Supply Voltage***



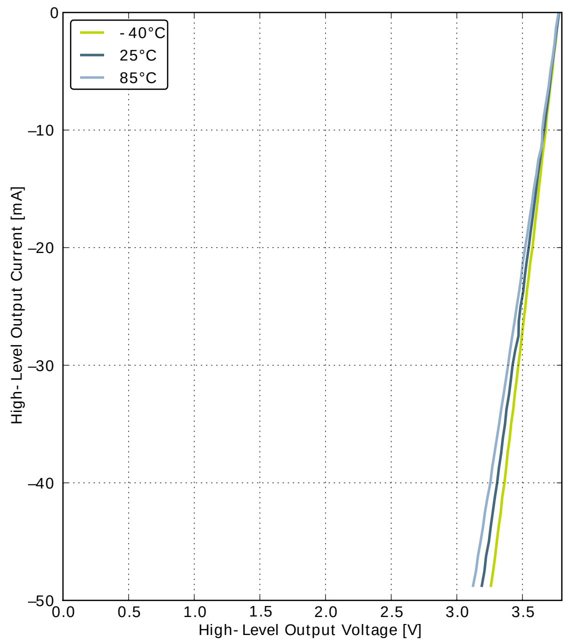

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW




GPIO_Px_CTRL DRIVEMODE = STANDARD




GPIO_Px_CTRL DRIVEMODE = HIGH

## 3.9.4 HFRCO

### *Table 3.11. HFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 21 MHz frequency band | 20.37 | 21.0 | 21.63 | MHz |
| | | 14 MHz frequency band | 13.58 | 14.0 | 14.42 | MHz |
| | | 11 MHz frequency band | 10.67 | 11.0 | 11.33 | MHz |
| | | 7 MHz frequency band | 6.40 | 6.60 | 6.80 | MHz |
| | | 1 MHz frequency band | 1.15 | 1.20 | 1.25 | MHz |
| $t_{HFRCO\_settling}$ | Settling time after start-up | $f_{HFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| $I_{HFRCO}$ | Current consumption (Production test condition = 14 MHz) | $f_{HFRCO}$ = 21 MHz | | 93 | 175 | µA |
| | | $f_{HFRCO}$ = 14 MHz | | 77 | 140 | µA |
| | | $f_{HFRCO}$ = 11 MHz | | 72 | 125 | µA |
| | | $f_{HFRCO}$ = 6.6 MHz | | 63 | 105 | µA |
| | | $f_{HFRCO}$ = 1.2 MHz | | 22 | 40 | µA |
| $TUNESTEP_{HFRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3[1] | | % |

[1]The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

### *Figure 3.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature*

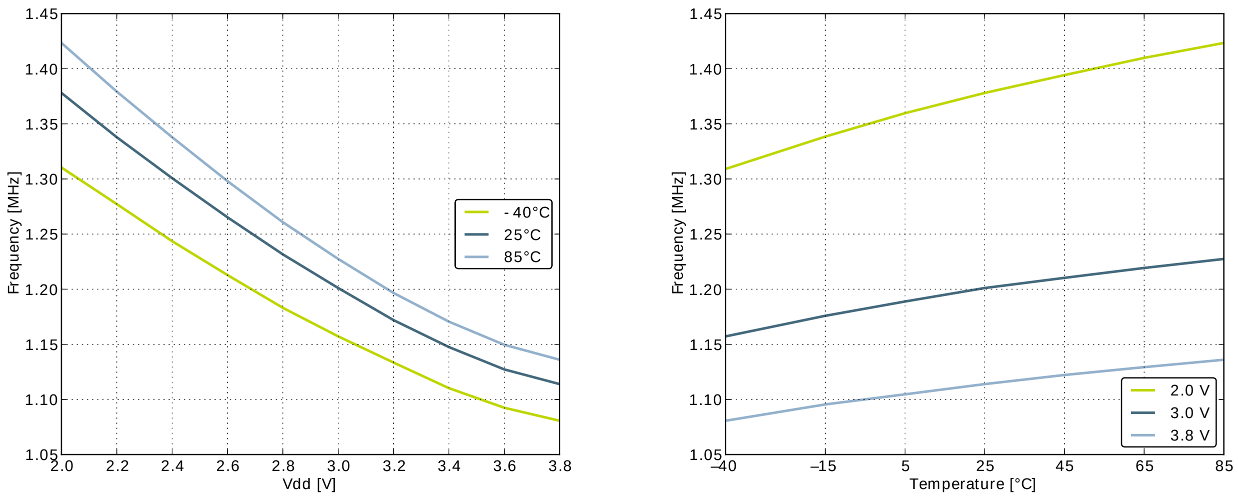
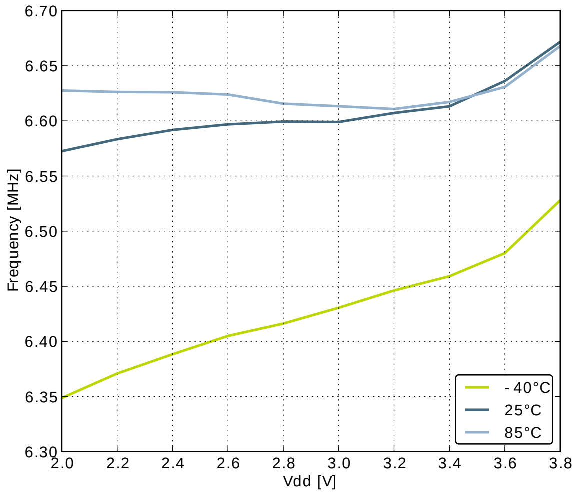


**Figure 3.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature**



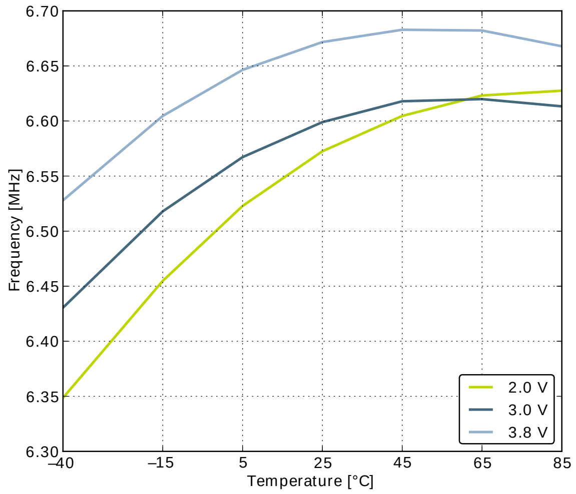
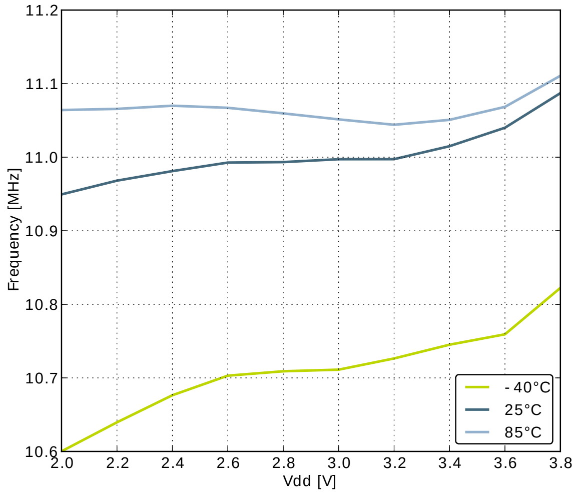




**Figure 3.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature**



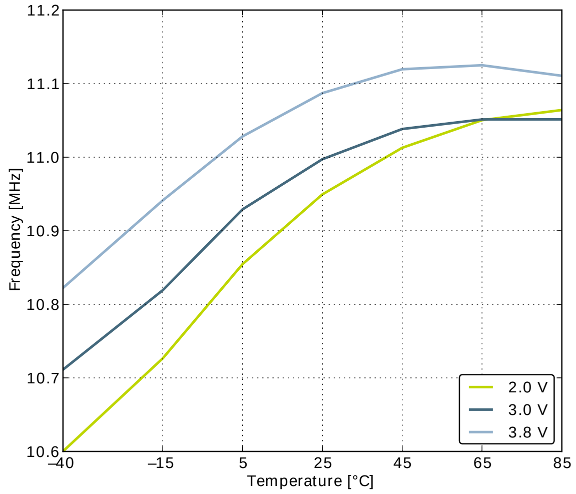
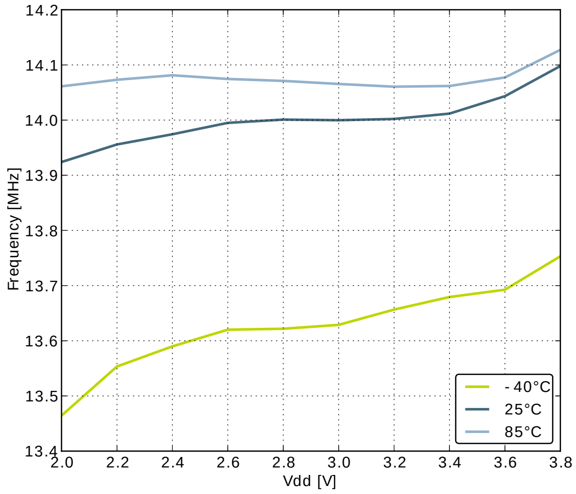
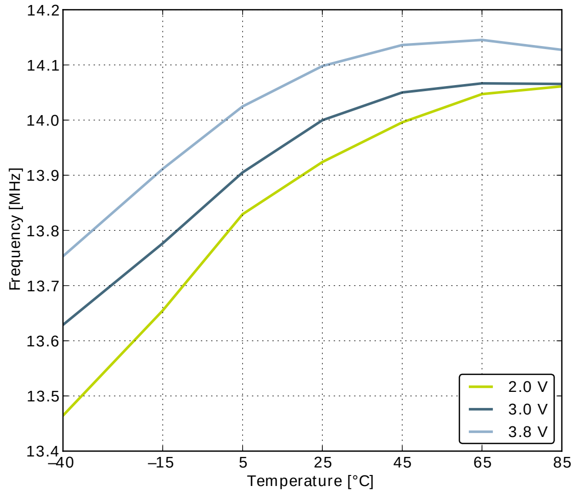




**Figure 3.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature**



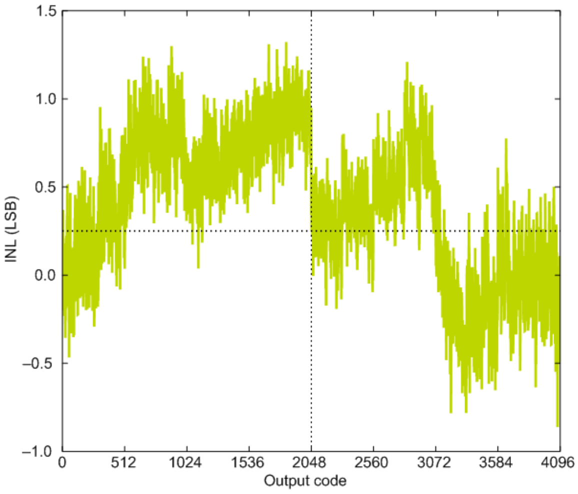
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | Differential | $-V_{REF}/2$ | | $V_{REF}/2$ | V |
| $V_{ADCREFIN}$ | Input range of external reference voltage, single ended and differential | | 1.25 | | $V_{DD}$ | V |
| $V_{ADCREFIN\_CH7}$ | Input range of external negative reference voltage on channel 7 | See $V_{ADCREFIN}$ | 0 | | $V_{DD}$ - 1.1 | V |
| $V_{ADCREFIN\_CH6}$ | Input range of external positive reference voltage on channel 6 | See $V_{ADCREFIN}$ | 0.625 | | $V_{DD}$ | V |
| $V_{ADCCMIN}$ | Common mode input range | | 0 | | $V_{DD}$ | V |
| $I_{ADCIN}$ | Input current | 2pF sampling capacitors | | <100 | | nA |
| $CMRR_{ADC}$ | Analog input common mode rejection ratio | | | 65 | | dB |
| $I_{ADC}$ | Average active current | 1 MSamples/s, 12 bit, external reference | | 351 | 500 | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00 | | 67 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01 | | 63 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10 | | 64 | | µA |
| $I_{ADCREF}$ | Current consumption of internal voltage reference | Internal voltage reference | | 65 | 127 | µA |
| $C_{ADCIN}$ | Input capacitance | | | 2 | | pF |
| $R_{ADCIN}$ | Input ON resistance | | 1 | | | MOhm |
| $R_{ADCFILT}$ | Input RC filter resistance | | | 10 | | kOhm |
| $C_{ADCFILT}$ | Input RC filter/decoupling capacitance | | | 250 | | fF |
| $f_{ADCCLK}$ | ADC Clock Frequency | | | | 13 | MHz |
| $t_{ADCCONV}$ | Conversion time | 6 bit | 7 | | | ADC-CLK Cycles |
| | | 8 bit | 11 | | | ADC-CLK Cycles |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 1 MSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 75 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 69 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 76 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 78 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 68 | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 79 | | dBc |
| $V_{ADCOFFSET}$ | Offset voltage | After calibration, single ended | -4 | 0.3 | 4 | mV |
| | | After calibration, differential | | 0.3 | | mV |
| $TGRAD_{ADCTH}$ | Thermometer output gradient | | | -1.92 | | mV/°C |
| | | | | -6.3 | | ADC Codes/°C |
| $DNL_{ADC}$ | Differential non-linearity (DNL) | $V_{DD}$= 3.0 V, external 2.5V reference | -1 | ±0.7 | 4 | LSB |
| $INL_{ADC}$ | Integral non-linearity (INL), End point method | $V_{DD}$= 3.0 V, external 2.5V reference | | ±1.2 | ±3 | LSB |
| $MC_{ADC}$ | No missing codes | | 11.999[1] | 12 | | bits |

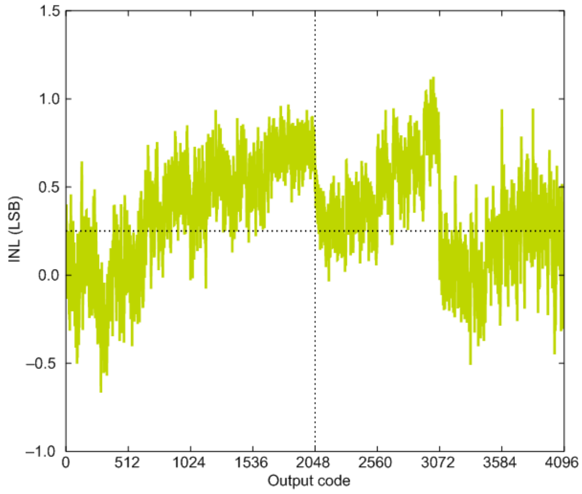
[1]On the average every ADC will have one missing code, most likely to appear around 2048 ± n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.26 (p. 36) and Figure 3.27 (p. 36) , respectively.

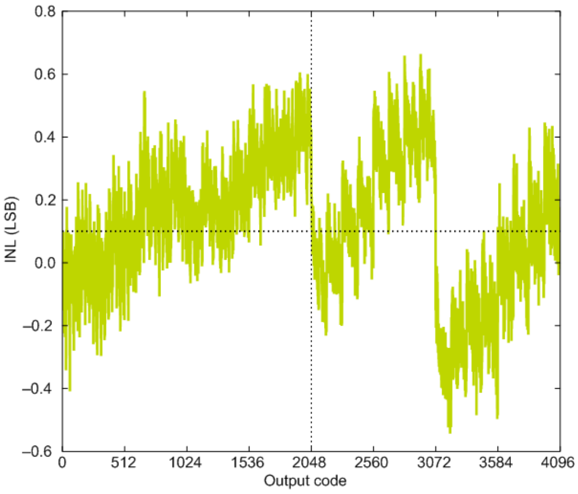
**Figure 3.29. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C**



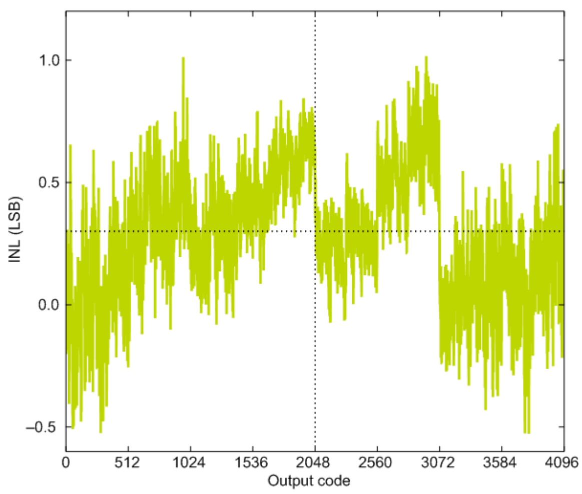

1.25V Reference



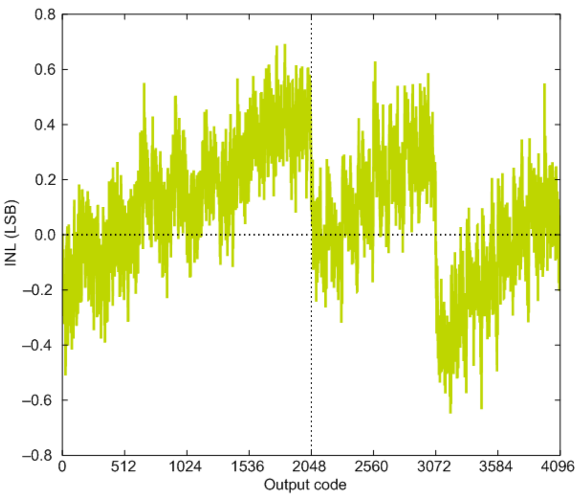

2.5V Reference




2XVDDVSS Reference

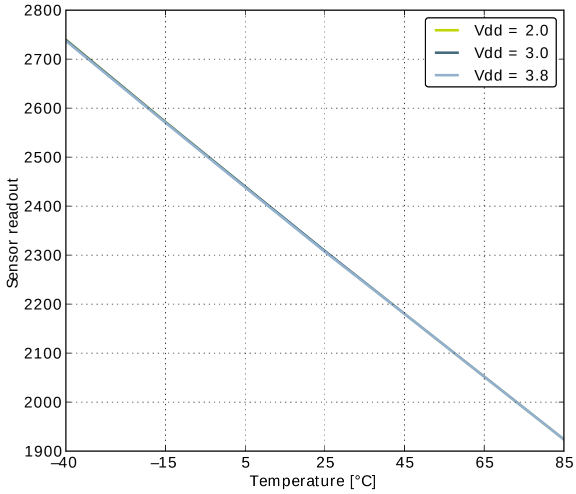



5VDIFF Reference




VDD Reference

**Figure 3.33. ADC Temperature sensor readout**




# 3.11 Current Digital Analog Converter (IDAC)

**Table 3.15. IDAC Range 0 Source**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 11.7 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 0.84 | | µA |
| $I_{STEP}$ | Step size | | | 0.049 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = $V_{DD}$ - 100mV | | 0.73 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0V, STEPSEL=0x10 | | 0.3 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 11.7 | | nA/V |

**Table 3.16. IDAC Range 0 Sink**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 13.7 | | µA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 0.84 | | µA |
| $I_{STEP}$ | Step size | | | 0.050 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = 200 mV | | 0.16 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 0.2 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 12.5 | | nA/V |

### Table 3.17. IDAC Range 1 Source

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 13.0 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 3.17 | | µA |
| $I_{STEP}$ | Step size | | | 0.097 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT} = V_{DD}$ - 100mV | | 0.79 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 0.7 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 38.4 | | nA/V |

### Table 3.18. IDAC Range 1 Sink

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 17.9 | | µA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 3.18 | | µA |
| $I_{STEP}$ | Step size | | | 0.098 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = 200 mV | | 0.20 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 0.7 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 40.9 | | nA/V |

### Table 3.19. IDAC Range 2 Source

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 16.2 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 8.40 | | µA |
| $I_{STEP}$ | Step size | | | 0.493 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT} = V_{DD}$ - 100mV | | 1.26 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 2.8 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 96.6 | | nA/V |

### Table 3.20. IDAC Range 2 Sink

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 28.4 | | µA |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 8.44 | | µA |
| $I_{STEP}$ | Step size | | | 0.495 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = 200 mV | | 0.55 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 2.8 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 94.4 | | nA/V |

### *Table 3.21. IDAC Range 3 Source*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 18.3 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 34.03 | | µA |
| $I_{STEP}$ | Step size | | | 1.996 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = $V_{DD}$ - 100 mV | | 3.18 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 10.9 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 159.5 | | nA/V |

### *Table 3.22. IDAC Range 3 Sink*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 62.9 | | µA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 34.16 | | µA |
| $I_{STEP}$ | Step size | | | 2.003 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = 200 mV | | 1.65 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 10.9 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 148.6 | | nA/V |

### *Table 3.23. IDAC*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{IDACSTART}$ | Start-up time, from enabled to output settled | | 40 | | µs |

# 4 Pinout and Package

**Note**

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32ZG222.

## 4.1 Pinout

The *EFM32ZG222* pinout is shown in Figure 4.1 (p. 51) and Table 4.1 (p. 51). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

***Figure 4.1. EFM32ZG222 Pinout (top view, not to scale)***

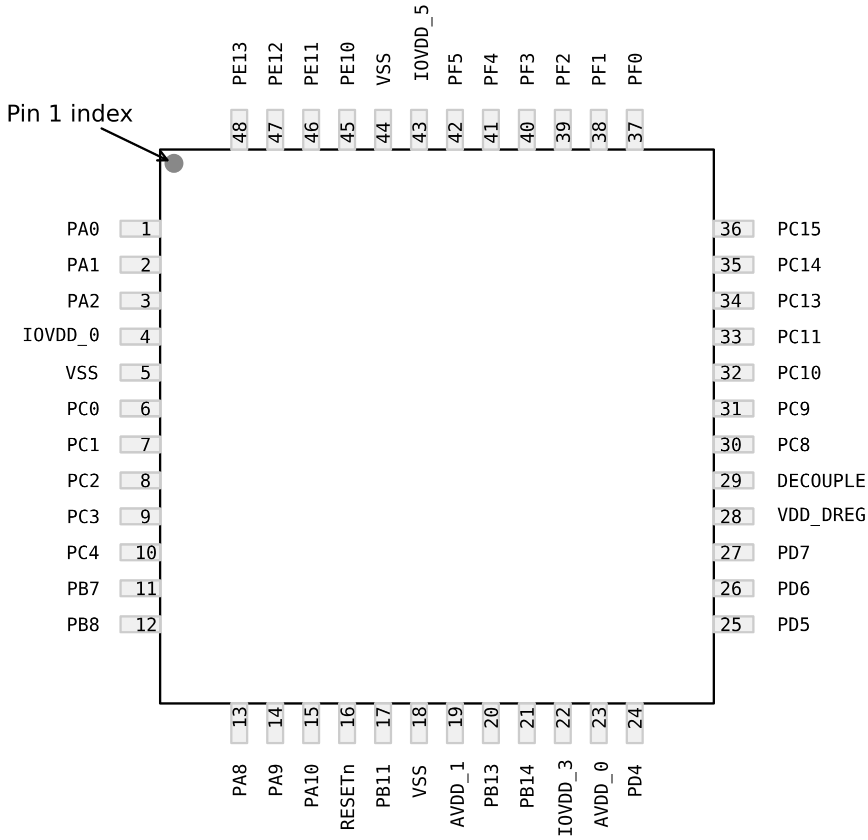



***Table 4.1. Device Pinout***

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |

5. Dimensions S and V to be determined at seating plane AC.
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.250 per side. Dimensions A and B do include mold mismatch and are determined at datum AB.
7. Dimension D does not include dambar protrusion. Dambar protrusion shall not cause the D dimension to exceed 0.350.
8. Minimum solder plate thickness shall be 0.0076.
9. Exact shape of each corner is optional.

*Table 4.4. QFP48 (Dimensions in mm)*

| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|---|---|---|---|---|---|---|---|
| A | - | 7.000 BSC | - | M | - | 12DEG REF | - |
| A1 | - | 3.500 BSC | - | N | 0.090 | - | 0.160 |
| B | - | 7.000 BSC | - | P | - | 0.250 BSC | - |
| B1 | - | 3.500 BSC | - | R | 0.150 | - | 0.250 |
| C | 1.000 | - | 1.200 | S | - | 9.000 BSC | - |
| D | 0.170 | - | 0.270 | S1 | - | 4.500 BSC | - |
| E | 0.950 | - | 1.050 | V | - | 9.000 BSC | - |
| F | 0.170 | - | 0.230 | V1 | - | 4.500 BSC | - |
| G | - | 0.500 BSC | - | W | - | 0.200 BSC | - |
| H | 0.050 | - | 0.150 | AA | - | 1.000 BSC | - |
| J | 0.090 | - | 0.200 | | | | |
| K | 0.500 | - | 0.700 | | | | |
| L | 0DEG | - | 7DEG | | | | |

The TQFP48 Package is 7 by 7 mm in size and has a 0.5 mm pin pitch.

The TQFP48 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx

***Figure 5.2. TQFP48 PCB Solder Mask***

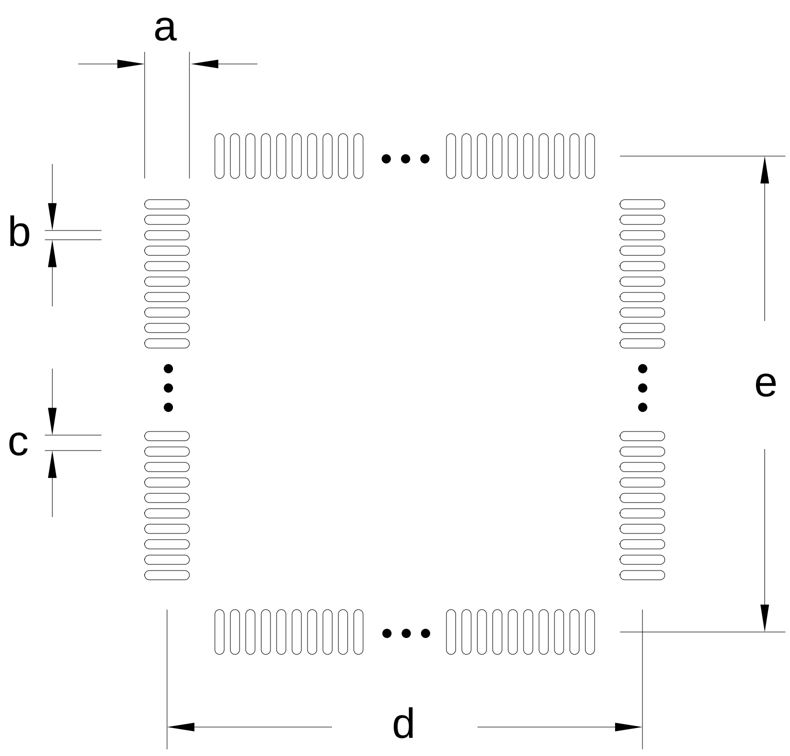



***Table 5.2. QFP48 PCB Solder Mask Dimensions (Dimensions in mm)***

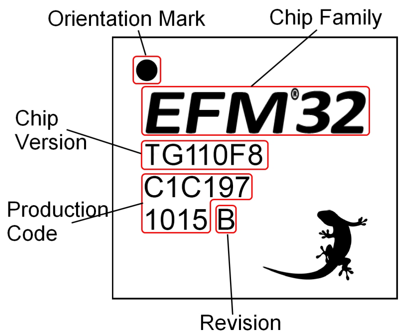
| Symbol | Dim. (mm) |
|---|---|
| a | 1.72 |
| b | 0.42 |
| c | 0.50 |
| d | 8.50 |
| e | 8.50 |

# 6 Chip Marking, Revision and Errata

## 6.1 Chip Marking

In the illustration below package fields and position are shown.

***Figure 6.1. Example Chip Marking (top view)***




## 6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 60) .

## 6.3 Errata

Please see the errata document for EFM32ZG222 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:
http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

# A Disclaimer and Trademarks

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