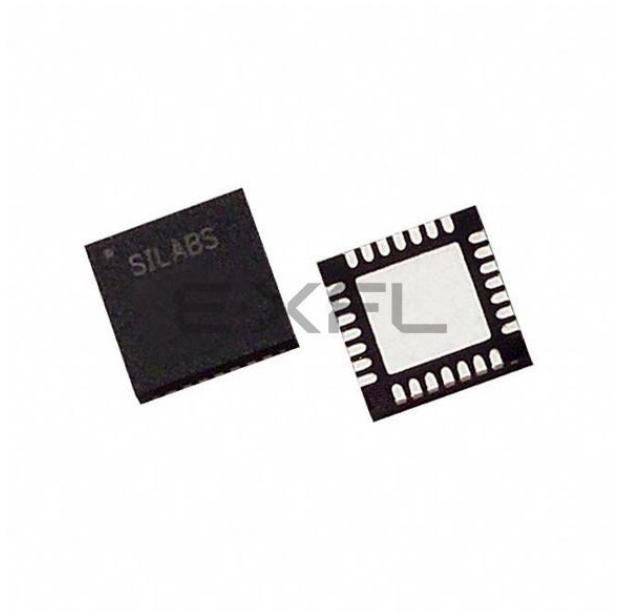


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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 25MHz |
| Connectivity | SMBus (2-Wire/I²C), SPI, UART/USART |
| Peripherals | POR, PWM, Temp Sensor, WDT |
| Number of I/O | 25 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 1.25K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 17x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VFQFN Exposed Pad |
| Supplier Device Package | 28-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/c8051t611-gmr |

# 1. System Overview

C8051T610/1/2/3/4/5/6/7 devices are fully integrated, mixed-signal, system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- C8051F310 ISP Flash device is available for quick in-system code development
- 10-bit 500 ksps Single-ended ADC with analog multiplexer and integrated temperature sensor
- Precision calibrated 24.5 MHz internal oscillator
- 16 k or 8 k of on-chip Byte-Programmable EPROM—(512 bytes are reserved on 16k version)
- 1280 bytes of on-chip RAM
- SMBus/$I^2C$, SPI, and Enhanced UART serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with five capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset and $V_{DD}$ Monitor
- On-chip Voltage Comparators (2)
- 29/25/21 Port I/O

With on-chip power-on reset, $V_{DD}$ monitor, watchdog timer, and clock oscillator, the C8051T610/1/2/3/4/5/6/7 devices are truly stand-alone, system-on-a-chip solutions. User software has complete control of all peripherals and may individually shut down any or all peripherals for power savings.

Code written for the C8051T610/1/2/3/4/5/6/7 family of processors will run on the C8051F310 Mixed-Signal ISP Flash microcontroller, providing a quick, cost-effective way to develop code without requiring special emulator circuitry. The C8051T610/1/2/3/4/5/6/7 processors include Silicon Laboratories' 2-Wire C2 Debug and Programming interface, which allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection of memory, viewing and modification of special function registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 1.8–3.6 V operation over the industrial temperature range (–45 to +85 °C). An internal LDO is used to supply the processor core voltage. The Port I/O and $\overline{RST}$ pins are tolerant of input signals up to 5 V. See Table 2.1 for ordering information. Block diagrams of the devices in the C8051T610/1/2/3/4/5/6/7 family are shown in Figure 1.1, Figure 1.2 and Figure 1.3.

## 5. QFN-28 Package Specifications

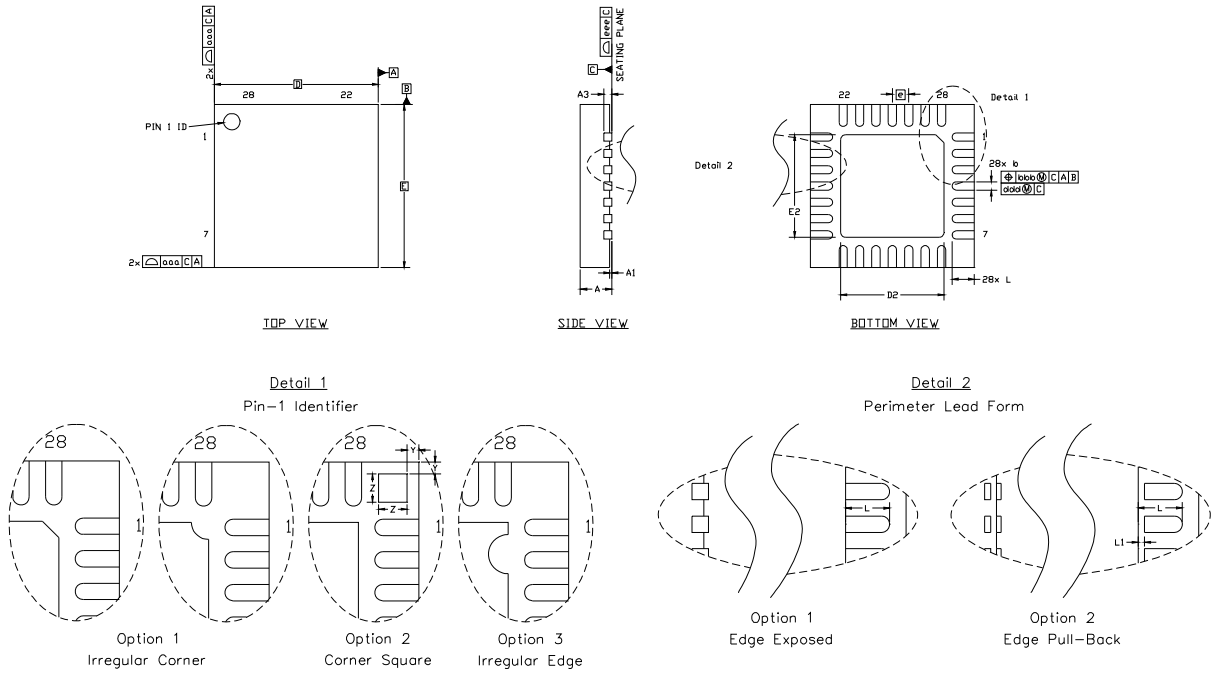


**Figure 5.1. QFN-28 Package Drawing**

**Table 5.1. QFN-28 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.25 REF | |
| b | 0.18 | 0.23 | 0.30 |
| D | | 5.00 BSC. | |
| D2 | 2.90 | 3.15 | 3.35 |
| e | | 0.50 BSC. | |
| E | | 5.00 BSC. | |
| E2 | 2.90 | 3.15 | 3.35 |

| Dimension | Min | Typ | Max |
|---|---|---|---|
| L | 0.35 | 0.55 | 0.65 |
| L1 | 0.00 | — | 0.15 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| Z | | 0.44 | |
| Y | | 0.18 | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 7.2. Electrical Characteristics

### Table 7.2. Global Electrical Characteristics

–40 to +85 °C, 25 MHz system clock unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply Voltage (Note 1) | Regulator in Normal Mode<br>Regulator in Bypass Mode | 1.8<br>1.7 | 3.0<br>1.8 | 3.6<br>1.9 | V<br>V |
| Digital Supply Current with CPU Active | $V_{DD}$ = 1.8 V, Clock = 25 MHz<br>$V_{DD}$ = 1.8 V, Clock = 1 MHz<br>$V_{DD}$ = 3.0 V, Clock = 25 MHz<br>$V_{DD}$ = 3.0 V, Clock = 1 MHz | —<br>—<br>—<br>— | 6.2<br>2.7<br>7<br>2.9 | 8.8<br>—<br>8.9<br>— | mA<br>mA<br>mA<br>mA |
| Digital Supply Current with CPU Inactive (not accessing EPROM) | $V_{DD}$ = 1.8 V, Clock = 25 MHz<br>$V_{DD}$ = 1.8 V, Clock = 1 MHz<br>$V_{DD}$ = 3.0 V, Clock = 25 MHz<br>$V_{DD}$ = 3.0 V, Clock = 1 MHz | —<br>—<br>—<br>— | 2.2<br>0.41<br>2.3<br>0.42 | 3<br>—<br>3.1<br>— | mA<br>mA<br>mA<br>mA |
| Digital Supply Current (shutdown) | Oscillator not running (stop mode), Internal Regulator Off | — | 4 | — | µA |
| | Oscillator not running (stop or suspend mode), Internal Regulator On | — | 400 | — | µA |
| Digital Supply RAM Data Retention Voltage | | — | 1.5 | — | V |
| Specified Operating Temperature Range | | –40 | — | +85 | °C |
| SYSCLK (system clock frequency) | (Note 2) | 0 | — | 25 | MHz |
| Tsysl (SYSCLK low time) | | 18 | — | — | ns |
| Tsysh (SYSCLK high time) | | 18 | — | — | ns |

**Notes:**

1. Analog performance is not guaranteed when $V_{DD}$ is below 1.8 V.
2. SYSCLK must be at least 32 kHz to enable debugging.

## Table 7.3. Port I/O DC Electrical Characteristics

$V_{DD}$ = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

| Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Output High Voltage | $I_{OH}$ = –3 mA, Port I/O push-pull | $V_{DD}$ - 0.2 | — | — | V |
| | $I_{OH}$ = –10 µA, Port I/O push-pull | $V_{DD}$ - 0.1 | — | — | V |
| | $I_{OH}$ = –10 mA, Port I/O push-pull | — | $V_{DD}$ - 0.4 | — | V |
| Output Low Voltage | $I_{OL}$ = 8.5 mA | — | — | 0.4 | V |
| | $I_{OL}$ = 10 µA | — | — | 0.1 | V |
| | $I_{OL}$ = 25 mA | — | 0.6 | — | V |
| Input High Voltage | | 0.7 x $V_{DD}$ | — | — | V |
| Input Low Voltage | | — | — | 0.6 | V |
| Input Leakage Current | Weak Pullup Off | -1 | — | 1 | µA |
| | Weak Pullup On, $V_{IN}$ = 0 V | — | 25 | 50 | µA |

## Table 7.4. Reset Electrical Characteristics

–40 to +85 °C unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $\overline{RST}$ Output Low Voltage | $I_{OL}$ = 8.5 mA, $V_{DD}$ = 1.8 V to 3.6 V | — | — | 0.6 | V |
| $\overline{RST}$ Input High Voltage | | 0.75 x $V_{DD}$ | — | — | V |
| $\overline{RST}$ Input Low Voltage | | — | — | 0.6 | $V_{DD}$ |
| $\overline{RST}$ Input Pullup Current | $\overline{RST}$ = 0.0 V | — | 25 | 50 | µA |
| $V_{DD}$ POR Ramp Time | | — | — | 1 | ms |
| $V_{DD}$ Monitor Threshold ($V_{RST}$) | | 1.7 | 1.75 | 1.8 | V |
| Missing Clock Detector Timeout | Time from last system clock rising edge to reset initiation | 500 | 625 | 750 | µs |
| Reset Time Delay | Delay between release of any reset source and code execution at location 0x0000 | — | — | 60 | µs |
| Minimum $\overline{RST}$ Low Time to Generate a System Reset | | 15 | — | — | µs |
| $V_{DD}$ Monitor Turn-on Time | $V_{DD}$ = $V_{RST}$ - 0.1 V | — | 50 | — | µs |
| $V_{DD}$ Monitor Supply Current | | — | 20 | 30 | µA |

## 8.4. Programmable Window Detector

The ADC Programmable Window Detector continuously compares the ADC0 output registers to user-programmed limits, and notifies the system when a desired condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (AD0WINT in register ADC0CN) can also be used in polled mode. The ADC0 Greater-Than (ADC0GTH, ADC0GTL) and Less-Than (ADC0LTH, ADC0LTL) registers hold the comparison values. The window detector flag can be programmed to indicate when measured data is inside or outside of the user-programmed limits, depending on the contents of the ADC0 Less-Than and ADC0 Greater-Than registers.

### SFR Definition 8.5. ADC0GTH: ADC0 Greater-Than Data High Byte

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADC0GTH[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

SFR Address = 0xC4

| Bit | Name | Function |
|---|---|---|
| 7:0 | ADC0GTH[7:0] | **ADC0 Greater-Than Data Word High-Order Bits.** |

### SFR Definition 8.6. ADC0GTL: ADC0 Greater-Than Data Low Byte

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADC0GTL[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

SFR Address = 0xC3

| Bit | Name | Function |
|---|---|---|
| 7:0 | ADC0GTL[7:0] | **ADC0 Greater-Than Data Word Low-Order Bits.** |

## SFR Definition 8.9. AMX0P: AMUX0 Positive Channel Select

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | | | | AMX0P[4:0] | | | | |
| Type | R | R | R | R/W | | | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

SFR Address = 0xBB

| Bit | Name | Function | | |
|---|---|---|---|---|
| 7:5 | Unused | Unused. Read = 000b; Write = Don't Care. | | |
| 4:0 | AMX0P[4:0] | **AMUX0 Positive Input Selection.** | | |
| | | Setting | Channel | Available on Packages |
| | | 00000: | P1.0 | LQFP-32, QFN-28, QFN-24 |
| | | 00001: | P1.1 | LQFP-32, QFN-28, QFN-24 |
| | | 00010: | P1.2 | LQFP-32, QFN-28, QFN-24 |
| | | 00011: | P1.3 | LQFP-32, QFN-28, QFN-24 |
| | | 00100: | P1.4 | LQFP-32, QFN-28, QFN-24 |
| | | 00101: | P1.5 | LQFP-32, QFN-28, QFN-24 |
| | | 00110: | P1.6 | LQFP-32, QFN-28 |
| | | 00111: | P1.7 | LQFP-32, QFN-28 |
| | | 01000: | P2.0 | LQFP-32, QFN-28, QFN-24 |
| | | 01001: | P2.1 | LQFP-32, QFN-28, QFN-24 |
| | | 01010: | P2.2 | LQFP-32, QFN-28, QFN-24 |
| | | 01011: | P2.3 | LQFP-32, QFN-28, QFN-24 |
| | | 01100: | P2.4 | LQFP-32, QFN-28, QFN-24 |
| | | 01101: | P2.5 | LQFP-32, QFN-28, QFN-24 |
| | | 01110: | P2.6 | LQFP-32, QFN-28 |
| | | 01111: | P2.7 | LQFP-32, QFN-28 |
| | | 10000: | P3.0 | LQFP-32, QFN-28, QFN-24 |
| | | 10001: | P3.1 | LQFP-32 |
| | | 10010: | P3.2 | LQFP-32 |
| | | 10011: | P3.3 | LQFP-32 |
| | | 10100: | P3.4 | LQFP-32 |
| | | 10101-11101: | No Input Selected | N/A |
| | | 11110: | Temp Sensor | LQFP-32, QFN-28, QFN-24 |
| | | 11111: | $V_{DD}$ | LQFP-32, QFN-28, QFN-24 |

## SFR Definition 11.1. REG0CN: Voltage Regulator Control

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STOPCF | BYPASS | | | | | | MPCE |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0xC7

| Bit | Name | Function |
|---|---|---|
| 7 | STOPCF | **Stop Mode Configuration.**<br>This bit configures the regulator's behavior when the device enters STOP mode.<br>0: Regulator is still active in STOP mode. Any enabled reset source will reset the device.<br>1: Regulator is shut down in STOP mode. Only the $\overline{RST}$ pin or power cycle can reset the device. |
| 6 | BYPASS | **Bypass Internal Regulator.**<br>This bit places the regulator in bypass mode, turning off the regulator, and allowing the core to run directly from the $V_{DD}$ supply pin.<br>0: Normal Mode—Regulator is on.<br>1: Bypass Mode—Regulator is off, and the microcontroller core operates directly from the $V_{DD}$ supply voltage.<br>**IMPORTANT: Bypass mode is for use with an external regulator as the supply voltage only. Never place the regulator in bypass mode when the $V_{DD}$ supply voltage is greater than the specifications given in Table 7.1 on page 31. Doing so may cause permanent damage to the device.** |
| 5:1 | Reserved | Reserved. Must Write 00000b. |
| 0 | MPCE | **Memory Power Controller Enable.**<br>This bit can help the system save power at slower system clock frequencies (about 2.0 MHz or less) by automatically shutting down the EPROM memory between clocks when information is not being fetched from the EPROM memory.<br>0: Normal Mode—Memory power controller disabled (EPROM memory is always on).<br>1: Low Power Mode—Memory power controller enabled (EPROM memory turns on/off as needed).<br>**Note:** If an external clock source is used with the Memory Power Controller enabled, and the clock frequency changes from slow (<2.0 MHz) to fast (> 2.0 MHz), the EPROM power will turn on, and up to 20 clocks may be "skipped" to ensure that the EPROM power is stable before reading memory. |

## SFR Definition 16.2. IP: Interrupt Priority

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | | PSPI0 | PT2 | PS0 | PT1 | PX1 | PT0 | PX0 |
| Type | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0xB8; Bit-Addressable

| Bit | Name | Function |
|---|---|---|
| 7 | Unused | Unused. Read = 1, Write = Don't Care. |
| 6 | PSPI0 | **Serial Peripheral Interface (SPI0) Interrupt Priority Control.**<br>This bit sets the priority of the SPI0 interrupt.<br>0: SPI0 interrupt set to low priority level.<br>1: SPI0 interrupt set to high priority level. |
| 5 | PT2 | **Timer 2 Interrupt Priority Control.**<br>This bit sets the priority of the Timer 2 interrupt.<br>0: Timer 2 interrupt set to low priority level.<br>1: Timer 2 interrupt set to high priority level. |
| 4 | PS0 | **UART0 Interrupt Priority Control.**<br>This bit sets the priority of the UART0 interrupt.<br>0: UART0 interrupt set to low priority level.<br>1: UART0 interrupt set to high priority level. |
| 3 | PT1 | **Timer 1 Interrupt Priority Control.**<br>This bit sets the priority of the Timer 1 interrupt.<br>0: Timer 1 interrupt set to low priority level.<br>1: Timer 1 interrupt set to high priority level. |
| 2 | PX1 | **External Interrupt 1 Priority Control.**<br>This bit sets the priority of the External Interrupt 1 interrupt.<br>0: External Interrupt 1 set to low priority level.<br>1: External Interrupt 1 set to high priority level. |
| 1 | PT0 | **Timer 0 Interrupt Priority Control.**<br>This bit sets the priority of the Timer 0 interrupt.<br>0: Timer 0 interrupt set to low priority level.<br>1: Timer 0 interrupt set to high priority level. |
| 0 | PX0 | **External Interrupt 0 Priority Control.**<br>This bit sets the priority of the External Interrupt 0 interrupt.<br>0: External Interrupt 0 set to low priority level.<br>1: External Interrupt 0 set to high priority level. |

## 16.3. External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$

The $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ external interrupt sources are configurable as active high or low, edge or level sensitive. The IN0PL ($\overline{\text{INT0}}$ Polarity) and IN1PL ($\overline{\text{INT1}}$ Polarity) bits in the IT01CF register select active high or active low; the IT0 and IT1 bits in TCON (Section “25.1. Timer 0 and Timer 1” on page 172) select level or edge sensitive. The table below lists the possible configurations.

| IT0 | IN0PL | /INT0 Interrupt |
|---|---|---|
| 1 | 0 | Active low, edge sensitive |
| 1 | 1 | Active high, edge sensitive |
| 0 | 0 | Active low, level sensitive |
| 0 | 1 | Active high, level sensitive |

| IT1 | IN1PL | /INT1 Interrupt |
|---|---|---|
| 1 | 0 | Active low, edge sensitive |
| 1 | 1 | Active high, edge sensitive |
| 0 | 0 | Active low, level sensitive |
| 0 | 1 | Active high, level sensitive |

$\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ are assigned to Port pins as defined in the IT01CF register (see SFR Definition 16.5). Note that $\overline{\text{INT0}}$ and $\overline{\text{INT0}}$ Port pin assignments are independent of any Crossbar assignments. $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ will monitor their assigned Port pins without disturbing the peripheral that was assigned the Port pin via the Crossbar. To assign a Port pin only to $\overline{\text{INT0}}$ and/or $\overline{\text{INT1}}$, configure the Crossbar to skip the selected pin(s). This is accomplished by setting the associated bit in register XBR0 (see Section “21.3. Priority Crossbar Decoder” on page 117 for complete details on configuring the Crossbar).

IE0 (TCON.1) and IE1 (TCON.3) serve as the interrupt-pending flags for the $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ external interrupts, respectively. If an $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ external interrupt is configured as edge-sensitive, the corresponding interrupt-pending flag is automatically cleared by the hardware when the CPU vectors to the ISR. When configured as level sensitive, the interrupt-pending flag remains logic 1 while the input is active as defined by the corresponding polarity bit (IN0PL or IN1PL); the flag remains logic 0 while the input is inactive. The external interrupt source must hold the input active until the interrupt request is recognized. It must then deactivate the interrupt request before execution of the ISR completes or another interrupt request will be generated.

## 17.3. Program Memory CRC

A CRC engine is included on-chip which provides a means of verifying EPROM contents once the device has been programmed. The CRC engine is available for EPROM verification even if the device is fully read and write locked, allowing for verification of code contents at any time.

The CRC engine is operated through the C2 debug and programming interface, and performs 16-bit CRCs on individual 256-Byte blocks of program memory, or a 32-bit CRC the entire memory space. To prevent hacking and extrapolation of security-locked source code, the CRC engine will only allow CRCs to be performed on contiguous 256-Byte blocks beginning on 256-Byte boundaries (lowest 8-bits of address are 0x00). For example, the CRC engine can perform a CRC for locations 0x0400 through 0x04FF, but it cannot perform a CRC for locations 0x0401 through 0x0500, or on block sizes smaller or larger than 256 bytes.

### 17.3.1. Performing 32-bit CRCs on Full EPROM Content

A 32-bit CRC on the entire EPROM space is initiated by writing to the CRC1 byte over the C2 interface. The CRC calculation begins at address 0x0000 and ends at the end of user EPROM space. The EPBusy bit in register C2ADD will be set during the CRC operation, and cleared once the operation is complete. The 32-bit results will be available in the CRC3-0 registers. CRC3 is the MSB, and CRC0 is the LSB. The polynomial used for the 32-bit CRC calculation is 0x04C11DB7.

**Note**: If a 16-bit CRC has been performed since the last device reset, a device reset should be initiated before performing a 32-bit CRC operation.

### 17.3.2. Performing 16-bit CRCs on 256-Byte EPROM Blocks

A 16-bit CRC of individual 256-byte blocks of EPROM can be initiated by writing to the CRC0 byte over the C2 interface. The value written to CRC0 is the high byte of the beginning address for the CRC. For example, if CRC0 is written to 0x02, the CRC will be performed on the 256-bytes beginning at address 0x0200, and ending at address 0x2FF. The EPBusy bit in register C2ADD will be set during the CRC operation, and cleared once the operation is complete. The 16-bit results will be available in the CRC1-0 registers. CRC1 is the MSB, and CRC0 is the LSB. The polynomial for the 16-bit CRC calculation is 0x1021

## 19.2. Power-Fail Reset/$V_{DD}$ Monitor

When a power-down transition or power irregularity causes $V_{DD}$ to drop below $V_{RST}$, the power supply monitor will drive the $\overline{RST}$ pin low and hold the CIP-51 in a reset state (see Figure 19.2). When $V_{DD}$ returns to a level above $V_{RST}$, the CIP-51 will be released from the reset state. Note that even though internal data memory contents are not altered by the power-fail reset, it is impossible to determine if $V_{DD}$ dropped below the level required for data retention. If the PORSF flag reads 1, the data may no longer be valid. The $V_{DD}$ monitor is enabled after power-on resets. Its defined state (enabled/disabled) is not altered by any other reset source. For example, if the $V_{DD}$ monitor is disabled by code and a software reset is performed, the $V_{DD}$ monitor will still be disabled after the reset.

**Important Note:** If the $V_{DD}$ monitor is being turned on from a disabled state, it should be enabled before it is selected as a reset source. Selecting the $V_{DD}$ monitor as a reset source before it is enabled and stabilized may cause a system reset. In some applications, this reset may be undesirable. If this is not desirable in the application, a delay should be introduced between enabling the monitor and selecting it as a reset source. The procedure for enabling the $V_{DD}$ monitor and configuring it as a reset source from a disabled state is shown below:

1. Enable the $V_{DD}$ monitor (VDMEN bit in VDM0CN = 1).
2. If necessary, wait for the $V_{DD}$ monitor to stabilize (see Table 7.4 for the $V_{DD}$ Monitor turn-on time).
3. Select the $V_{DD}$ monitor as a reset source (PORSF bit in RSTSRC = 1).

See Figure 19.2 for $V_{DD}$ monitor timing; note that the power-on-reset delay is not incurred after a $V_{DD}$ monitor reset. See Table 7.4 for complete electrical characteristics of the $V_{DD}$ monitor.

## SFR Definition 20.4. OSCXCN: External Oscillator Control

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | | XOSCMD[2:0] | | | | XFCN[2:0] | | |
| Type | R | R/W | | | R | R/W | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0xB1

| Bit | Name | Function |
|---|---|---|
| 7 | Unused | Read = 0b; Write = Don't Care |
| 6:4 | XOSCMD[2:0] | **External Oscillator Mode Select.**<br>00x: External Oscillator circuit off.<br>010: External CMOS Clock Mode.<br>011: External CMOS Clock Mode with divide by 2 stage.<br>100: RC Oscillator Mode with divide by 2 stage.<br>101: Capacitor Oscillator Mode with divide by 2 stage.<br>11x: Reserved. |
| 3 | Unused | Read = 0b; Write = Don't Care |
| 2:0 | XFCN[2:0] | **External Oscillator Frequency Control Bits.**<br>Set according to the desired frequency range for RC mode.<br>Set according to the desired K Factor for C mode. |

| XFCN | RC Mode | C Mode |
|---|---|---|
| 000 | f ≤ 25 kHz | K Factor = 0.87 |
| 001 | 25 kHz < f ≤ 50 kHz | K Factor = 2.6 |
| 010 | 50 kHz < f ≤ 100 kHz | K Factor = 7.7 |
| 011 | 100 kHz < f ≤ 200 kHz | K Factor = 22 |
| 100 | 200 kHz < f ≤ 400 kHz | K Factor = 65 |
| 101 | 400 kHz < f ≤ 800 kHz | K Factor = 180 |
| 110 | 800 kHz < f ≤ 1.6 MHz | K Factor = 664 |
| 111 | 1.6 MHz < f ≤ 3.2 MHz | K Factor = 1590 |

## SFR Definition 21.6. P0SKIP: Port 0 Skip

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | P0SKIP[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0xD4

| Bit | Name | Function |
|---|---|---|
| 7:0 | P0SKIP[7:0] | **Port 0 Crossbar Skip Enable Bits.**<br>These bits select Port 0 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar.<br>0: Corresponding P0.n pin is not skipped by the Crossbar.<br>1: Corresponding P0.n pin is skipped by the Crossbar. |

## SFR Definition 21.7. P1: Port 1

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | P1[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

SFR Address = 0x90; Bit-Addressable

| Bit | Name | Description | Write | Read |
|---|---|---|---|---|
| 7:0 | P1[7:0] | **Port 1 Data.**<br>Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O. | 0: Set output latch to logic LOW.<br>1: Set output latch to logic HIGH. | 0: P1.n Port pin is logic LOW.<br>1: P1.n Port pin is logic HIGH. |
| **Note:** P1.6 and P1.7 are not connected to external pins on the C8051T616/7 devices. | | | | |

## SFR Definition 22.2. SMB0CN: SMBus Control

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASTER | TXMODE | STA | STO | ACKRQ | ARBLOST | ACK | SI |
| Type | R | R | R/W | R/W | R | R | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0xC0; Bit-Addressable

| Bit | Name | Description | Read | Write |
|---|---|---|---|---|
| 7 | MASTER | **SMBus Master/Slave Indicator.** This read-only bit indicates when the SMBus is operating as a master. | 0: SMBus operating in slave mode.<br>1: SMBus operating in master mode. | N/A |
| 6 | TXMODE | **SMBus Transmit Mode Indicator.** This read-only bit indicates when the SMBus is operating as a transmitter. | 0: SMBus in Receiver Mode.<br>1: SMBus in Transmitter Mode. | N/A |
| 5 | STA | **SMBus Start Flag.** | 0: No Start or repeated Start detected.<br>1: Start or repeated Start detected. | 0: No Start generated.<br>1: When Configured as a Master, initiates a START or repeated START. |
| 4 | STO | **SMBus Stop Flag.** | 0: No Stop condition detected.<br>1: Stop condition detected (if in Slave Mode) or pending (if in Master Mode). | 0: No STOP condition is transmitted.<br>1: When configured as a Master, causes a STOP condition to be transmitted after the next ACK cycle.<br>Cleared by Hardware. |
| 3 | ACKRQ | **SMBus Acknowledge Request.** | 0: No Ack requested<br>1: ACK requested | N/A |
| 2 | ARBLOST | **SMBus Arbitration Lost Indicator.** | 0: No arbitration error.<br>1: Arbitration Lost | N/A |
| 1 | ACK | **SMBus Acknowledge.** | 0: NACK received.<br>1: ACK received. | 0: Send NACK<br>1: Send ACK |
| 0 | SI | **SMBus Interrupt Flag.**<br>This bit is set by hardware under the conditions listed in Table 15.3. SI must be cleared by software. While SI is set, SCL is held low and the SMBus is stalled. | 0: No interrupt pending<br>1: Interrupt Pending | 0: Clear interrupt, and initiate next state machine event.<br>1: Force interrupt. |

## SFR Definition 25.1. CKCON: Clock Control

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | T3MH | T3ML | T2MH | T2ML | T1M | T0M | SCA[1:0] | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0x8E

| Bit | Name | Function |
|---|---|---|
| 7 | T3MH | **Timer 3 High Byte Clock Select.**<br>Selects the clock supplied to the Timer 3 high byte (split 8-bit timer mode only).<br>0: Timer 3 high byte uses the clock defined by the T3XCLK bit in TMR3CN.<br>1: Timer 3 high byte uses the system clock. |
| 6 | T3ML | **Timer 3 Low Byte Clock Select.**<br>Selects the clock supplied to Timer 3. Selects the clock supplied to the lower 8-bit timer in split 8-bit timer mode.<br>0: Timer 3 low byte uses the clock defined by the T3XCLK bit in TMR3CN.<br>1: Timer 3 low byte uses the system clock. |
| 5 | T2MH | **Timer 2 High Byte Clock Select.**<br>Selects the clock supplied to the Timer 2 high byte (split 8-bit timer mode only).<br>0: Timer 2 high byte uses the clock defined by the T2XCLK bit in TMR2CN.<br>1: Timer 2 high byte uses the system clock. |
| 4 | T2ML | **Timer 2 Low Byte Clock Select.**<br>Selects the clock supplied to Timer 2. If Timer 2 is configured in split 8-bit timer mode, this bit selects the clock supplied to the lower 8-bit timer.<br>0: Timer 2 low byte uses the clock defined by the T2XCLK bit in TMR2CN.<br>1: Timer 2 low byte uses the system clock. |
| 3 | T1 | **Timer 1 Clock Select.**<br>Selects the clock source supplied to Timer 1. Ignored when C/T1 is set to 1.<br>0: Timer 1 uses the clock defined by the prescale bits SCA[1:0].<br>1: Timer 1 uses the system clock. |
| 2 | T0 | **Timer 0 Clock Select.**<br>Selects the clock source supplied to Timer 0. Ignored when C/T0 is set to 1.<br>0: Counter/Timer 0 uses the clock defined by the prescale bits SCA[1:0].<br>1: Counter/Timer 0 uses the system clock. |
| 1:0 | SCA[1:0] | **Timer 0/1 Prescale Bits.**<br>These bits control the Timer 0/1 Clock Prescaler:<br>00: System clock divided by 12<br>01: System clock divided by 4<br>10: System clock divided by 48<br>11: External clock divided by 8 (synchronized with the system clock) |

## SFR Definition 25.13. TMR3CN: Timer 3 Control

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TF3H | TF3L | TF3LEN | | T3SPLIT | TR3 | | T3XCLK |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0x91; Bit-Addressable

| Bit | Name | Function |
|---|---|---|
| 7 | TF3H | **Timer 3 High Byte Overflow Flag.**<br>Set by hardware when the Timer 3 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 interrupt service routine. This bit is not automatically cleared by hardware. |
| 6 | TF3L | **Timer 3 Low Byte Overflow Flag.**<br>Set by hardware when the Timer 3 low byte overflows from 0xFF to 0x00. TF3L will be set when the low byte overflows regardless of the Timer 3 mode. This bit is not automatically cleared by hardware. |
| 5 | TF3LEN | **Timer 3 Low Byte Interrupt Enable.**<br>When set to 1, this bit enables Timer 3 Low Byte interrupts. If Timer 3 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 3 overflows. |
| 4 | Unused | Unused. Read = 0b; Write = Don't Care |
| 3 | T3SPLIT | **Timer 3 Split Mode Enable.**<br>When this bit is set, Timer 3 operates as two 8-bit timers with auto-reload.<br>0: Timer 3 operates in 16-bit auto-reload mode.<br>1: Timer 3 operates as two 8-bit auto-reload timers. |
| 2 | TR3 | **Timer 3 Run Control.**<br>Timer 3 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR3H only; TMR3L is always enabled in split mode. |
| 1 | Unused | Unused. Read = 0b; Write = Don't Care |
| 0 | T3XCLK | **Timer 3 External Clock Select.**<br>This bit selects the external clock source for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer.<br>0: Timer 3 clock is the system clock divided by 12.<br>1: Timer 3 clock is the external clock divided by 8 (synchronized with SYSCLK). |

## SFR Definition 25.17. TMR3H Timer 3 High Byte

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TMR3H[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0x95

| Bit | Name | Function |
|---|---|---|
| 7:0 | TMR3H[7:0] | **Timer 3 Low Byte.**<br>In 16-bit mode, the TMR3H register contains the high byte of the 16-bit Timer 3. In 8-bit mode, TMR3H contains the 8-bit high byte timer value. |

## SFR Definition 26.3. PCA0CPMn: PCA Capture/Compare Mode

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PWM16n | ECOMn | CAPPn | CAPNn | MATn | TOGn | PWMn | ECCFn |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Addresses: 0xDA (n = 0), 0xDB (n = 1), 0xDC (n = 2), 0xDD (n = 3), 0xDE (n = 4)

| Bit | Name | Function |
|---|---|---|
| 7 | PWM16n | **16-bit Pulse Width Modulation Enable.**<br>This bit enables 16-bit mode when Pulse Width Modulation mode is enabled.<br>0: 8-bit PWM selected.<br>1: 16-bit PWM selected. |
| 6 | ECOMn | **Comparator Function Enable.**<br>This bit enables the comparator function for PCA module n when set to 1. |
| 5 | CAPPn | **Capture Positive Function Enable.**<br>This bit enables the positive edge capture for PCA module n when set to 1. |
| 4 | CAPNn | **Capture Negative Function Enable.**<br>This bit enables the negative edge capture for PCA module n when set to 1. |
| 3 | MATn | **Match Function Enable.**<br>This bit enables the match function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1. |
| 2 | TOGn | **Toggle Function Enable.**<br>This bit enables the toggle function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode. |
| 1 | PWMn | **Pulse Width Modulation Mode Enable.**<br>This bit enables the PWM function for PCA module n when set to 1. When enabled, a pulse width modulated signal is output on the CEXn pin. 8-bit PWM is used if PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode. |
| 0 | ECCFn | **Capture/Compare Flag Interrupt Enable.**<br>This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt.<br>0: Disable CCFn interrupts.<br>1: Enable a Capture/Compare Flag interrupt request when CCFn is set. |
| **Note:** When the WDTE bit is set to 1, the PCA0CPM4 register cannot be modified, and module 4 acts as the watchdog timer. To change the contents of the PCA0CPM4 register or the function of module 4, the Watchdog Timer must be disabled. | | |

## C2 Register Definition 27.12. CRC2: CRC Byte 2

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CRC[23:16] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

C2 Address: 0xAB

| Bit | Name | Function |
|---|---|---|
| 7:0 | CRC[23:16] | **CRC Byte 2.**<br>See Section “17.3. Program Memory CRC” on page 96. |

## C2 Register Definition 27.13. CRC3: CRC Byte 3

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CRC[31:24] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

C2 Address: 0xAC

| Bit | Name | Function |
|---|---|---|
| 7:0 | CRC[31:24] | **CRC Byte 3.**<br>See Section “17.3. Program Memory CRC” on page 96. |

## NOTES: