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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VFQFN Exposed Pad
Supplier Device Package	28-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051t613-gm

C8051T610/1/2/3/4/5/6/7

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2. Ordering Information

Table 2.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	EPROM Memory (Bytes)	RAM (Bytes)	Calibrated Internal 24.5 MHz Oscillator	SMBus/I ² C	Enhanced SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 500ksps ADC	Temperature Sensor	Analog Comparators	Lead-free (RoHS Compliant)	Package
C8051T610-GQ	25	16k*	1280	Y	Y	Y	Y	4	Y	29	Y	Y	2	Y	LQFP-32
C8051T611-GM	25	16k*	1280	Y	Y	Y	Y	4	Y	25	Y	Y	2	Y	QFN-28
C8051T612-GQ	25	8k	1280	Y	Y	Y	Y	4	Y	29	Y	Y	2	Y	LQFP-32
C8051T613-GM	25	8k	1280	Y	Y	Y	Y	4	Y	25	Y	Y	2	Y	QFN-28
C8051T614-GQ	25	8k	1280	Y	Y	Y	Y	4	Y	29	—	—	2	Y	LQFP-32
C8051T615-GM	25	8k	1280	Y	Y	Y	Y	4	Y	25	—	—	2	Y	QFN-28
C8051T616-GM	25	16k*	1280	Y	Y	Y	Y	4	Y	21	Y	Y	2	Y	QFN-24
C8051T617-GM	25	16k*	1280	Y	Y	Y	Y	4	Y	21	—	—	2	Y	QFN-24
* 512 Bytes Reserved for Factory Use															

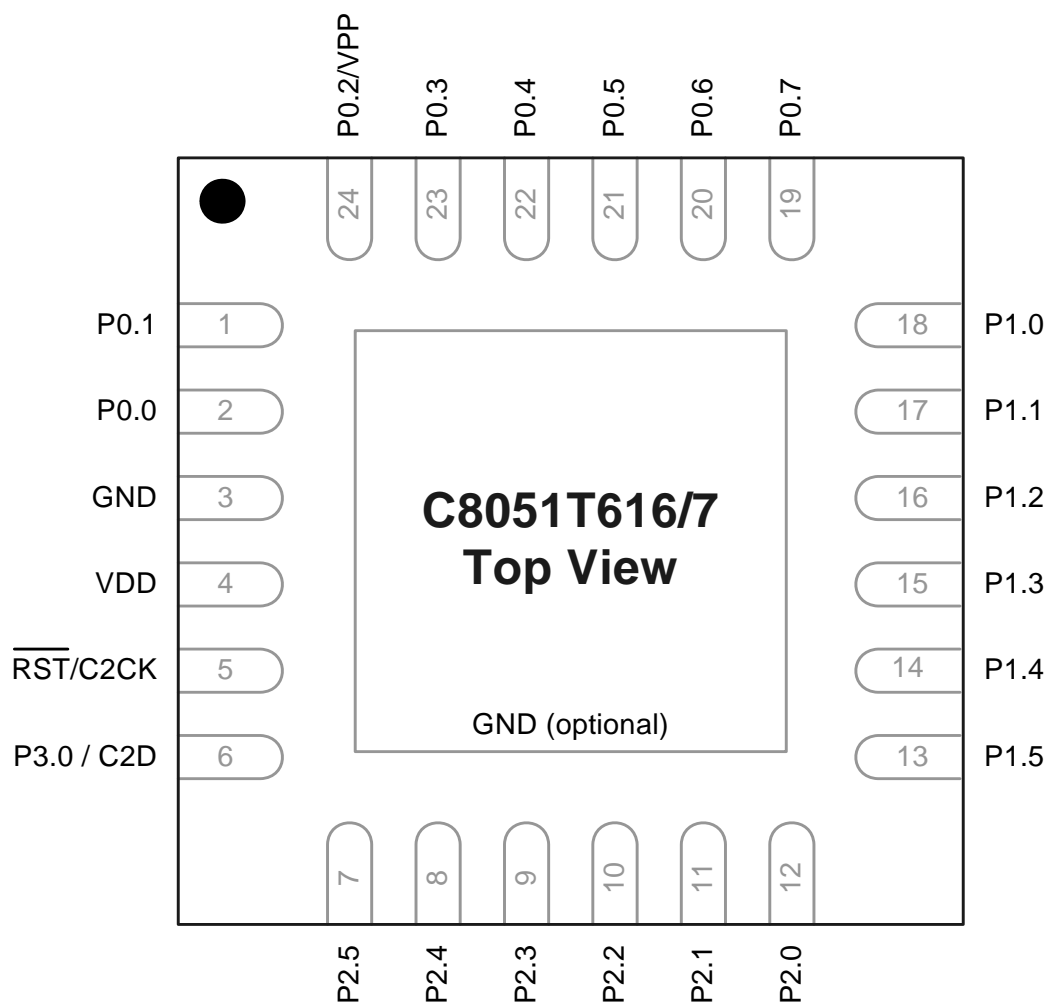


Figure 3.3. QFN-24 Pinout Diagram (Top View)

5. QFN-28 Package Specifications

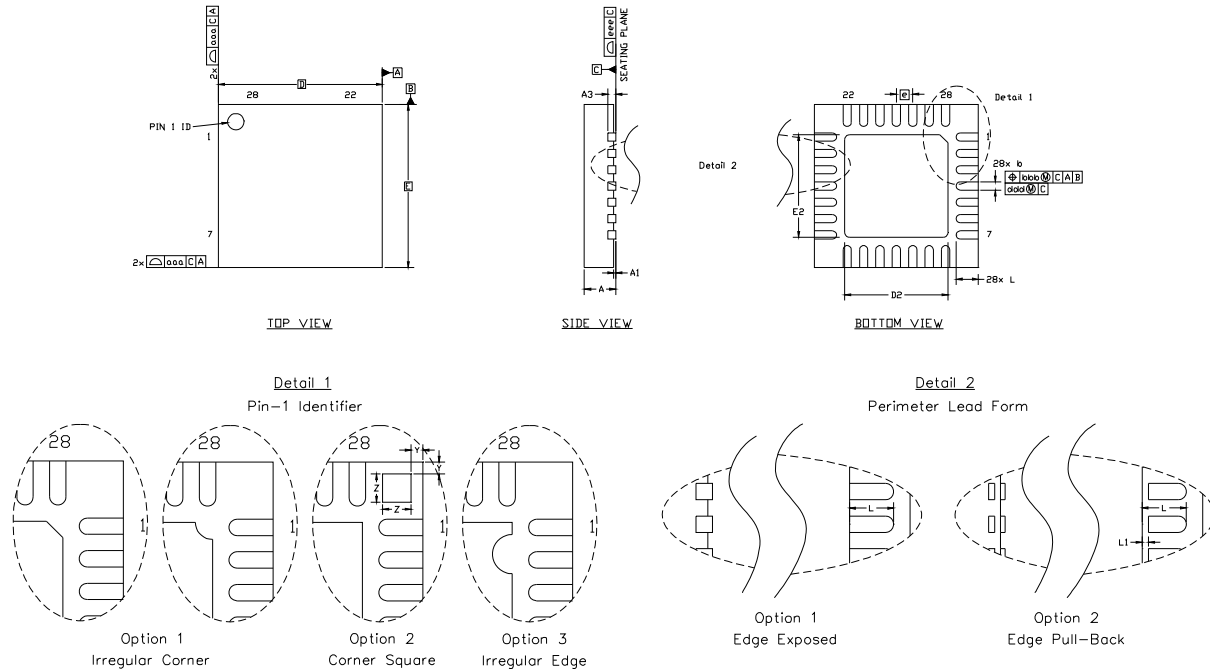


Figure 5.1. QFN-28 Package Drawing

Table 5.1. QFN-28 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.25 REF		
b	0.18	0.23	0.30
D	5.00 BSC.		
D2	2.90	3.15	3.35
e	0.50 BSC.		
E	5.00 BSC.		
E2	2.90	3.15	3.35
L	0.35	0.55	0.65
L1	0.00	—	0.15
aaa	0.15		
bbb	0.10		
ddd	0.05		
eee	0.08		
Z	0.44		
Y	0.18		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Table 7.3. Port I/O DC Electrical Characteristics $V_{DD} = 1.8$ to 3.6 V, -40 to $+85$ °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	Units
Output High Voltage	$I_{OH} = -3$ mA, Port I/O push-pull	$V_{DD} - 0.2$	—	—	V
	$I_{OH} = -10$ μ A, Port I/O push-pull	$V_{DD} - 0.1$	—	—	V
	$I_{OH} = -10$ mA, Port I/O push-pull	—	$V_{DD} - 0.4$	—	V
Output Low Voltage	$I_{OL} = 8.5$ mA	—	—	0.4	V
	$I_{OL} = 10$ μ A	—	—	0.1	V
	$I_{OL} = 25$ mA	—	0.6	—	V
Input High Voltage		$0.7 \times V_{DD}$	—	—	V
Input Low Voltage		—	—	0.6	V
Input Leakage Current	Weak Pullup Off	-1	—	1	μ A
	Weak Pullup On, $V_{IN} = 0$ V	—	25	50	μ A

Table 7.4. Reset Electrical Characteristics -40 to $+85$ °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
RST Output Low Voltage	$I_{OL} = 8.5$ mA, $V_{DD} = 1.8$ V to 3.6 V	—	—	0.6	V
RST Input High Voltage		$0.75 \times V_{DD}$	—	—	V
RST Input Low Voltage		—	—	0.6	V_{DD}
RST Input Pullup Current	$\overline{RST} = 0.0$ V	—	25	50	μ A
V_{DD} POR Ramp Time		—	—	1	ms
V_{DD} Monitor Threshold (V_{RST})		1.7	1.75	1.8	V
Missing Clock Detector Timeout	Time from last system clock rising edge to reset initiation	500	625	750	μ s
Reset Time Delay	Delay between release of any reset source and code execution at location 0x0000	—	—	60	μ s
Minimum \overline{RST} Low Time to Generate a System Reset		15	—	—	μ s
V_{DD} Monitor Turn-on Time	$V_{DD} = V_{RST} - 0.1$ V	—	50	—	μ s
V_{DD} Monitor Supply Current		—	20	30	μ A

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SFR Definition 12.3. CPT1CN: Comparator1 Control

Bit	7	6	5	4	3	2	1	0
Name	CP1EN	CP1OUT	CP1RIF	CP1FIF	CP1HYP[1:0]		CP1HYN[1:0]	
Type	R/W	R	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9A

Bit	Name	Function
7	CP1EN	Comparator1 Enable Bit. 0: Comparator1 Disabled. 1: Comparator1 Enabled.
6	CP1OUT	Comparator1 Output State Flag. 0: Voltage on CP1+ < CP0−. 1: Voltage on CP1+ > CP0−.
5	CP1RIF	Comparator1 Rising-Edge Flag. Must be cleared by software. 0: No Comparator1 Rising Edge has occurred since this flag was last cleared. 1: Comparator1 Rising Edge has occurred.
4	CP1FIF	Comparator1 Falling-Edge Flag. Must be cleared by software. 0: No Comparator1 Falling-Edge has occurred since this flag was last cleared. 1: Comparator1 Falling-Edge has occurred.
3:2	CP1HYP[1:0]	Comparator1 Positive Hysteresis Control Bits. 00: Positive Hysteresis Disabled. 01: Positive Hysteresis = 5 mV. 10: Positive Hysteresis = 10 mV. 11: Positive Hysteresis = 20 mV.
1:0	CP1HYN[1:0]	Comparator1 Negative Hysteresis Control Bits. 00: Negative Hysteresis Disabled. 01: Negative Hysteresis = 5 mV. 10: Negative Hysteresis = 10 mV. 11: Negative Hysteresis = 20 mV.

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SFR Definition 12.5. CPT0MX: Comparator0 MUX Selection

Bit	7	6	5	4	3	2	1	0
Name			CMX0N[1:0]				CMX0P[1:0]	
Type	R	R	R/W		R	R	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9F

Bit	Name	Function
7:6	Unused	Unused, Read = 00b; Write = Don't Care
5:4	CMX0N[1:0]	Comparator0 Negative Input MUX Selection. 00: P1.1 01: P1.5 10: P2.1 11: P2.5
3:2	Unused	Unused, Read = 00b; Write = Don't Care
1:0	CMX0P[1:0]	Comparator0 Positive Input MUX Selection. 00: P1.0 01: P1.4 10: P2.0 11: P2.4

Table 13.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
ANL C, bit	AND direct bit to Carry	2	2
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
JC rel	Jump if Carry is set	2	2/3
JNC rel	Jump if Carry is not set	2	2/3
JB bit, rel	Jump if direct bit is set	3	3/4
JNB bit, rel	Jump if direct bit is not set	3	3/4
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/4
Program Branching			
ACALL addr11	Absolute subroutine call	2	3
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	5
RETI	Return from interrupt	1	5
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
JZ rel	Jump if A equals zero	2	2/3
JNZ rel	Jump if A does not equal zero	2	2/3
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	4/5
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/4
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/4
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/5
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/3
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/4
NOP	No operation	1	1

SFR Definition 16.4. EIP1: Extended Interrupt Priority 1

Bit	7	6	5	4	3	2	1	0
Name	PT3	PCP1	PCP0	PPCA0	PADC0	PWADC0	Reserved	PSMB0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF6

Bit	Name	Function
7	PT3	Timer 3 Interrupt Priority Control. This bit sets the priority of the Timer 3 interrupt. 0: Timer 3 interrupts set to low priority level. 1: Timer 3 interrupts set to high priority level.
6	PCP1	Comparator1 (CP1) Interrupt Priority Control. This bit sets the priority of the CP1 interrupt. 0: CP1 interrupt set to low priority level. 1: CP1 interrupt set to high priority level.
5	PCP0	Comparator0 (CP0) Interrupt Priority Control. This bit sets the priority of the CP0 interrupt. 0: CP0 interrupt set to low priority level. 1: CP0 interrupt set to high priority level.
4	PPCA0	Programmable Counter Array (PCA0) Interrupt Priority Control. This bit sets the priority of the PCA0 interrupt. 0: PCA0 interrupt set to low priority level. 1: PCA0 interrupt set to high priority level.
3	PADC0	ADC0 Conversion Complete Interrupt Priority Control. This bit sets the priority of the ADC0 Conversion Complete interrupt. 0: ADC0 Conversion Complete interrupt set to low priority level. 1: ADC0 Conversion Complete interrupt set to high priority level.
2	PWADC0	ADC0 Window Comparator Interrupt Priority Control. This bit sets the priority of the ADC0 Window interrupt. 0: ADC0 Window interrupt set to low priority level. 1: ADC0 Window interrupt set to high priority level.
1	Reserved	Reserved. Must Write 0.
0	PSMB0	SMBus (SMB0) Interrupt Priority Control. This bit sets the priority of the SMB0 interrupt. 0: SMB0 interrupt set to low priority level. 1: SMB0 interrupt set to high priority level.

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17.1.2. EPROM Read Procedure

1. Reset the device using the /RST pin.
2. Wait at least 20 μ s before sending the first C2 command.
3. Place the device in core reset: Write 0x04 to the DEVCTL register.
4. Write 0x00 to the EPCTL register.
5. Write the first EPROM address for reading to EPADDRH and EPADDRL.
6. Read a data byte from EPDAT. EPADDRH:L will increment by 1 after this read.
7. (Optional) Check the ERROR bit in register EPSTAT and abort the memory read operation if necessary.
8. If reading is not finished, return to Step 6 to read the next address in sequence, or return to Step 5 to select a new address.
9. Remove read mode (1st step): Write 0x40 to the EPCTL register.
10. Remove read mode (2nd step): Write 0x00 to the EPCTL register.
11. Reset the device: Write 0x02 and then 0x00 to the DEVCTL register.

17.2. Security Options

The C8051T610/1/2/3/4/5/6/7 devices provide security options to prevent unauthorized viewing of proprietary program code and constants. A security byte in EPROM address space can be used to lock the program memory from being read or written across the C2 interface. When read, the RDLOCK and WRLOCK bits in register EPSTAT will indicate the lock status of the location currently addressed by EPADDR. Table 17.1 shows the security byte decoding. See Section “14. Memory Organization” on page 77 for the security byte location and EPROM memory map.

Important Note: Once the security byte has been written, there are no means of unlocking the device. Locking memory from write access should be performed only after all other code has been successfully programmed to memory.

Table 17.1. Security Byte Decoding

Bits	Description
7–4	Write Lock: Clearing any of these bits to logic 0 prevents all code memory from being written across the C2 interface.
3–0	Read Lock: Clearing any of these bits to logic 0 prevents all code memory from being read across the C2 interface.

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SFR Definition 20.4. OSCXCN: External Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name		XOSCMD[2:0]				XFCN[2:0]		
Type	R	R/W			R	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB1

Bit	Name	Function																											
7	Unused	Read = 0b; Write = Don't Care																											
6:4	XOSCMD[2:0]	External Oscillator Mode Select. 00x: External Oscillator circuit off. 010: External CMOS Clock Mode. 011: External CMOS Clock Mode with divide by 2 stage. 100: RC Oscillator Mode with divide by 2 stage. 101: Capacitor Oscillator Mode with divide by 2 stage. 11x: Reserved.																											
3	Unused	Read = 0b; Write = Don't Care																											
2:0	XFCN[2:0]	External Oscillator Frequency Control Bits. Set according to the desired frequency range for RC mode. Set according to the desired K Factor for C mode. <table> <tr> <th>XFCN</th><th>RC Mode</th><th>C Mode</th></tr> <tr> <td>000</td><td>$f \leq 25 \text{ kHz}$</td><td>K Factor = 0.87</td></tr> <tr> <td>001</td><td>$25 \text{ kHz} < f \leq 50 \text{ kHz}$</td><td>K Factor = 2.6</td></tr> <tr> <td>010</td><td>$50 \text{ kHz} < f \leq 100 \text{ kHz}$</td><td>K Factor = 7.7</td></tr> <tr> <td>011</td><td>$100 \text{ kHz} < f \leq 200 \text{ kHz}$</td><td>K Factor = 22</td></tr> <tr> <td>100</td><td>$200 \text{ kHz} < f \leq 400 \text{ kHz}$</td><td>K Factor = 65</td></tr> <tr> <td>101</td><td>$400 \text{ kHz} < f \leq 800 \text{ kHz}$</td><td>K Factor = 180</td></tr> <tr> <td>110</td><td>$800 \text{ kHz} < f \leq 1.6 \text{ MHz}$</td><td>K Factor = 664</td></tr> <tr> <td>111</td><td>$1.6 \text{ MHz} < f \leq 3.2 \text{ MHz}$</td><td>K Factor = 1590</td></tr> </table>	XFCN	RC Mode	C Mode	000	$f \leq 25 \text{ kHz}$	K Factor = 0.87	001	$25 \text{ kHz} < f \leq 50 \text{ kHz}$	K Factor = 2.6	010	$50 \text{ kHz} < f \leq 100 \text{ kHz}$	K Factor = 7.7	011	$100 \text{ kHz} < f \leq 200 \text{ kHz}$	K Factor = 22	100	$200 \text{ kHz} < f \leq 400 \text{ kHz}$	K Factor = 65	101	$400 \text{ kHz} < f \leq 800 \text{ kHz}$	K Factor = 180	110	$800 \text{ kHz} < f \leq 1.6 \text{ MHz}$	K Factor = 664	111	$1.6 \text{ MHz} < f \leq 3.2 \text{ MHz}$	K Factor = 1590
XFCN	RC Mode	C Mode																											
000	$f \leq 25 \text{ kHz}$	K Factor = 0.87																											
001	$25 \text{ kHz} < f \leq 50 \text{ kHz}$	K Factor = 2.6																											
010	$50 \text{ kHz} < f \leq 100 \text{ kHz}$	K Factor = 7.7																											
011	$100 \text{ kHz} < f \leq 200 \text{ kHz}$	K Factor = 22																											
100	$200 \text{ kHz} < f \leq 400 \text{ kHz}$	K Factor = 65																											
101	$400 \text{ kHz} < f \leq 800 \text{ kHz}$	K Factor = 180																											
110	$800 \text{ kHz} < f \leq 1.6 \text{ MHz}$	K Factor = 664																											
111	$1.6 \text{ MHz} < f \leq 3.2 \text{ MHz}$	K Factor = 1590																											

SFR Definition 21.2. XBR1: Port I/O Crossbar Register 1

Bit	7	6	5	4	3	2	1	0
Name	WEAKPUD	XBARE	T1E	T0E	ECIE		PCA0ME[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE2

Bit	Name	Function
7	WEAKPUD	Port I/O Weak Pullup Disable. 0: Weak Pullups enabled (except for Ports whose I/O are configured for analog mode). 1: Weak Pullups disabled.
6	XBARE	Crossbar Enable. 0: Crossbar disabled. 1: Crossbar enabled.
5	T1E	T1 Enable. 0: T1 unavailable at Port pin. 1: T1 routed to Port pin.
4	T0E	T0 Enable. 0: T0 unavailable at Port pin. 1: T0 routed to Port pin.
3	ECIE	PCA0 External Counter Input Enable. 0: ECI unavailable at Port pin. 1: ECI routed to Port pin.
2	Unused	Unused. Read = 0b; Write = Don't Care.
1:0	PCA0ME[1:0]	PCA Module I/O Enable Bits. 00: All PCA I/O unavailable at Port pins. 01: CEX0 routed to Port pin. 10: CEX0, CEX1 routed to Port pins. 11: CEX0, CEX1, CEX2 routed to Port pins.

22.5. SMBus Transfer Modes

The SMBus interface may be configured to operate as master and/or slave. At any particular time, it will be operating in one of the following four modes: Master Transmitter, Master Receiver, Slave Transmitter, or Slave Receiver. The SMBus interface enters Master Mode any time a START is generated, and remains in Master Mode until it loses an arbitration or generates a STOP. An SMBus interrupt is generated at the end of all SMBus byte frames. As a receiver, the interrupt for an ACK occurs **before** the ACK. As a transmitter, interrupts occur **after** the ACK.

22.5.1. Write Sequence (Master)

During a write sequence, an SMBus master writes data to a slave device. The master in this transfer will be a transmitter during the address byte, and a transmitter during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 0 (WRITE). The master then transmits one or more bytes of serial data. After each byte is transmitted, an acknowledge bit is generated by the slave. The transfer is ended when the STO bit is set and a STOP is generated. Note that the interface will switch to Master Receiver Mode if SMB0DAT is not written following a Master Transmitter interrupt. Figure 22.5 shows a typical master write sequence. Two transmit data bytes are shown, though any number of bytes may be transmitted. Notice that all of the “data byte transferred” interrupts occur **after** the ACK cycle in this mode.

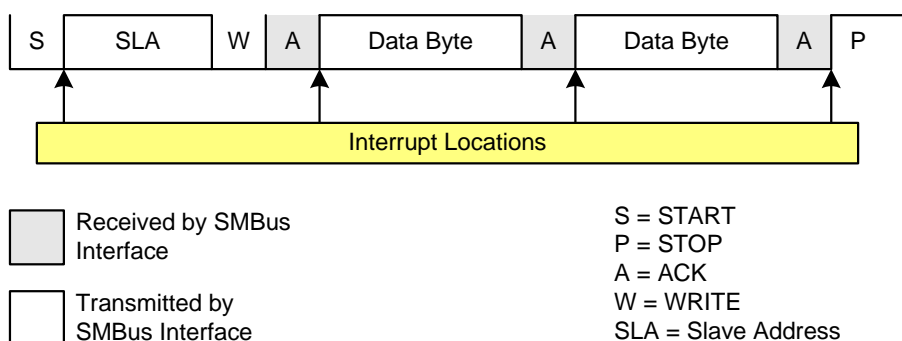


Figure 22.5. Typical Master Write Sequence

24.1. Signal Descriptions

The four signals used by SPI0 (MOSI, MISO, SCK, NSS) are described below.

24.1.1. Master Out, Slave In (MOSI)

The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. This signal is an output when SPI0 is operating as a master and an input when SPI0 is operating as a slave. Data is transferred most-significant bit first. When configured as a master, MOSI is driven by the MSB of the shift register in both 3- and 4-wire mode.

24.1.2. Master In, Slave Out (MISO)

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. This signal is an input when SPI0 is operating as a master and an output when SPI0 is operating as a slave. Data is transferred most-significant bit first. The MISO pin is placed in a high-impedance state when the SPI module is disabled and when the SPI operates in 4-wire mode as a slave that is not selected. When acting as a slave in 3-wire mode, MISO is always driven by the MSB of the shift register.

24.1.3. Serial Clock (SCK)

The serial clock (SCK) signal is an output from the master device and an input to slave devices. It is used to synchronize the transfer of data between the master and slave on the MOSI and MISO lines. SPI0 generates this signal when operating as a master. The SCK signal is ignored by a SPI slave when the slave is not selected (NSS = 1) in 4-wire slave mode.

24.1.4. Slave Select (NSS)

The function of the slave-select (NSS) signal is dependent on the setting of the NSSMD1 and NSSMD0 bits in the SPI0CN register. There are three possible modes that can be selected with these bits:

1. NSSMD[1:0] = 00: 3-Wire Master or 3-Wire Slave Mode: SPI0 operates in 3-wire mode, and NSS is disabled. When operating as a slave device, SPI0 is always selected in 3-wire mode. Since no select signal is present, SPI0 must be the only slave on the bus in 3-wire mode. This is intended for point-to-point communication between a master and one slave.
2. NSSMD[1:0] = 01: 4-Wire Slave or Multi-Master Mode: SPI0 operates in 4-wire mode, and NSS is enabled as an input. When operating as a slave, NSS selects the SPI0 device. When operating as a master, a 1-to-0 transition of the NSS signal disables the master function of SPI0 so that multiple master devices can be used on the same SPI bus.
3. NSSMD[1:0] = 1x: 4-Wire Master Mode: SPI0 operates in 4-wire mode, and NSS is enabled as an output. The setting of NSSMD0 determines what logic level the NSS pin will output. This configuration should only be used when operating SPI0 as a master device.

See Figure 24.2, Figure 24.3, and Figure 24.4 for typical connection diagrams of the various operational modes. **Note that the setting of NSSMD bits affects the pinout of the device.** When in 3-wire master or 3-wire slave mode, the NSS pin will not be mapped by the crossbar. In all other modes, the NSS signal will be mapped to a pin on the device. See Section “21. Port Input/Output” on page 113 for general purpose port I/O and crossbar information.

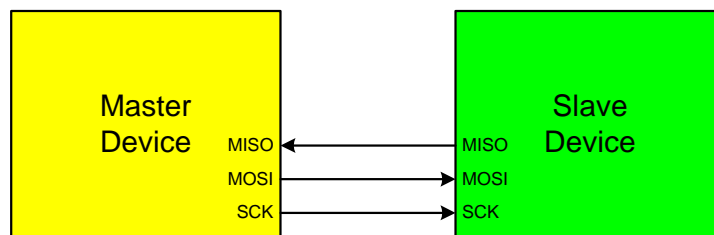


Figure 24.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram

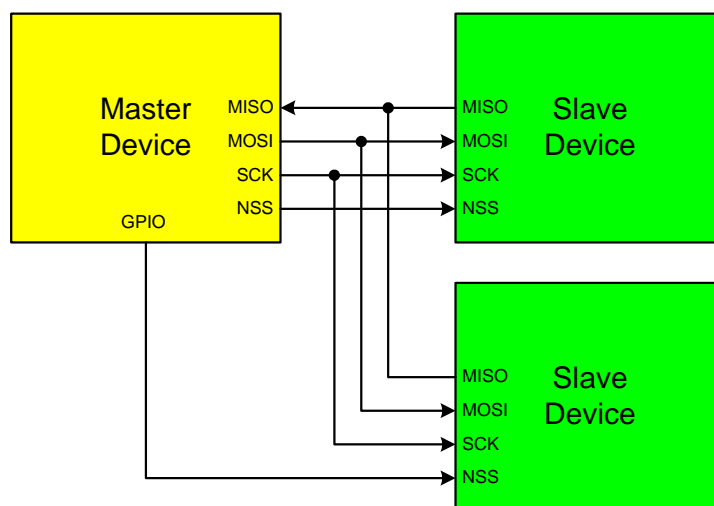


Figure 24.4. 4-Wire Single Master Mode and 4-Wire Slave Mode Connection Diagram

24.3. SPI0 Slave Mode Operation

When SPI0 is enabled and not configured as a master, it will operate as a SPI slave. As a slave, bytes are shifted in through the MOSI pin and out through the MISO pin by a master device controlling the SCK signal. A bit counter in the SPI0 logic counts SCK edges. When 8 bits have been shifted through the shift register, the SPIF flag is set to logic 1, and the byte is copied into the receive buffer. Data is read from the receive buffer by reading SPI0DAT. A slave device cannot initiate transfers. Data to be transferred to the master device is pre-loaded into the shift register by writing to SPI0DAT. Writes to SPI0DAT are double-buffered, and are placed in the transmit buffer first. If the shift register is empty, the contents of the transmit buffer will immediately be transferred into the shift register. When the shift register already contains data, the SPI will load the shift register with the transmit buffer's contents after the last SCK edge of the next (or current) SPI transfer.

When configured as a slave, SPI0 can be configured for 4-wire or 3-wire operation. The default, 4-wire slave mode, is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In 4-wire mode, the NSS signal is routed to a port pin and configured as a digital input. SPI0 is enabled when NSS is logic 0, and disabled when NSS is logic 1. The bit counter is reset on a falling edge of NSS. Note that the NSS signal must be driven low at least 2 system clocks before the first active edge of SCK for each byte transfer. Figure 24.4 shows a connection diagram between two slave devices in 4-wire slave mode and a master device.

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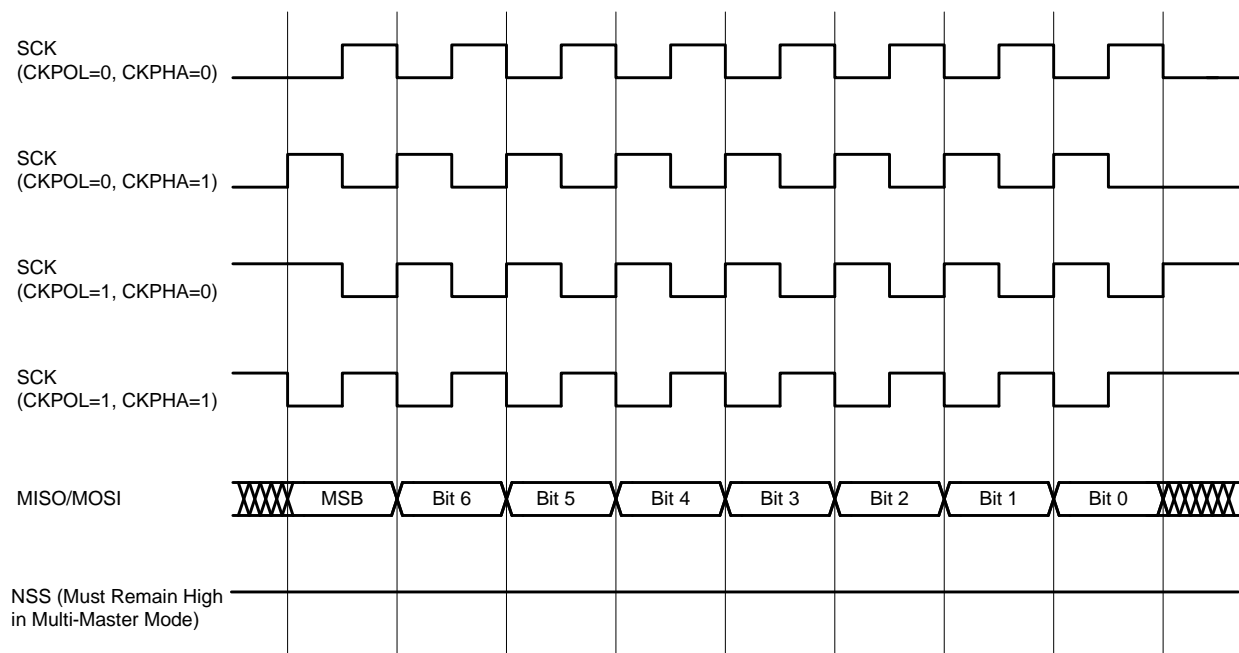


Figure 24.5. Master Mode Data/Clock Timing

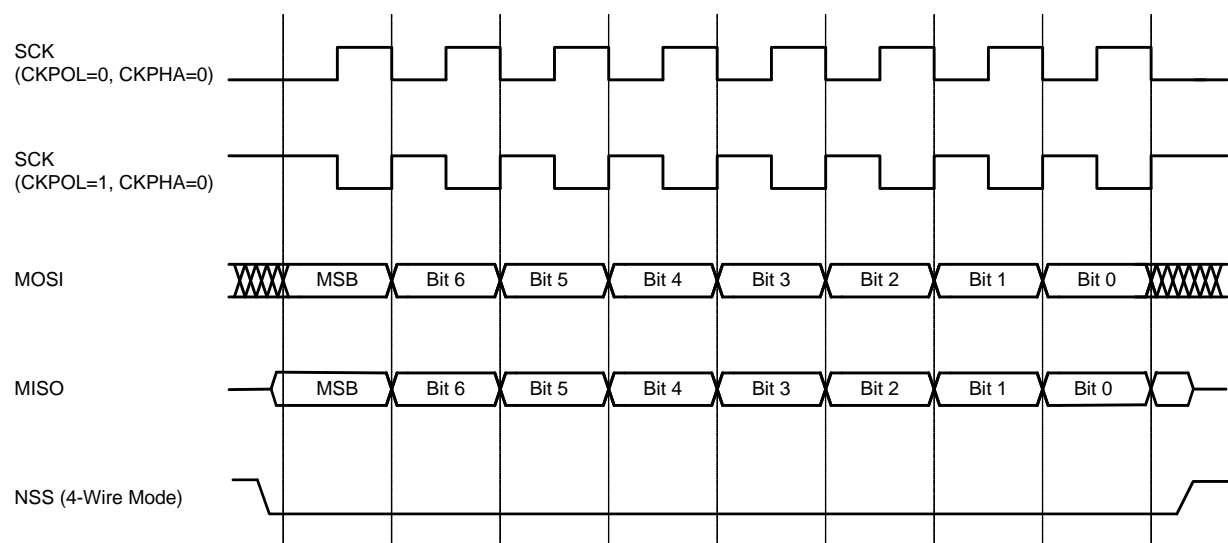


Figure 24.6. Slave Mode Data/Clock Timing (CKPHA = 0)

26.2. PCA0 Interrupt Sources

Figure 26.3 shows a diagram of the PCA interrupt tree. There are six independent event flags that can be used to generate a PCA0 interrupt. They are: the main PCA counter overflow flag (CF), which is set upon a 16-bit overflow of the PCA0 counter and the individual flags for each PCA channel (CCF0, CCF1, CCF2, CCF3, and CCF4), which are set according to the operation mode of that module. These event flags are always set when the trigger condition occurs. Each of these flags can be individually selected to generate a PCA0 interrupt, using the corresponding interrupt enable flag (ECF for CF, and ECCFn for each CCFn). PCA0 interrupts must be globally enabled before any individual interrupt sources are recognized by the processor. PCA0 interrupts are globally enabled by setting the EA bit and the EPCA0 bit to logic 1.

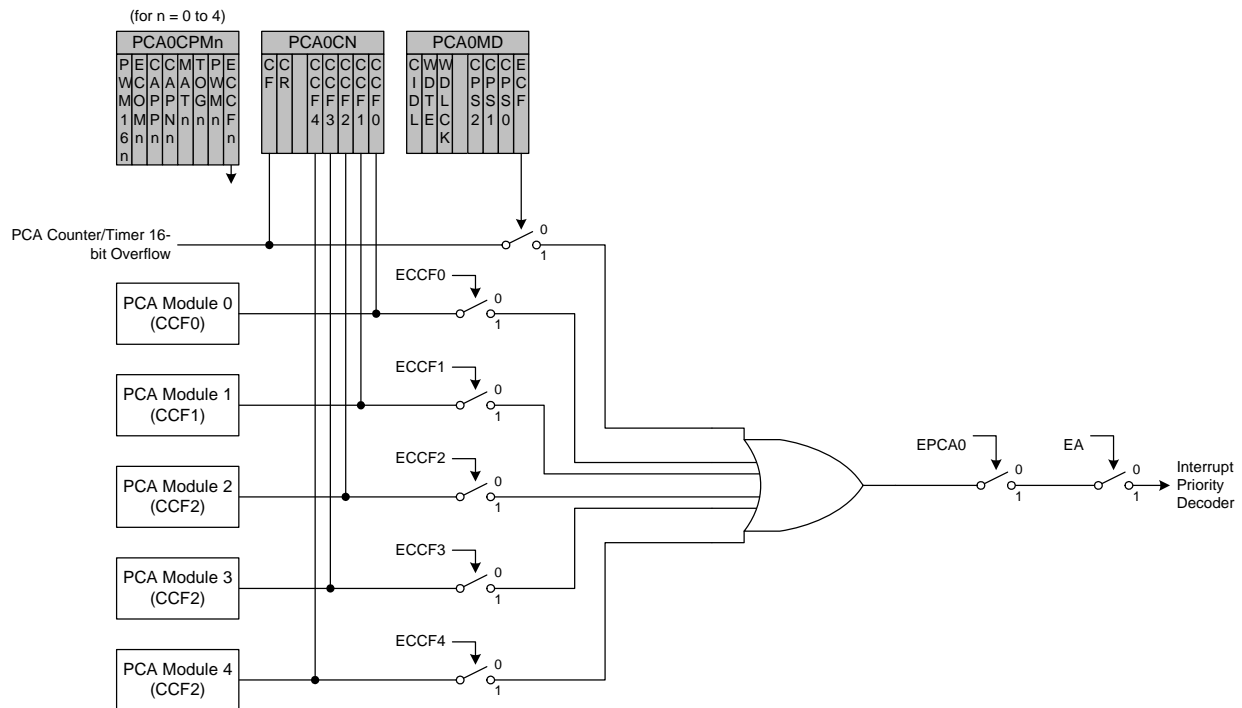


Figure 26.3. PCA Interrupt Block Diagram

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C2 Register Definition 27.6. EPDAT: C2 EPROM Data

Bit	7	6	5	4	3	2	1	0
Name	EPDAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xBF

Bit	Name	Function
7:0	EPDAT[7:0]	C2 EPROM Data Register. This register is used to pass EPROM data during C2 EPROM operations.

C2 Register Definition 27.7. EPSTAT: C2 EPROM Status

Bit	7	6	5	4	3	2	1	0
Name	WRLOCK	RDLOCK						ERROR
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xB7

Bit	Name	Function
7	WRLOCK	Write Lock Indicator. Set to 1 if EPADDR currently points to a write-locked address.
6	RDLOCK	Read Lock Indicator. Set to 1 if EPADDR currently points to a read-locked address.
5:1	Unused	Unused. Read = 00000b; Write = don't care.
0	ERROR	Error Indicator. Set to 1 if last EPROM read or write operation failed due to a security restriction.

C2 Register Definition 27.8. EPADDRH: C2 EPROM Address High Byte

Bit	7	6	5	4	3	2	1	0
Name	EPADDR[15:8]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xAF

Bit	Name	Function
7:0	EPADDR[15:8]	C2 EPROM Address High Byte. This register is used to set the EPROM address location during C2 EPROM operations.

C2 Register Definition 27.9. EPADDRL: C2 EPROM Address Low Byte

Bit	7	6	5	4	3	2	1	0
Name	EPADDR[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xAE

Bit	Name	Function
7:0	EPADDR[7:0]	C2 EPROM Address Low Byte. This register is used to set the EPROM address location during C2 EPROM operations.

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NOTES: