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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c22213-24lfi

processor. The CPU utilizes an interrupt controller with 10 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

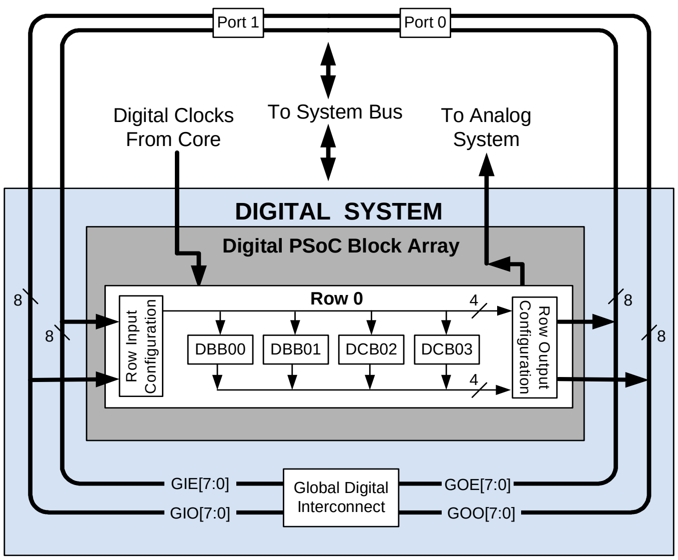
Memory encompasses 2 KB of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of 4 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.



Digital System Block Diagram

Digital peripheral configurations include those listed below.

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8-bit with selectable parity (up to 1)
- SPI master and slave (up to 1)
- I2C slave and master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to 1)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

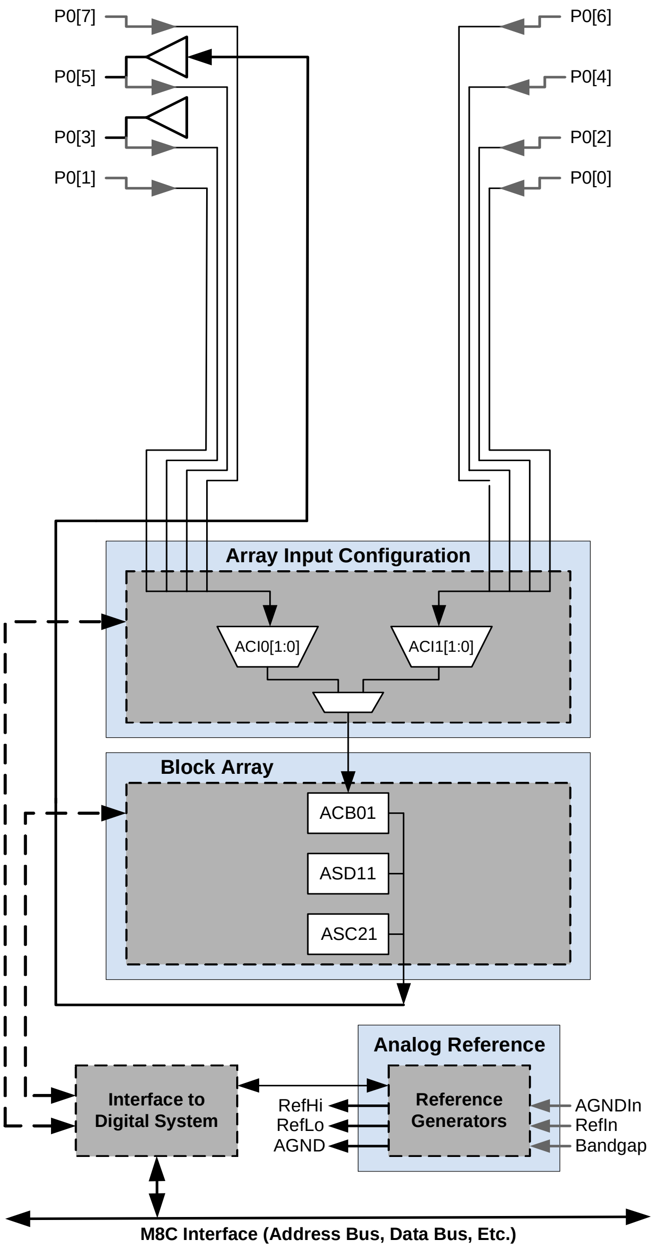
Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled "PSoC Device Characteristics" on page 3.

The Analog System

The Analog System is composed of 3 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (one with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (two pole band-pass, low-pass, and notch)
- Amplifiers (one with selectable gain to 48x)
- Comparators (one with 16 selectable thresholds)
- DACs (one with 6- to 9-bit resolution)
- Multiplying DACs (one with 6- to 9-bit resolution)
- High current output drivers (one with 30 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks. The number of blocks is dependant on the device family which is detailed in the table titled "PSoC Device Characteristics" on page 3.



Analog System Block Diagram

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a decimator, low voltage detection, and power on reset. Brief statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

PSoC Device Characteristics

PSoC Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks
CY8C29x66	up to 64	4	16	12	4	4	12
CY8C27x66	up to 44	2	8	12	4	4	12
CY8C27x43	up to 44	2	8	12	4	4	12
CY8C24x23	up to 24	1	4	12	2	2	6
CY8C22x13	**up to 16**	**1**	**4**	**8**	**1**	**1**	**3**

Getting Started

The quickest path to understanding the PSoC silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, reference the *PSoC™ Mixed Signal Array Technical Reference Manual*.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest PSoC device data sheets on the web at http://www.cypress.com/psoc.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store at http://www.onfulfillment.com/cypressstore/ contains development kits, C compilers, and all accessories for PSoC development. Click on *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Tele-Training

Free PSoC "Tele-training" is available for beginners and taught by a live marketing or application engineer over the phone. Five training classes are available to accelerate the learning curve including introduction, designing, debugging, advanced design, advanced analog, as well as application-specific classes covering topics like PSoC and the LIN bus. For days and times of the tele-training, see http://www.cypress.com/support/training.cfm.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant, go to the following Cypress support web site: http://www.cypress.com/support/cypros.cfm.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at http://www.cypress.com/support/login.cfm.

Application Notes

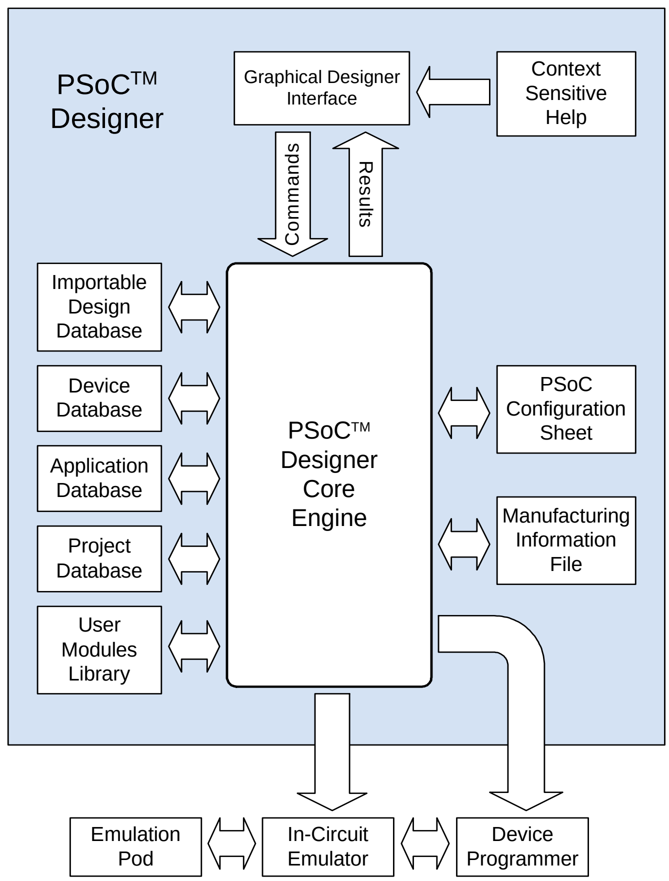
A long list of application notes will assist you in every aspect of your design effort. To locate the PSoC application notes, go to http://www.cypress.com/design/results.cfm.

Development Tools

The Cypress MicroSystems PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows 98, Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP. (Reference the PSoC Designer Functional Flow diagram below.)

PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.



PSoC Designer Subsystems

PSoC Designer Software Subsystems

Device Editor

The Device Editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

PSoC Designer sets up power-on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It's also possible to change the selected components and regenerate the framework.

Design Browser

The Design Browser allows users to select and import preconfigured designs into the user's project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Examples provided in the tools include a 300-baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports Cypress MicroSystems' PSoC family devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the parallel or USB port. The base unit is universal and will operate with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

PSoC Development Tool Kit

1. Pin Information

This chapter describes, lists, and illustrates the CY8C22x13 PSoC device pins and pinout configurations.

1.1 Pinouts

The CY8C22x13 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital IO. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

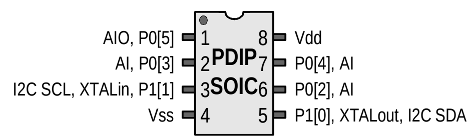
1.1.1 8-Pin Part Pinout

Table 1-1. 8-Pin Part Pinout (PDIP, SOIC)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	IO	P0[5]	Analog column mux input and column output.
2	IO	I	P0[3]	Analog column mux input.
3	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
4	Power		Vss	Ground connection.
5	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
6	IO	I	P0[2]	Analog column mux input.
7	IO	I	P0[4]	Analog column mux input.
8	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

CY8C22113 8-Pin PSoC Device



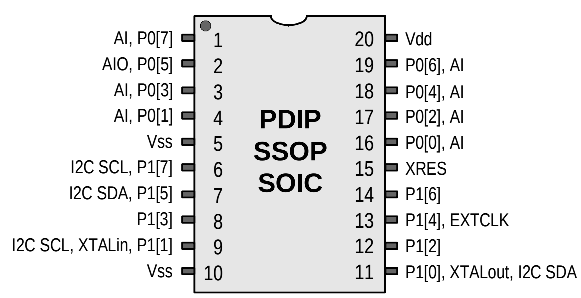
1.1.2 20-Pin Part Pinout

Table 1-2. 20-Pin Part Pinout (PDIP, SSOP, SOIC)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog column mux input.
2	IO	IO	P0[5]	Analog column mux input and column output.
3	IO	I	P0[3]	Analog column mux input.
4	IO	I	P0[1]	Analog column mux input.
5	Power		Vss	Ground connection.
6	IO		P1[7]	I2C Serial Clock (SCL)
7	IO		P1[5]	I2C Serial Data (SDA)
8	IO		P1[3]	
9	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
10	Power		Vss	Ground connection.
11	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
12	IO		P1[2]	
13	IO		P1[4]	Optional External Clock Input (EXTCLK)
14	IO		P1[6]	
15	Input		XRES	Active high external reset with internal pull down.
16	IO	I	P0[0]	Analog column mux input.
17	IO	I	P0[2]	Analog column mux input.
18	IO	I	P0[4]	Analog column mux input.
19	IO	I	P0[6]	Analog column mux input.
20	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

CY8C22213 20-Pin PSoC Device



2. Register Reference

This chapter lists the registers of the CY8C22x13 PSoC device by way of mapping tables, in offset order. For detailed register information, reference the *PSoC™ Mixed Signal Array Technical Reference Manual*.

2.1 Register Conventions

2.1.1 Abbreviations Used

The register conventions specific to this section are listed in the following table.

Convention	Description
RW	Read and write register or bit(s)
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

2.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is also referred to as IO space and is broken into two parts. The XOI bit in the Flag register determines which bank the user is currently in. When the XOI bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40			80			C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8			E8	
DCB02DR1	29	W		69			A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#		6C			AC			EC	
DCB03DR1	2D	W		6D			AD			ED	
DCB03DR2	2E	RW		6E			AE			EE	
DCB03CR0	2F	#		6F			AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32			72		RDI0IS	B2	RW		F2	
	33			73		RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDIOLT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW		D6	
	17			57		ASC21CR3	97	RW		D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32			72		RDI0IS	B2	RW		F2	
	33			73		RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDIOLT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

3. Electrical Specifications

This chapter presents the DC and AC electrical specifications of the CY8C22x13 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by referencing the web at http://www.cypress.com/psoc.

Specifications are valid for $-40^oC \le T_A \le 85^oC$ and $T_J \le 100^oC$ as specified, except where noted. Specifications for devices running at greater than 12 MHz are valid for $-40^oC \le T_A \le 70^oC$ and $T_J \le 82^oC$.

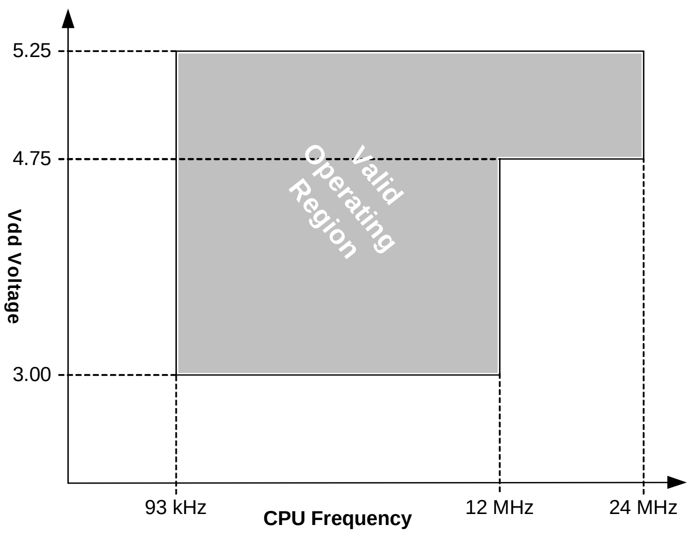


Figure 3-1. Voltage versus Operating Frequency

The following table lists the units of measure that are used in this chapter.

Table 3-1: Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
^oC	degree Celsius	µW	micro watts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nano ampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	pico ampere
MΩ	megaohm	pF	pico farad
µA	micro ampere	pp	peak-to-peak
µF	micro farad	ppm	parts per million
µH	micro henry	ps	picosecond
µs	microsecond	sps	samples per second
µV	micro volts	σ	sigma: one standard deviation
µVrms	micro volts root-mean-square	V	volts

3.3 DC Electrical Characteristics

3.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-4. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	3.00	–	5.25	V	
I_{DD}	Supply Current	–	5	8	mA	Conditions are Vdd = 5.0V, 25 ^oC, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DD3}	Supply Current	–	3.3	6.0	mA	Conditions are Vdd = 3.3V, T_A = 25 ^oC, CPU = 3 MHz, 48 MHz = Disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[a]	–	3	6.5	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, -40 ^oC <= T_A <= 55 ^oC.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[a]	–	4	25	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55 ^oC < T_A <= 85 ^oC.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal.[a]	–	4	7.5	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3V, -40 ^oC <= T_A <= 55 ^oC.
I_{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature.[a]	–	5	26	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3V, 55 ^oC < T_A <= 85 ^oC.
V_{REF}	Reference Voltage (Bandgap)	1.275	1.3	1.325	V	Trimmed for appropriate Vdd.

a. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

3.3.2 DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-5. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (80 mA maximum combined IOH budget)
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (150 mA maximum combined IOL budget)
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25^oC.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25^oC.

3.3.3 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-6. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Low Power	–	1.6	10	mV	
	Input Offset Voltage (absolute value) Mid Power	–	1.3	8	mV	
	Input Offset Voltage (absolute value) High Power	–	1.2	7.5	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.0	–	Vdd	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
	Common Mode Voltage Range (high power or high opamp bias)	0.5	–	Vdd - 0.5		
G_{OLOA}	Open Loop Gain		–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Low	60				
	Power = Medium	60				
	Power = High	80				
$V_{OHIGHOA}$	High Output Voltage Swing (worst case internal load)					
	Power = Low	Vdd - 0.2	–	–	V	
	Power = Medium	Vdd - 0.2	–	–	V	
	Power = High	Vdd - 0.5	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (worst case internal load)					
	Power = Low	–	–	0.2	V	
	Power = Medium	–	–	0.2	V	
	Power = High	–	–	0.5	V	
I_{SOA}	Supply Current (including associated AGND buffer)					
	Power = Low	–	150	200	µA	
	Power = Low, Opamp Bias = High	–	300	400	µA	
	Power = Medium	–	600	800	µA	
	Power = Medium, Opamp Bias = High	–	1200	1600	µA	
	Power = High	–	2400	3200	µA	
	Power = High, Opamp Bias = High	–	4600	6400	µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	60	–	–	dB	

3.3.8 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-14. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[a]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (and so forth to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

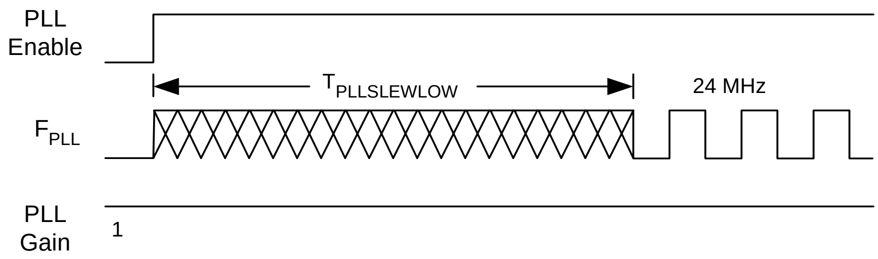


Figure 3-3. PLL Lock for Low Gain Setting Timing Diagram

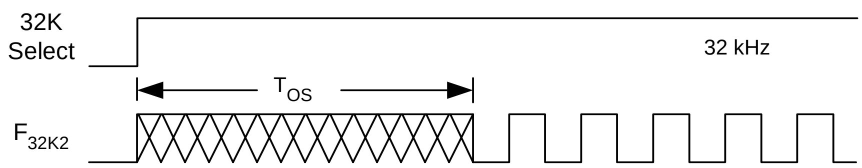


Figure 3-4. External Crystal Oscillator Startup Timing Diagram

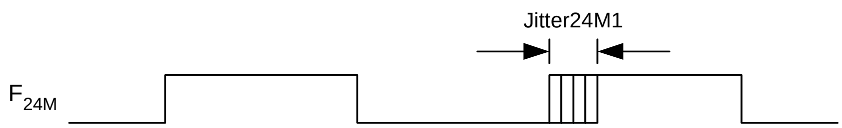


Figure 3-5. 24 MHz Period Jitter (IMO) Timing Diagram

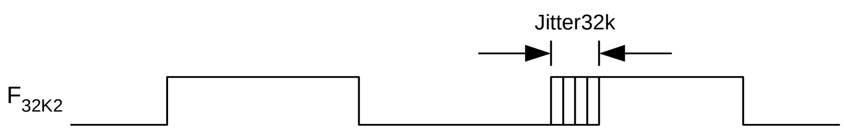


Figure 3-6. 32 kHz Period Jitter (ECO) Timing Diagram

3.4.2 AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-16. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

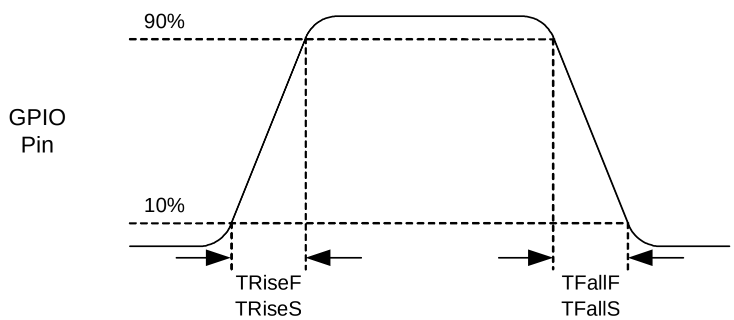


Figure 3-7. GPIO Timing Diagram

3.4.3 AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Note Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 3-17. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	3.9	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
	Power = High	–			µs	
	Power = High, Opamp Bias = High	–	–	0.62	µs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	5.9	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.92	µs	
	Power = High	–			µs	
	Power = High, Opamp Bias = High	–	–	0.72	µs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.15	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	1.7	–		V/µs	
	Power = High				V/µs	
	Power = High, Opamp Bias = High	6.5	–		V/µs	
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.01	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	0.5	–		V/µs	
	Power = High				V/µs	
	Power = High, Opamp Bias = High	4.0	–		V/µs	
BW_{OA}	Gain Bandwidth Product					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.75	–		MHz	
	Power = Low, Opamp Bias = High				MHz	
	Power = Medium				MHz	
	Power = Medium, Opamp Bias = High	3.1	–		MHz	
	Power = High				MHz	
	Power = High, Opamp Bias = High	5.4	–		MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	200	–	nV/rt-Hz	

4. Packaging Information

This chapter illustrates the packaging specifications for the CY8C22x13 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

4.1 Packaging Dimensions

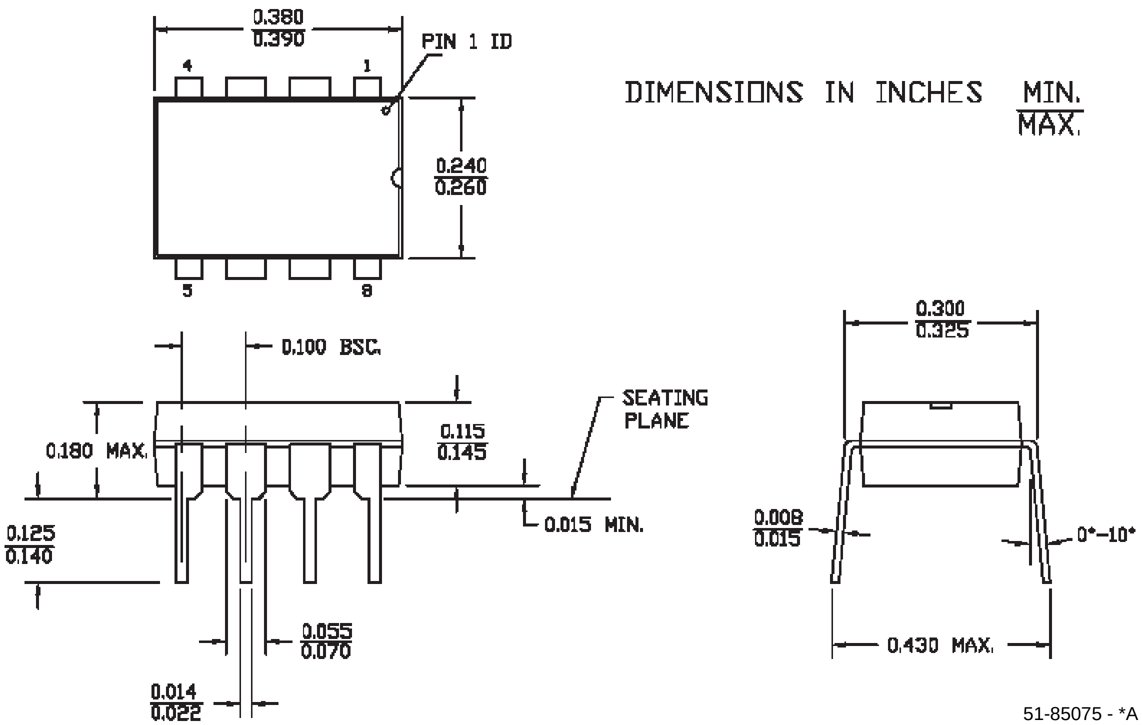


Figure 4-1. 8-Lead (300-Mil) PDIP

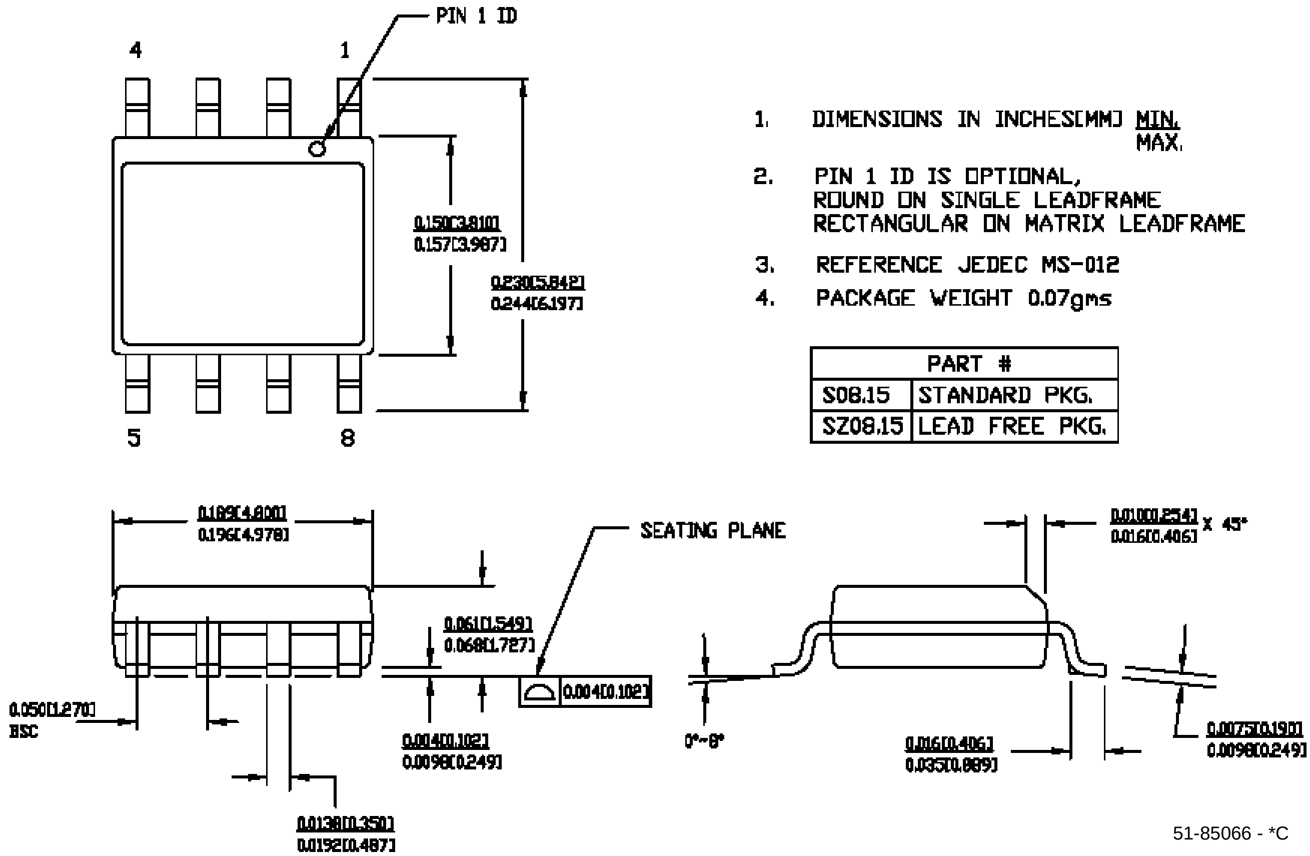


Figure 4-2. 8-Lead (150-Mil) SOIC

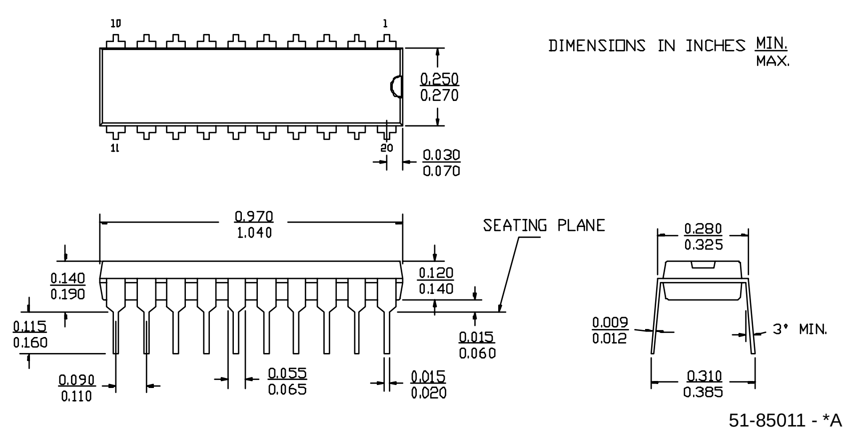


Figure 4-3. 20-Lead (300-Mil) Molded DIP

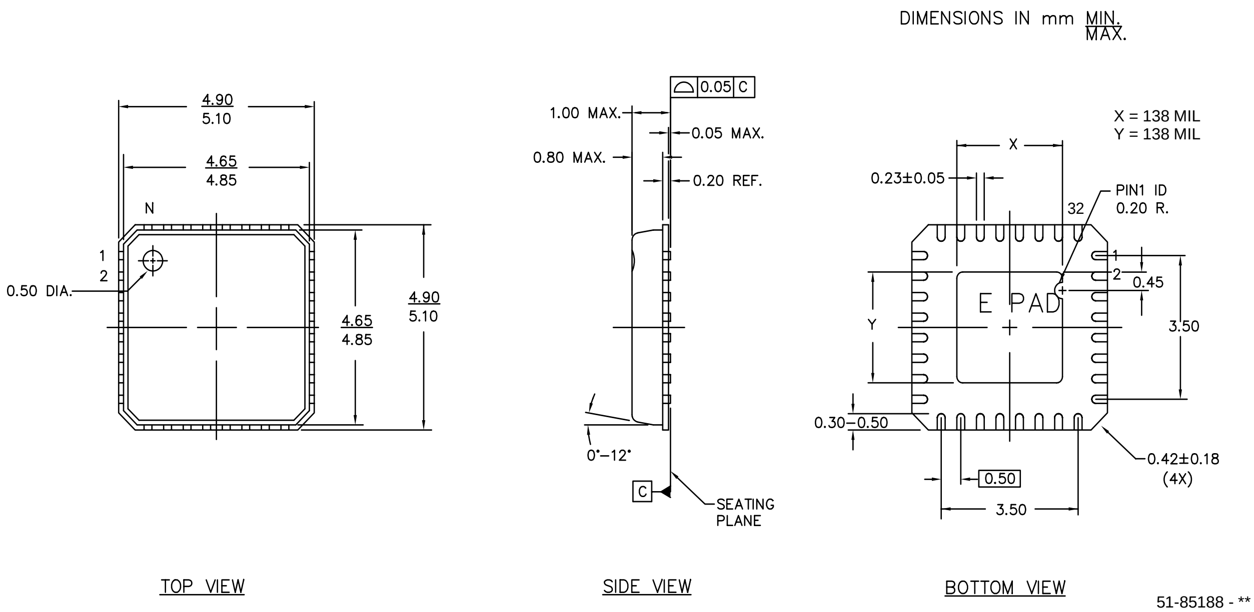


Figure 4-6. 32-Lead (5x5 mm) MLF

4.2 Thermal Impedances

Table 4-1. Thermal Impedances per Package

Package	Typical θ_{JA} *
8 PDIP	123 $^oC/W$
8 SOIC	185 $^oC/W$
20 PDIP	109 $^oC/W$
20 SSOP	117 $^oC/W$
20 SOIC	81 $^oC/W$
32 MLF	22 $^oC/W$

* $T_J = T_A$ + POWER x θ_{JA}

4.3 Capacitance on Crystal Pins

Table 4-2: Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
8 PDIP	2.8 pF
8 SOIC	2.0 pF
20 PDIP	3.0 pF
20 SSOP	2.6 pF
20 SOIC	2.5 pF
32 MLF	2.0 pF

5. Ordering Information

The following table lists the CY8C22x13 PSoC Device family's key package features and ordering codes.

Table 5-1. CY8C22x13 PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
8 Pin (300 Mil) DIP	CY8C22113-24PI	2	256	No	-40C to +85C	4	3	6	4	1	No
8 Pin (150 Mil) SOIC	CY8C22113-24SI	2	256	No	-40C to +85C	4	3	6	4	1	No
8 Pin (150 Mil) SOIC (Tape and Reel)	CY8C22113-24SIT	2	256	No	-40C to +85C	4	3	6	4	1	No
20 Pin (300 Mil) DIP	CY8C22213-24PI	2	256	No	-40C to +85C	4	3	16	8	1	Yes
20 Pin (210 Mil) SSOP	CY8C22213-24PVI	2	256	No	-40C to +85C	4	3	16	8	1	Yes
20 Pin (210 Mil) SSOP (Tape and Reel)	CY8C22213-24PVIT	2	256	No	-40C to +85C	4	3	16	8	1	Yes
20 Pin (300 Mil) SOIC	CY8C22213-24SI	2	256	No	-40C to +85C	4	3	16	8	1	Yes
20 Pin (300 Mil) SOIC (Tape and Reel)	CY8C22213-24SIT	2	256	No	-40C to +85C	4	3	16	8	1	Yes
32 Pin (5x5 mm) MLF	CY8C22213-24LFI	2	256	No	-40C to +85C	4	3	16	8	1	Yes

5.1 Ordering Code Definitions

CY 8 C 22 xxx-SPxx

Package Type:
- P = PDIP
- S = SOIC
- PV = SSOP
- LF = MLF
- A = TQFP

Thermal Rating:
- C = Commercial
- I = Industrial
- E = Extended

Speed: 24 MHz

Part Number

Family Code

Technology Code: C = CMOS

Marketing Code: 8 = Cypress MicroSystems

Company ID: CY = Cypress

6. Sales and Company Information

To obtain information about Cypress MicroSystems or PSoC sales and technical support, reference the following information or go to the section titled "Getting Started" on page 4 in this document.

Cypress MicroSystems
2700 162nd Street SW
Building D
Lynnwood, WA 98037

Phone: 800.669.0557
Facsimile: 425.787.4641

Web Sites: Company Information – http://www.cypress.com
Sales – http://www.cypress.com/aboutus/sales_locations.cfm
Technical Support – http://www.cypress.com/support/login.cfm

6.1 Revision History

Table 6-1. CY8C22x13 Data Sheet Revision History

Document Title: CY8C22113 and CY8C22213 PSoC Mixed Signal Array Final Data Sheet
Document Number: 38-12009

Revision	ECN #	Issue Date	Origin of Change	Description of Change
**	128180	06/30/2003	New Silicon.	New document – Advanced Data Sheet (two page product brief).
*A	129202	09/16/2003	NWJ	New document – Preliminary Data Sheet (300 page product detail).
*B	130127	10/15/2003	NWJ	Revised document for Silicon Revision A.
*C	131679	12/05/2003	NWJ	Changes to Electrical Specifications section, Miscellaneous changes to I2C, GDI, RDI, Registers, and Digital Block chapters.
*D	131803	12/22/2003	NWJ	Changes to Electrical Specifications and miscellaneous small changes throughout the data sheet.
*E	229421	06/03/2004	SFV	New data sheet format and organization. Reference the *PSoC Mixed Signal Array Technical Reference Manual* for additional information. Title change.

Distribution: External/Public **Posting**: None

6.2 Copyrights