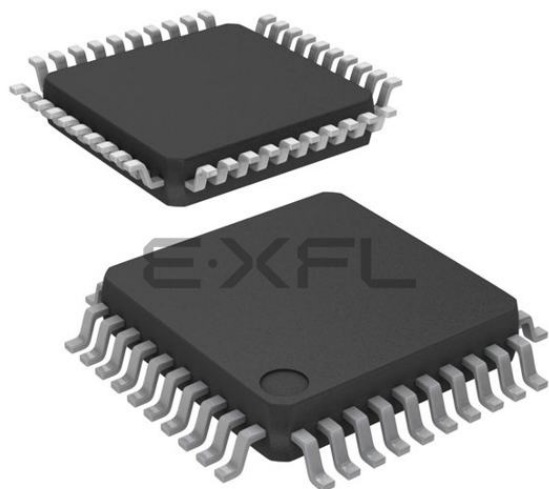




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Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	27
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21335tdfp-30

Table 1.2 Specifications for R8C/33T Group (2)

Item	Function	Specification
Serial Interface	UART0	Clock synchronous serial I/O/UART
	UART2	Clock synchronous serial I/O/UART, I ² C mode (I ² C-bus), SSU mode, multiprocessor communication function
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function, with sweep mode
Sensor Control Unit		System CH × 3, electrostatic capacitive touch detection × 18
Flash Memory		• Programming and erasure voltage: VCC = 2.7 V to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V)
Current Consumption		Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 3.5 μA (VCC = 3.0 V, wait mode) Typ. 2.0 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		−20 to 85°C (N version)
Package		32-pin LQFP Package code: PLQP0032GB-A (previous code: 32P6U-A)

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

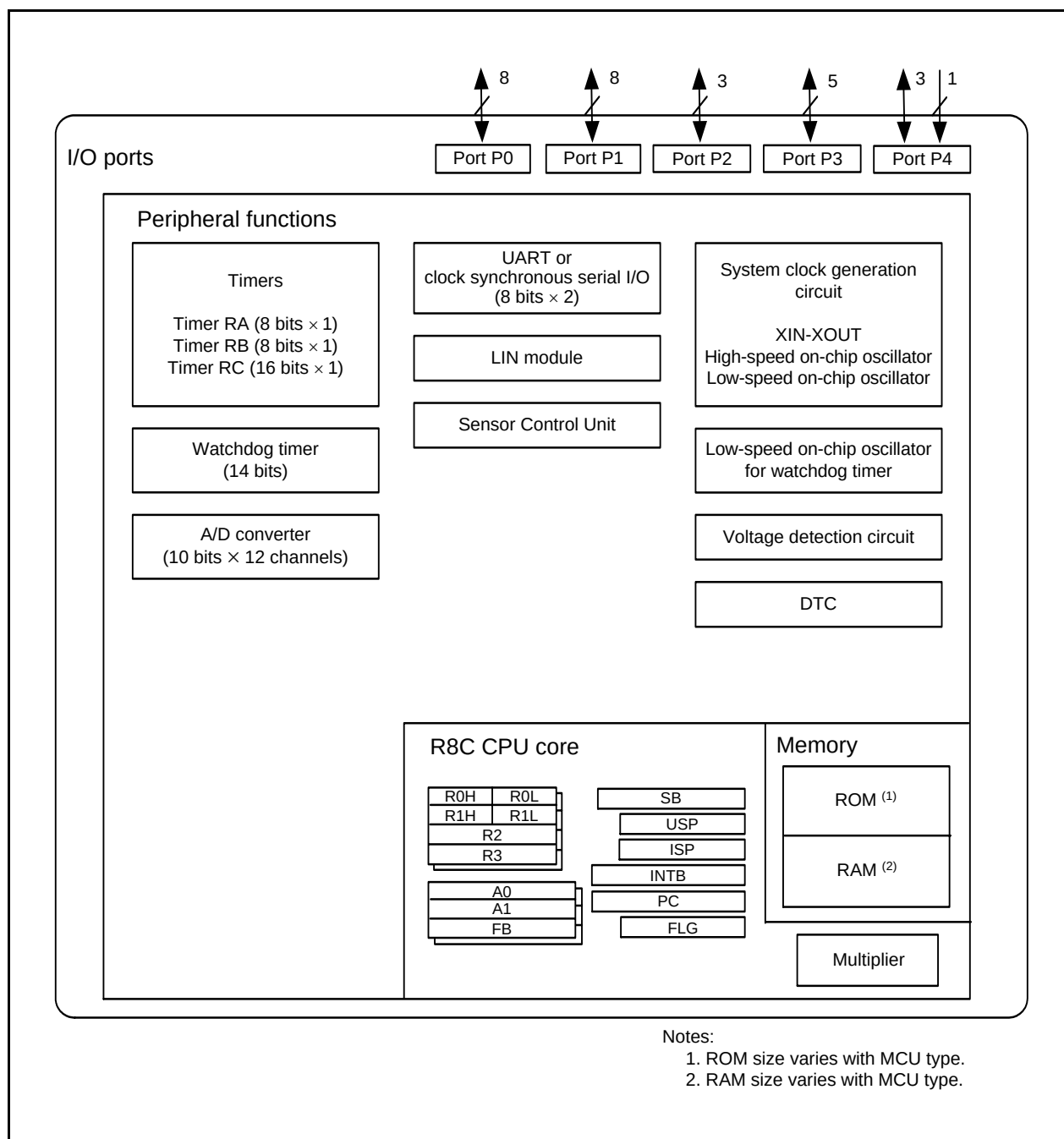


Figure 1.2 Block Diagram

Table 1.4 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules				
			Interrupt	Timer	Serial Interface	A/D Converter	Sensor Control Unit
1		P4_2				VREF	
2	MODE						
3	$\overline{\text{RESET}}$						
4	XOUT	P4_7					
5	VSS/AVSS						
6	XIN	P4_6					
7	VCC/AVCC						
8		P3_7	$\overline{(\text{INT3})}$	TRAO/ (TRCCLK)	(RXD2/SCL2/ TXD2/SDA2)		
9		P3_5	$\overline{(\text{INT1})}$	TRAIO/ (TRCIOD)	(CLK2)		
10		P3_4	$\overline{\text{INT2}}$	(TRCIOA)	(RXD2/SCL2/ TXD2/SDA2)		
11		P3_3	$\overline{\text{INT3}}$	TRBO/ (TRCCLK)	$\overline{(\text{CTS2/RTS2})}$		$\overline{\text{SCUTRG}}$
12		P2_2		(TRCIOA)	(RXD2/TXD2/ SCL2/SDA2)		CH17
13		P2_1		(TRCIOA)	(CLK2)		CH16
14		P2_0	$\overline{(\text{INT1})}$	(TRCIOB)	(RXD2/TXD2/ SCL2/SDA2)		CH15
15		P3_1		TRBO/ (TRCTRG/ TRCIOA)	$\overline{(\text{CTS2/RTS2})}$		CH14
16		P4_5	$\overline{\text{INT0}}$		(RXD2/SCL2)	$\overline{\text{ADTRG}}$	CH13
17		P1_7	$\overline{\text{INT1}}$	(TRAIO)			CH12
18		P1_6			(CLK0)		CH11
19		P1_5	$\overline{(\text{INT1})}$	(TRAIO)	(RXD0)		CH10
20		P1_4		(TRCCLK)	(TXD0)		CH9
21		P1_3	$\overline{\text{KI3}}$	TRBO (/TRCIOA)		AN11	CH8
22		P1_2	$\overline{\text{KI2}}$	(TRCIOB)		AN10	CH7
23		P1_1	$\overline{\text{KI1}}$	(TRCIOA/ TRCTRG)		AN9	CH6
24		P1_0	$\overline{\text{KI0}}$	(TRCIOA)		AN8	CH5
25		P0_7		(TRCIOA)		AN0	CH4
26		P0_6		(TRCIOA)		AN1	CH3
27		P0_5		(TRCIOB)	(CLK2)	AN2	CH2
28		P0_4		(TRCIOB)		AN3	CH1
29		P0_3		(TRCIOB)		AN4	CH0
30		P0_2		(TRCIOA/ TRCTRG)		AN5	CHxA
31		P0_1		(TRCIOA/ TRCTRG)		AN6	CHxB
32		P0_0		(TRCIOA/ TRCTRG)	(TXD2/SDA2)	AN7	CHxC

Note:

1. Can be assigned to the pin in parentheses by a program.

Table 4.2 SFR Information (2) ⁽¹⁾

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah			
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh			
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah	Sensor Control Unit Interrupt Control Register	SCUIC	XXXXX000b
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRES	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h			
0119h			
011Ah			
011Bh			
011Ch			
011Dh			
011Eh			
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 SFR Information (6) ⁽¹⁾

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC} /AV _{CC}	Supply voltage		−0.3 to 6.5	V
V _I	Input voltage		−0.3 to V _{CC} + 0.3	V
V _O	Output voltage		−0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	−20°C ≤ T _{opr} ≤ 85°C	500	mW
T _{opr}	Operating ambient temperature		−20 to 85 (N version)	°C
T _{stg}	Storage temperature		−65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter				Conditions	Standard			Unit		
						Min.	Typ.	Max.			
V _{CC} /AV _{CC}	Supply voltage					1.8	—	5.5	V		
V _{SS} /AV _{SS}	Supply voltage					—	0	—	V		
V _{IH}	Input “H” voltage	Other than CMOS input					0.8 V _{CC}	—	V _{CC}	V	
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.5 V _{CC}	—	V _{CC}	V		
					2.7 V ≤ V _{CC} < 4.0 V	0.55 V _{CC}	—	V _{CC}	V		
					1.8 V ≤ V _{CC} < 2.7 V	0.65 V _{CC}	—	V _{CC}	V		
			Input level selection : 0.5 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.65 V _{CC}	—	V _{CC}	V			
				2.7 V ≤ V _{CC} < 4.0 V	0.7 V _{CC}	—	V _{CC}	V			
				1.8 V ≤ V _{CC} < 2.7 V	0.8 V _{CC}	—	V _{CC}	V			
			Input level selection : 0.7 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.85 V _{CC}	—	V _{CC}	V			
				2.7 V ≤ V _{CC} < 4.0 V	0.85 V _{CC}	—	V _{CC}	V			
				1.8 V ≤ V _{CC} < 2.7 V	0.85 V _{CC}	—	V _{CC}	V			
		External clock input (XOUT)					1.2	—	V _{CC}	V	
		V _{IL}	Input “L” voltage	Other than CMOS input					0	—	0.2 V _{CC}
	CMOS input			Input level switching function (I/O port)	Input level selection : 0.35 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.2 V _{CC}	V	
2.7 V ≤ V _{CC} < 4.0 V						0	—	0.2 V _{CC}	V		
1.8 V ≤ V _{CC} < 2.7 V						0	—	0.2 V _{CC}	V		
Input level selection : 0.5 V _{CC}				4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.4 V _{CC}	V			
				2.7 V ≤ V _{CC} < 4.0 V	0	—	0.3 V _{CC}	V			
				1.8 V ≤ V _{CC} < 2.7 V	0	—	0.2 V _{CC}	V			
Input level selection : 0.7 V _{CC}				4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.55 V _{CC}	V			
				2.7 V ≤ V _{CC} < 4.0 V	0	—	0.45 V _{CC}	V			
				1.8 V ≤ V _{CC} < 2.7 V	0	—	0.35 V _{CC}	V			
External clock input (XOUT)					0	—	0.4 V _{CC}	V			
I _{OH} (sum)	Peak sum output “H” current			Sum of all pins I _{OH} (peak)				—	—	−160	mA
I _{OH} (sum)	Average sum output “H” current		Sum of all pins I _{OH} (avg)				—	—	−80	mA	
I _{OH} (peak)	Peak output “H” current	Drive capacity Low				—	—	−10	mA		
		Drive capacity High				—	—	−40	mA		
I _{OH} (avg)	Average output “H” current	Drive capacity Low				—	—	−5	mA		
		Drive capacity High				—	—	−20	mA		
I _{OL} (sum)	Peak sum output “L” current	Sum of all pins I _{OL} (peak)				—	—	160	mA		
I _{OL} (sum)	Average sum output “L” current	Sum of all pins I _{OL} (avg)				—	—	80	mA		
I _{OL} (peak)	Peak output “L” current	Drive capacity Low				—	—	10	mA		
		Drive capacity High				—	—	40	mA		
I _{OL} (avg)	Average output “L” current	Drive capacity Low				—	—	5	mA		
		Drive capacity High				—	—	20	mA		
f _(XIN)	XIN clock input oscillation frequency				2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz		
					1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz		
f _{OCO40M}	When used as the count source for timer RC ⁽³⁾				2.7 V ≤ V _{CC} ≤ 5.5 V	32	—	40	MHz		
f _{OCO-F}	f _{OCO-F} frequency				2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz		
					1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz		
—	System clock frequency				2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz		
					1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz		
f _(CLK)	CPU clock frequency				2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz		
					1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz		

Notes:

1. V_{CC} = 1.8 V to 5.5 V at T_{opr} = −20°C to 85°C (N version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. f_{OCO40M} can be used as the count source for timer RC in the range of V_{CC} = 2.7 V to 5.5 V.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVcc		—	—	10	Bit
—	Absolute accuracy	10-bit mode	Vref = AVcc = 5.0 V	AN0 to AN7 input AN8 to AN11 input	—	—	±3	LSB
			Vref = AVcc = 3.3 V	AN0 to AN7 input AN8 to AN11 input	—	—	±5	LSB
			Vref = AVcc = 3.0 V	AN0 to AN7 input AN8 to AN11 input	—	—	±5	LSB
			Vref = AVcc = 2.2 V	AN0 to AN7 input AN8 to AN11 input	—	—	±5	LSB
		8-bit mode	Vref = AVcc = 5.0 V	AN0 to AN7 input AN8 to AN11 input	—	—	±2	LSB
			Vref = AVcc = 3.3 V	AN0 to AN7 input AN8 to AN11 input	—	—	±2	LSB
			Vref = AVcc = 3.0 V	AN0 to AN7 input AN8 to AN11 input	—	—	±2	LSB
			Vref = AVcc = 2.2 V	AN0 to AN7 input AN8 to AN11 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ Vref = AVcc ≤ 5.5 V ⁽²⁾		2	—	20	MHz
			3.2 V ≤ Vref = AVcc ≤ 5.5 V ⁽²⁾		2	—	16	MHz
			2.7 V ≤ Vref = AVcc ≤ 5.5 V ⁽²⁾		2	—	10	MHz
			2.2 V ≤ Vref = AVcc ≤ 5.5 V ⁽²⁾		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVcc = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVcc = 5.0 V, φAD = 20 MHz		2.2	—	—	ms
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5.0 V, XIN = f1 = φAD = 20 MHz		—	45	—	μA
Vref	Reference voltage				2.2	—	AVcc	V
VIA	Analog input voltage ⁽³⁾				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

1. Vcc/AVcc = Vref = 2.2 V to 5.5 V, Vss = 0 V at Topr = −20°C to 85°C (N version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-consumption current mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	—	—	year

Notes:

1. V_{CC} = 2.7 V to 5.5 V at T_{opr} = 0°C to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet0	Voltage detection level Vdet0_0 ⁽²⁾		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 ⁽²⁾		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 ⁽²⁾		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 ⁽²⁾		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time ⁽⁴⁾	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = –20°C to 85°C (N version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level Vdet1_0 ⁽²⁾	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 ⁽²⁾	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 ⁽²⁾	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 ⁽²⁾	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 ⁽²⁾	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 ⁽²⁾	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 ⁽²⁾	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 ⁽²⁾	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 ⁽²⁾	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 ⁽²⁾	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A ⁽²⁾	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B ⁽²⁾	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C ⁽²⁾	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D ⁽²⁾	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E ⁽²⁾	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F ⁽²⁾	At the falling of Vcc	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time ⁽³⁾	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	—	60	150	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = –20°C to 85°C (N version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	Vcc = 1.8 V to 5.5 V −20°C ≤ Topr ≤ 85°C	38.4	40	41.6	MHz
—	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (2)	Vcc = 1.8 V to 5.5 V −20°C ≤ Topr ≤ 85°C	35.389	36.864	38.338	MHz
—	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	Vcc = 1.8 V to 5.5 V −20°C ≤ Topr ≤ 85°C	30.72	32	33.28	MHz
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	0.5	3	ms
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	400	—	μA

Notes:

1. Vcc = 1.8 V to 5.5 V, Topr = −20°C to 85°C (N version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	30	100	μs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	2	—	μA

Note:

1. Vcc = 1.8 V to 5.5 V, Topr = −20°C to 85°C (N version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during power-on (2)		—	—	2000	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.13 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

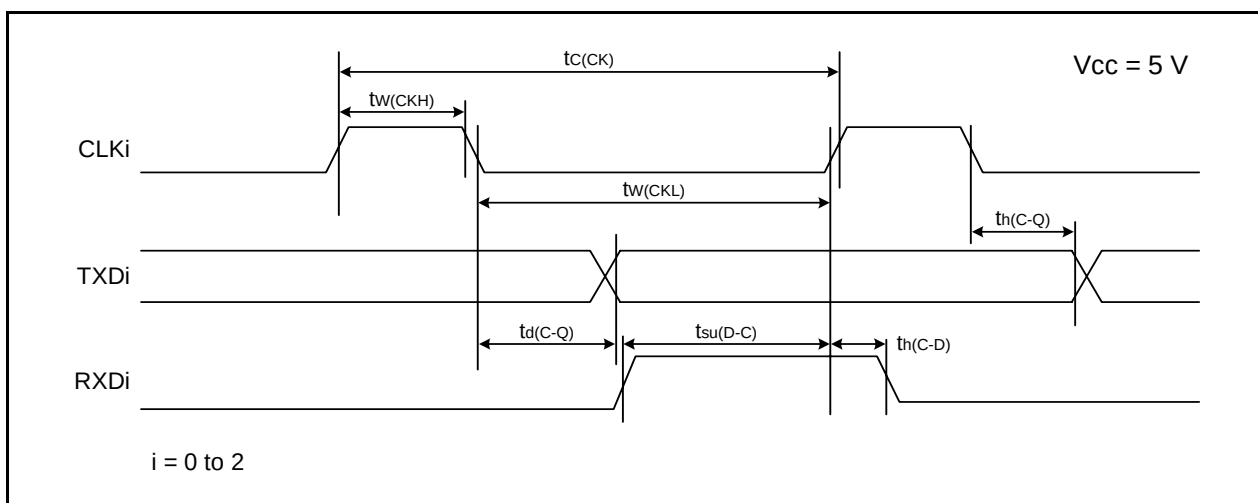
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage	Other than XOUT	Drive capacity High Vcc = 5 V	IOH = -20 mA	Vcc - 2.0	—	Vcc	V
			Drive capacity Low Vcc = 5 V	IOH = -5 mA	Vcc - 2.0	—	Vcc	V
		XOUT	Vcc = 5 V	IOH = -200 μA	1.0	—	Vcc	V
VOL	Output "L" voltage	Other than XOUT	Drive capacity High Vcc = 5 V	IOL = 20 mA	—	—	2.0	V
			Drive capacity Low Vcc = 5 V	IOL = 5 mA	—	—	2.0	V
		XOUT	Vcc = 5 V	IOL = 200 μA	—	—	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOA, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SCL2, SDA2			0.1	1.2	—	V
		RESET			0.1	1.2	—	V
IiH	Input "H" current		Vi = 5 V, Vcc = 5.0 V		—	—	5.0	μA
IiL	Input "L" current		Vi = 0 V, Vcc = 5.0 V		—	—	-5.0	μA
RPULLUP	Pull-up resistance		Vi = 0 V, Vcc = 5.0 V		25	50	100	kΩ
RfXIN	Feedback resistance	XIN			—	0.3	—	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. 4.2 V ≤ Vcc ≤ 5.5 V at Topr = -20°C to 85°C (N version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.17 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.6 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.18 External Interrupt $\overline{INTi}$ ($i = 0 \text{ to } 3$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0 \text{ to } 3$)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	250 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	250 (2)	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

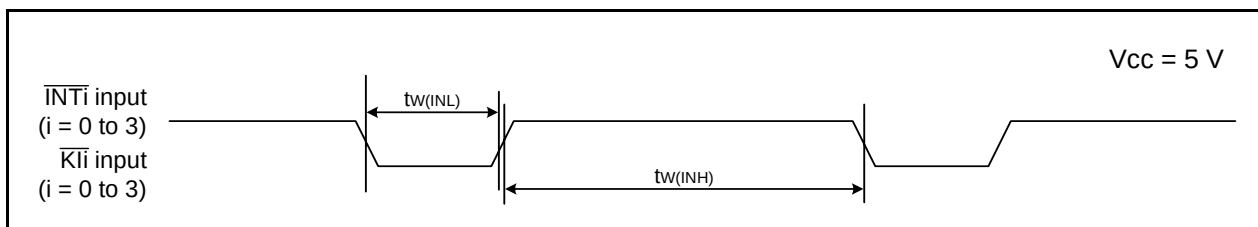
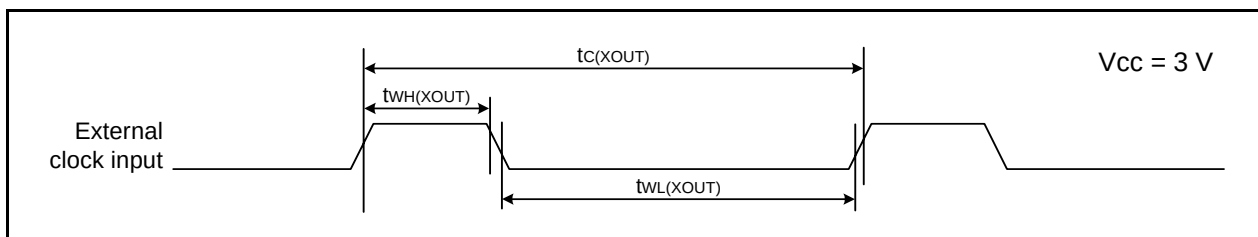
**Figure 5.7 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 5 V**

Table 5.20 Electrical Characteristics (4) [$2.7\text{ V} \leq V_{CC} < 3.3\text{ V}$]
($T_{opr} = -20^{\circ}\text{C}$ to 85°C (N version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current ($V_{CC} = 2.7\text{ V}$ to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	—	3.5	10	mA
		High-speed clock mode	—	1.5	7.5	mA
		High-speed on-chip oscillator mode	—	7	15	mA
		Low-speed on-chip oscillator mode	—	90	390	μA
		Wait mode	—	15	90	μA
		Stop mode	—	2	5.0	μA

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$)****Table 5.21 External Clock Input (XOUT)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{XOUT})$	XOUT input cycle time	50	—	ns
$t_{WH}(\text{XOUT})$	XOUT input "H" width	24	—	ns
$t_{WL}(\text{XOUT})$	XOUT input "L" width	24	—	ns

**Figure 5.8 External Clock Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.22 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{TRAIO})$	TRAIO input cycle time	300	—	ns
$t_{WH}(\text{TRAIO})$	TRAIO input "H" width	120	—	ns
$t_{WL}(\text{TRAIO})$	TRAIO input "L" width	120	—	ns

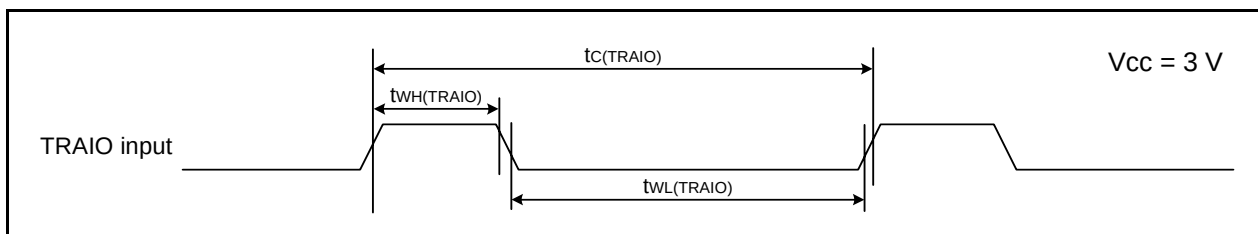
**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.25 Electrical Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]

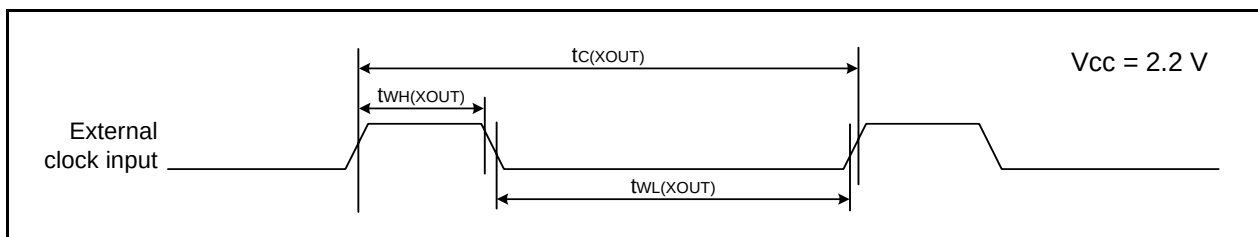
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I _{OH} = -2 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT		I _{OH} = -200 μ A	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
		XOUT		I _{OL} = 200 μ A	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}}, \overline{\text{INT3}}, \overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}}, \overline{\text{TRAIO}}, \overline{\text{TRBO}}, \overline{\text{TRCIOA}}, \overline{\text{TRCIOB}}, \overline{\text{TRCIOA}}, \overline{\text{TRCIOC}}, \overline{\text{TRCIOD}}, \overline{\text{TRCTRG}}, \overline{\text{TRCCLK}}, \overline{\text{ADTRG}}, \overline{\text{RXD0}}, \overline{\text{RXD2}}, \overline{\text{CLK0}}, \overline{\text{CLK2}}, \overline{\text{SCL2}}, \overline{\text{SDA2}}$			0.05	0.20	—	V
		$\overline{\text{RESET}}$			0.05	0.20	—	V
I _{IH}	Input "H" current		V _I = 2.2 V, V _{CC} = 2.2 V		—	—	4.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 2.2 V		—	—	-4.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 2.2 V		70	140	300	k Ω
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

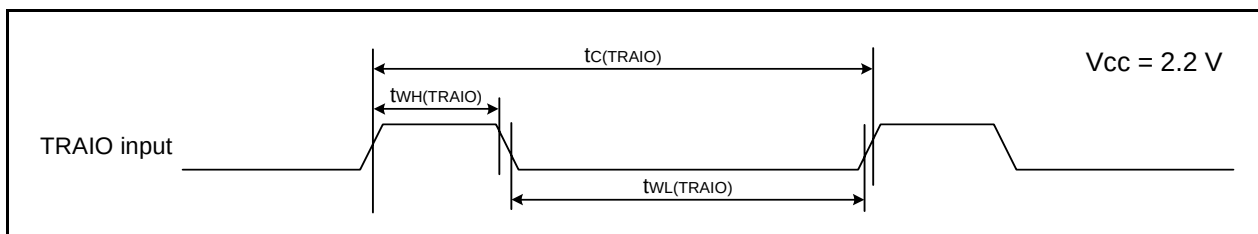
1. $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ at T_{opr} = -20°C to 85°C (N version), f(XIN) = 5 MHz, unless otherwise specified.

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$)****Table 5.27 External Clock Input (XOUT)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	200	—	ns
$t_{WH(XOUT)}$	XOUT input "H" width	90	—	ns
$t_{WL(XOUT)}$	XOUT input "L" width	90	—	ns

**Figure 5.12 External Clock Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.28 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	—	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	200	—	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	200	—	ns

**Figure 5.13 TRAIO Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

Technical drawing of a square microstrip antenna array. The top view shows a square layout with dimensions H_D , H_E , D , E , and Z_E . It features 24 elements on the top and bottom edges, and 16 elements on the left and right edges. An index mark is shown at the bottom-left corner. A side view shows the profile of the elements. A terminal cross-section shows dimensions b_p , b_1 , G , and c . A detail F shows a cross-section of the antenna structure with dimensions A , A_1 , A_2 , L , L_1 , and θ . A bottom view shows dimensions G , y , b_p , and $*3$, along with a coordinate system (x, y).