

Welcome to **E-XFL.COM**

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

| Details | |
|----------------------------|--|
| Product Status | Not For New Designs |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I ² C, LINbus, SIO, SSU, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 27 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 2.5K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21336tdfp-30 |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

R8C/33T Group 1. Overview

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/33T Group.

Table 1.1 Specifications for R8C/33T Group (1)

| Item | Function | Specification |
|--------------------------------------|---------------------------|---|
| CPU | Central processing unit | R8C CPU core Number of fundamental instructions: 89 Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 V to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 V to 5.5 V) Multiplier: 16 bits x 16 bits → 32 bits Multiply-accumulate instruction: 16 bits x 16 bits + 32 bits → 32 bits Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM, Data flash | Refer to Table 1.3 Product List for R8C/33T Group. |
| Power Supply Voltage Detection | Voltage detection circuit | Power-on reset Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable) |
| I/O Ports | Programmable I/O ports | Input-only: 1 pin CMOS I/O ports: 27, selectable pull-up resistor High current drive ports: 27 |
| Clock | Clock generation circuits | 3 circuits: XIN clock oscillation circuit, High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator Oscillation stop detection: XIN clock oscillation stop detection function Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | Number of interrupt vectors: 69 External Interrupt: 7 (INT × 4, Key input × 4) Priority levels: 7 levels |
| Watchdog Tim | er | 14 bits x 1 (with prescaler) Reset start selectable Low-speed on-chip oscillator for watchdog timer selectable |
| DTC (Data Tra | nsfer Controller) | 1 channel Activation sources: 22 Transfer modes: 2 (normal mode, repeat mode) |
| Timer | Timer RA | 8 bits x 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits x 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |

R8C/33T Group 1. Overview

1.2 Product List

Table 1.3 lists Product List for R8C/33T Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/33T Group.

Table 1.3 Product List for R8C/33T Group

Current of Apr 2011

| Part No. | ROM C | apacity | RAM | Package Type | Remarks |
|-----------------|-------------|-------------|------------|--------------|---------------------------------------|
| rait No. | Program ROM | Data flash | Capacity | rackage Type | Remarks |
| R5F21334TNFP | 16 Kbytes | 1 Kbyte × 4 | 1.5 Kbytes | PLQP0032GB-A | N version |
| R5F21335TNFP | 24 Kbytes | 1 Kbyte × 4 | 2 Kbytes | PLQP0032GB-A | |
| R5F21336TNFP | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PLQP0032GB-A | |
| R5F21334TNXXXFP | 16 Kbytes | 1 Kbyte × 4 | 1.5 Kbytes | PLQP0032GB-A | N version |
| R5F21335TNXXXFP | 24 Kbytes | 1 Kbyte × 4 | 2 Kbytes | PLQP0032GB-A | Factory- |
| R5F21336TNXXXFP | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PLQP0032GB-A | programming product ⁽¹⁾ |

Note:

1. The user ROM is programmed before shipment.

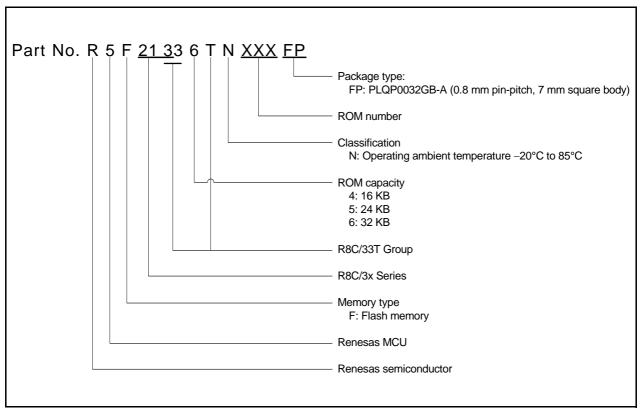


Figure 1.1 Part Number, Memory Size, and Package of R8C/33T Group

R8C/33T Group 1. Overview

1.5 Pin Functions

Table 1.5 lists Pin Functions.

Table 1.5 Pin Functions

| Item | Pin Name | I/O Type | Description |
|-----------------------------------|--|-------------|--|
| Power supply input | VCC, VSS | _ | Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | _ | Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS. |
| Reset input | RESET | I | Input "L" on this pin resets the MCU. |
| MODE | MODE | I | Connect this pin to VCC via a resistor. |
| XIN clock input XIN clock output | XIN | I/O | These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. (1) |
| And clock output | 7001 | 1/0 | To use an external clock, input it to the XOUT pin and leave the XIN pin open. |
| INT interrupt input | INTO to INT3 | I | INT interrupt input pins. INT0 is timer RB, and RC input pin. |
| Key input interrupt | KI0 to KI3 | I | Key input interrupt input pins |
| Timer RA | TRAIO | I/O | Timer RA I/O pin |
| | TRAO | 0 | Timer RA output pin |
| Timer RB | TRBO | 0 | Timer RB output pin |
| Timer RC | TRCCLK | I | External clock input pin |
| | TRCTRG | I | External trigger input pin |
| | TRCIOA, TRCIOB, TRCIOC, TRCIOD | I/O | Timer RC I/O pins |
| Serial interface | CLK0, CLK2 | I/O | Transfer clock I/O pins |
| | RXD0, RXD2 | I | Serial data input pins |
| | TXD0, TXD2 | 0 | Serial data output pins |
| | CTS2 | I | Transmission control input pin |
| | RTS2 | 0 | Reception control output pin |
| | SCL2 | I/O | I ² C mode clock I/O pin |
| | SDA2 | I/O | I ² C mode data I/O pin |
| Reference voltage | VREF | 1 | Reference voltage input pin to A/D converter |
| input | VIX.2. | • | The form to the desired to the section of the secti |
| A/D converter | AN0 to AN11 | I | Analog input pins to A/D converter |
| | ADTRG | I | AD external trigger input pin |
| Sensor control unit | CHxA, CHxB, CHxC | I/O | Control pins for electrostatic capacitive touch detection |
| | CH0 to CH17 | 1 | Electrostatic capacitive touch detection pins |
| | SCUTRG | ı | Sensor control unit external trigger input |
| I/O port | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_2, P3_1, P3_3 to P3_5, P3_7, P4_5 to P4_7 | I/O | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. All ports can be used as LED drive ports. |
| Input port | P4_2 | 1 | Input-only port |

I: Input

O: Output

I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

R8C/33T Group 3. Memory

3. Memory

3.1 R8C/33T Group

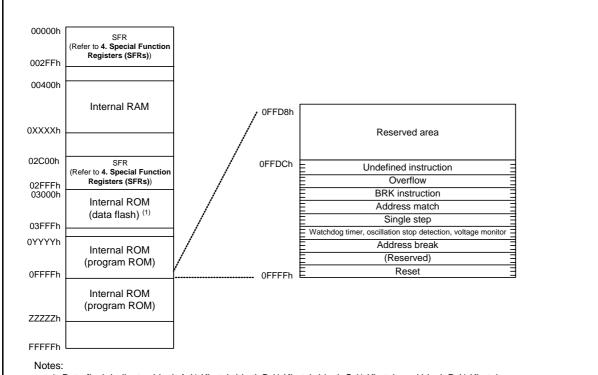
Figure 3.1 is a Memory Map of R8C/33T Group. The R8C/33T Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 32-Kbyte internal ROM area is allocated addresses 08000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



- - 1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
 - The blank areas are reserved and cannot be accessed by users.

| Part Number | | Internal ROM | Internal RAM | | | |
|----------------------------------|-----------|----------------|----------------|------------|----------------|--|
| Fait Number | Size | Address 0YYYYh | Address ZZZZZh | Size | Address 0XXXXh | |
| R5F21334TNFP, R5F21334TDFP, | 16 Kbytes | 0C000h | | 1.5 Kbytes | 009FFh | |
| R5F21334TNXXXFP, R5F21334TDXXXFP | 10 NDytes | 0000011 | _ | 1.5 Kbytes | 009FFII | |
| R5F21335TNFP, R5F21335TDFP, | 24 Kbytes | 0A000h | _ | 2 Kbytes | 00BFFh | |
| R5F21335TNXXXFP, R5F21335TDXXXFP | 24 Noyles | UAUUUII | _ | 2 Noyles | OODITII | |
| R5F21336TNFP, R5F21336TDFP, | 32 Kbytes | 08000h | | 2.5 Kbytes | 00DFFh | |
| R5F21336TNXXXFP, R5F21336TDXXXFP | 32 Noytes | 0000011 | | 2.0 Rbytes | 0001111 | |

Figure 3.1 Memory Map of R8C/33T Group

Table 4.4 SFR Information (4) (1)

| Add Add Add Register ADD ADD ADD ADD | A -l -l | Donister. | 0 | A4 D |
|--|---------|------------------------------|--------------|-------------|
| 000000000000000000000000000000000000 | Address | Register | Symbol | After Reset |
| 00029h | | A/D Register 0 | AD0 | |
| 00000AX 0000AX 00000AX 00000AX 0000C 0000C | | | | 000000XXb |
| 00000AX 0000AX 00000AX 00000AX 0000C 0000C | 00C2h | A/D Register 1 | AD1 | XXh |
| 600C4h AD Register 2 AD2 XXh 600C8h AD Register 3 AD3 XXh 600C8h AD Register 4 AD4 XXh 600C9h AD Register 5 AD5 XXh 600CBh AD Register 6 AD6 XXh 600CBh AD7 XXh 000000000000000000000000000000000000 | 00C3h | 1 | | 000000XXb |
| | | Δ/D Register 2 | AD2 | |
| OCC AD Register 3 | | - Nogister 2 | ND2 | |
| 00000Xb | | | 100 | |
| 0005h AD Register 4 0000000000000000000000000000000000 | | A/D Register 3 | AD3 | |
| 000000000000000000000000000000000000 | | | | |
| OOCAh AD Register 5 | 00C8h | A/D Register 4 | AD4 | XXh |
| 000000000000000000000000000000000000 | 00C9h | | | 000000XXb |
| 000000000000000000000000000000000000 | 00CAh | A/D Register 5 | AD5 | XXh |
| OOCCh AD Register 6 | | 1 | | |
| 000000000000000000000000000000000000 | | A/D Pagistor 6 | AD6 | |
| 00CEh AD Register 7 00DCh 000000000000000000000000000000000000 | | A/D Register 0 | ADO | |
| 000000000000000000000000000000000000 | | | | |
| | | A/D Register 7 | AD7 | |
| 00D2h 00D2h 00D2h 00D3h 00D5h AD Mode Register ADMOD 00D5h AD Input Select Register ADINSEL 11000000b 00D5h AD Control Register 0 ADCONI 00h 00D8h AD Control Register 1 00h 00D8h ADCONI 00D 00D8h ADCONI 00D 00D8h Port P8 Register P0 XXh 00E2h Port P9 Direction Register P01 XXh 00E3h Port P2 Register P2 XXh 00E4h P | | | | 000000XXb |
| 00D2h 00D3h AD Mode Register ADMOD 00h 00D4h AD Input Select Register ADINSEL 11000000b 00D5h AD Control Register 0 ADCON1 00h 00D7h AD Control Register 1 ADCON1 00h 00D8h 00D8h 00D0h 00D0h 00DAh 00D0h 00D0h 00D0h 00DCh 00D0h 00D0h 00D0h 00DDh 00D0h 00D0h 00D0h 00DCh 00D0h 00D0h 00D0h 00DCh 00D0h 00D0h 00D0h 00DCh 00D0h 00D0h 00D0h 00E1h Port P0 Register P0 XXh 00E2h Port P1 Register P0 00h 00E3h Port P2 Register P0 00h 00E4h Port P3 Register P2 XXh 00E5h Port P3 Register P2 00h 00E6h Port P4 Register P0 00h 00E8h | 00D0h | | | |
| 00D2h 00D3h AD Mode Register ADMOD 00h 00D4h AD Input Select Register ADINSEL 11000000b 00D5h AD Control Register 0 ADCON1 00h 00D7h AD Control Register 1 ADCON1 00h 00D8h 00D8h 00D0h 00D0h 00DAh 00D0h 00D0h 00D0h 00DCh 00D0h 00D0h 00D0h 00DDh 00D0h 00D0h 00D0h 00DCh 00D0h 00D0h 00D0h 00DCh 00D0h 00D0h 00D0h 00DCh 00D0h 00D0h 00D0h 00E1h Port P0 Register P0 XXh 00E2h Port P1 Register P0 00h 00E3h Port P2 Register P0 00h 00E4h Port P3 Register P2 XXh 00E5h Port P3 Register P2 00h 00E6h Port P4 Register P0 00h 00E8h | 00D1h | | | |
| 00D3h AD Mode Register ADMOD 00h 00D5h AD Input Select Register ADINSEL 11000000b 00D6h AD Control Register 0 ADCONI 00h 00D8h DODOBh 00h 00h 00D8h DODOBh 00DAh 00DAh 00D8h DODOBh 00DCh 00DCh 00DCh DODOBh 00DCh 00DCh 00DCh DODOBh 00DCh 00DCh 00DEh DODOBh 00DCh 00DCh 00DEh DODOBh 00DCh 00DCh 00DEh DOTOBH 00DCh 00DCh 00E0h Port PO Register P0 XXh 00E1h Port PO Register P1 XXh 00E2h Port PO Inection Register PD1 00h 00E3h Port P1 Register P2 XXh 00E5h Port P2 Register P2 XXh 00E5h Port P3 Direction Register PD2 00h 00E8h P0T | | | + | <u> </u> |
| 00D4h AD Mode Register ADMOD 00h 00D5h AD Input Select Register 0 ADKON0 00h 00D5h AD Control Register 1 ADCON1 00h 00D8h 00D8h 00DA 00DAN 00DA 00DA 00DA 00DA 00DA 00DCh 00DCh 00DCh 00DEh 00DEh 00DCh 00DEh 00DCh 00DCh 00E2D Port PO Register PO XXh 00E3D Port PO Register PO XXh 00E3D Port PO Direction Register PD0 00h 00E3h Port PO Direction Register PD0 00h 00E3h Port PO Register PD0 00h 00E3h Port PO Register PD1 00h 00E3h Port PO Register PD2 00h 00E4h Port PS Register PP2 XXh 00E5h Port PS Direction Register PD2 00h 00E4h Port P4 Reg | | | | |
| ODDSh | | A/D Mada Davistor | ADMOD | 006 |
| 00DEh AD Control Register 0 ADCON0 O0h 00DPh 00DBh 00D 00h 00DBh 00DAh 00DBh 00DBh 00DBh 00DCh | | A/D Iviode Register | | |
| 00DPh A/D Control Register 1 00h 00D8h 00Dah 00DBh 00DAh 00DBh 00DBh 00DBh 00DBh 00DDh 00DDh 00DDh 00DBh 00DDh 00DDh 00DDh 00DDh 00Eh 00Eh 00Eh Port P0 Register 00Eh Port P1 Register 00Eh Port P2 Register 00Eh Port P3 Direction Register 00EAh Port P2 Register 00EAh Port P3 Direction Register 00EAh Port P3 Direction Register 00EAh Port P4 Register 00EAh Port P4 Register 00EAh Port P4 Register 00EAh Port P4 Register 00EAh Port P5 Direction Register 00EAh Port P4 Direction Register 00EAh Port P5 Direction Register 00EAh Port P4 Register 00EAh Port P5 Direction Register 00EAh Port P5 P5 P5 P5 P5 P5 P5 P5 P5 | | A/D Input Select Register | | |
| 00D8h 00DAh 00DAh 00DBh 00DCh 00DCh 00DEh 00DEh 00DEh 00DEh 00Eh 00Eh 00Eh 00Eh 00Eh Port PO Register 00Eh Port PI Register 00Eh Port PD Direction Register 00Eh Port PD Direction Register 00Eh Port P2 Register 00Eh Port P3 Register 00Eh Port P3 Register 00Eh Port P3 Direction Register 00Eh Port P3 Direction Register 00Eh Port P3 Direction Register 00Eh Port P4 Direction Registe | | A/D Control Register 0 | | |
| 00D8h 00DAh 00DAh 00DBh 00DCh 00DCh 00DEh 00DEh 00DEh 00DEh 00Eh 00Eh 00Eh 00Eh 00Eh Port PO Register 00Eh Port PI Register 00Eh Port PD Direction Register 00Eh Port PD Direction Register 00Eh Port P2 Register 00Eh Port P3 Register 00Eh Port P3 Register 00Eh Port P3 Direction Register 00Eh Port P3 Direction Register 00Eh Port P3 Direction Register 00Eh Port P4 Direction Registe | 00D7h | A/D Control Register 1 | ADCON1 | 00h |
| 00D9h 00DAh 00DBh 00DCh 00DCh 00DDh 00DPh 00DEh 00DFh 00DFh 00E0h 00E0h 00E1h Port P0 Register 00E2h Port P1 Register 00E2h Port P2 Register 00E3h Port P1 Direction Register 00E3h Port P2 Register 00E3h Port P3 Register 00E4h Port P2 Register 00E5h Port P3 Direction Register 00E7h Port P3 Direction Register 00E7h Port P4 Register 00E8h Port P4 Register 00E9h Port P4 Direction Register 00E8h Port P4 Direction Register 00EAh Port P4 Direction Register | | - | | |
| 00DAh 00DBh 00DCh 00DDh 00DFh 00DFh 00Eh 00Eh 00E1h Port P0 Register 00E1h Port P1 Register 00E1h Port P1 Register 00E1h Port P0 Direction Register 00E3h Port P1 Direction Register 00E4h Port P2 Register 00E4h Port P3 Register 00E6h Port P2 Register 00E6h Port P3 Direction Register 00E7h Port P3 Direction Register 00E8h Port P4 Register 00E9h Port P4 Register 00E8h Port P4 Direction Register 00E8h Port P4 Direction Register 00E9h Port P4 Register 00E9h Port P4 Direction Register 00E8h Port P4 Direction Register | | | | |
| 00DBh 00DCh 00DDh 00DEh 00DFh 00DFh 00E0h Port P0 Register 00E1h Port P1 Register 00E2h Port P1 Direction Register 00E2h Port P1 Direction Register 00E3h Port P2 Direction Register 00E3h Port P3 Register 00E5h Port P3 Register 00E7h Port P3 Direction Register 00E7h Port P3 Direction Register 00E7h Port P4 Register 00E8h Port P4 Register 00E8h Port P4 Direction Register 00EAh Port P4 Direction Register 00EDh OOBEN 00ECh OOBEN 00ECh OOBEN 00ECh OOBEN 00ECh OOBEN 00ECh OOECh 00ECh OOECh 00F3h OOECh 00F4h OOFSh 00F5h OOFSh 00F6h OOFSh 00F8h OOFSh | | | | |
| GODCh 00DDh OODFh 00DFh OOE0h Port P0 Register O0E1h Port P1 Register O0E1h Port P1 Direction Register O0E2h Port P0 Direction Register O0E3h Port P1 Direction Register O0E3h Port P2 Register O0E4h Port P3 Register O0E6h Port P3 Register O0E6h Port P3 Direction Register O0E6h Port P3 Direction Register O0E7h Port P4 Register O0E8h Port P4 Register O0E9h Port P4 Direction Register O0E8h Port P4 Direction Register O0E9h Port P4 Direction Register O0E0h Port P4 Direction Register <t< td=""><td></td><td></td><td></td><td></td></t<> | | | | |
| OODDh OODEh OODFh 00DFh OOE0h Port P0 Register PO XXh O0E1h Port P1 Register P1 XXh O0E2h Port P0 Direction Register PD0 O0h O0E3h Port P1 Direction Register PD0 O0h O0E4h Port P2 Register PD1 O0h O0E5h Port P3 Register P2 XXh O0E6h Port P2 Direction Register PD2 O0h O0E7h Port P2 Direction Register PD3 O0h O0E8h Port P4 Register PP3 O0h O0E8h Port P4 Direction Register PD4 ONh O0E8h Port P4 Direction Register PD4 ONh O0E8h O0E0 ONh ONh O0E8h O0E0 ONh ONh O0E9h O0E0 ONh ONh O0E9h O0E0 ONh ONh O0E9h O0E0 ONH ONh O0E9h <td></td> <td></td> <td></td> <td></td> | | | | |
| 00DEh 00DFh 00E0h Port P0 Register P0 XXh 00E1h Port P1 Register P1 XXh 00E2h Port P0 Direction Register PD0 00h 00E3h Port P1 Direction Register PD1 00h 00E4h Port P2 Register P2 XXh 00E6h Port P2 Direction Register P3 XXh 00E6h Port P3 Direction Register PD2 00h 00E7h Port P4 Register PA XXh 00E9h Port P4 Register PA XXh 00E9h Port P4 Direction Register PD4 00h 00E8h POT P4 Direction Register PD4 00h 00E8h POT P4 Direction Register PD4 00h 00E8h POT P4 Direction Register PD4 00h 00E0h POT P4 Direction Register PD4 00h 00E0h POT P4 | | | | |
| 00DFh Port P0 Register P0 XXh 00E1h Port P1 Register P1 XXh 00E2h Port P0 Direction Register PD0 00h 00E3h Port P1 Direction Register PD1 00h 00E3h Port P2 Register P2 XXh 00E5h Port P3 Register P3 XXh 00E6h Port P2 Direction Register PD2 00h 00E7h Port P3 Direction Register PD3 00h 00E8h Port P4 Register P4 XXh 00E8h Port P4 Direction Register PD4 00h 00E8h Port P4 Direction Register PD4 00h 00E8h Port P4 Direction Register PD4 00h 00EBh 00EA 00h 00h 00ECh 00ECh 00h 00h 00EDh 00EBh 00EBh 00EBh 00F3h 00F3h 00F3h 00F3h 00F3h 00F4h 00F5h 00F6h | | | | |
| 00E0h Port P0 Register P0 XXh 00E1h Port P1 Register P1 XXh 00E2h Port P0 Direction Register PD0 00h 00E3h Port P1 Direction Register PD1 00h 00E4h Port P2 Register P2 XXh 00E5h Port P2 Register P3 XXh 00E6h Port P2 Direction Register PD2 00h 00E7h Port P3 Direction Register PD3 00h 00E8h Port P4 Register P4 XXh 00E9h P0t P4 Direction Register PD4 00h 00EBh P0t P4 Direction Register PD4 00h 00EDh P0t P4 Direction Register PD4 00h 00EDh P0t P4 Direction Register PD4 00h 00EDh P0t P4 Direction Register PD4 00h 00Ebh P0t P4 Direction Register PD4 00h 00Eh P0t P4 P0t P4 P0h 00Eh P0t P4 P0t P4 </td <td>00DEh</td> <td></td> <td></td> <td></td> | 00DEh | | | |
| 00E0h Port P0 Register P0 XXh 00E1h Port P1 Register P1 XXh 00E2h Port P0 Direction Register PD0 00h 00E3h Port P1 Direction Register PD1 00h 00E4h Port P2 Register P2 XXh 00E5h Port P2 Register P3 XXh 00E6h Port P2 Direction Register PD2 00h 00E7h Port P3 Direction Register PD3 00h 00E8h Port P4 Register P4 XXh 00E9h P0t P4 Direction Register PD4 00h 00EBh P0t P4 Direction Register PD4 00h 00EDh P0t P4 Direction Register PD4 00h 00EDh P0t P4 Direction Register PD4 00h 00EDh P0t P4 Direction Register PD4 00h 00Ebh P0t P4 Direction Register PD4 00h 00Eh P0t P4 P0t P4 P0h 00Eh P0t P4 P0t P4 </td <td>00DFh</td> <td></td> <td></td> <td></td> | 00DFh | | | |
| 00E1h Port P1 Register P1 XXh 00E2h Port P0 Direction PD0 00h 00E3h Port P1 Direction Register PD1 00h 00E4h Port P2 Register P2 XXh 00E6h Port P3 Register P3 XXh 00E6h Port P3 Direction Register PD2 00h 00E7h Port P4 Spirection Register PD3 00h 00E8h Port P4 Register P4 XXh 00E9h Port P4 Direction Register PD4 00h 00EAh Port P4 Direction Register PD4 00h 00EDh O0ECh 00EDh 00EDh 00ECh 00EDh 00EDh 00EDh 00Eh 00Eh 00Eh 00Eh 00Fh 00Fh 00Eh 00Eh 00Fh 00Fh 00Fh 00Eh 00Fh 00Fh 00Fh 00Fh 00Fh 00Fh 00Fh 00Fh 00Fh 00Fh | | Port P0 Register | PO | XXh |
| 00E2h Port P0 Direction Register PD0 00h 00E3h Port P1 Direction Register PD1 00h 00E4h Port P2 Register P2 XXh 00E5h Port P3 Register P3 XXh 00E6h Port P2 Direction Register PD2 00h 00E7h Port P3 Direction Register PD3 00h 00E8h Port P4 Register P4 XXh 00E9h 00EAh 00H 00EAh 00EAh Port P4 Direction Register PD4 00h 00EBh 00EAh 00h 00H 00EDh 00EBh 00EAh 00H 00EBh 00EBh 00EAh 00EAh 00EBh 00EAH 00EAH 00EAH 00EBh 00EAH 00EAH 00EAH 00EBh 00EAH 00EAH 00EAH 00EAH 00EAH 00EAH 00EAH 00F3h 00EAH 00EAH 00EAH 00F3h 00EAH | | Port P1 Pogistor | | |
| 00E3h Port P1 Direction Register PD1 00h 00E4h Port P2 Register P2 XXh 00E6h Port P3 Register P3 XXh 00E6h Port P2 Direction Register PD2 00h 00E7h Pot P3 Direction Register PD3 00h 00E8h Port P4 Register P4 XXh 00E9h | | Port DO Discretion Desciotes | | |
| 00E4h Port P2 Register P2 XXh 00E5h Port P3 Register P3 XXh 00E6h Port P2 Direction Register PD2 00h 00E7h Port P3 Direction Register PD3 00h 00E8h Port P4 Register P4 XXh 00E9h P0T P4 Direction Register PD4 00h 00ECh O0EOBh PD4 00h 00h 00ECh O0EOBh PD4 00h 00h 00Eh O0EOBh PD4 00h 00h 00F1h O0F2h PD4 00h 00h 00F3h P0F3h | | Port Pu Direction Register | | |
| 00E5h Port P3 Register P3 XXh 00E6h Port P2 Direction Register PD2 00h 00E7h Port P3 Direction Register PD3 00h 00E8h Port P4 Register P4 XXh 00E9h P0E9h PD4 00h 00EAh Port P4 Direction Register PD4 00h 00EDh PD5 PD4 00h 00ECh PD6 PD7 PD8 PD8 00EDh PD8 PD9 PD9 PD9 PD9 PD9 00E0h PD4 PD9 | | | | |
| 00E6h Port P2 Direction Register PD2 00h 00E7h Port P3 Direction Register PD3 00h 00E8h Port P4 Register P4 XXh 00EAh Port P4 Direction Register PD4 00h 00EBh 00ECh 00 00 00ECh 00EDh 00EDh 00EDh 00EFh 00F0h 00F0h 00F0h 00F3h 00F3h 00F3h 00F3h 00F6h 00F7h 00F8h 00F8h 00F8h 00F8h 00F8h 00F8h 00F8h 00F8h 00F8h 00F8h 00FCh 00FDh 00FDh 00FDh 00FEh 00FDh 00FDh 00FDh | 00E4h | Port P2 Register | | XXh |
| 00E7h Port P3 Direction Register P4 XXh 00E8h Port P4 Register P4 XXh 00EAh Port P4 Direction Register PD4 00h 00EBh 00ECh 00 00 00EDh 00ECh 00ECh 00ECh 00EFh 00F0h 00ECh 00ECh 00F1h 00F3h 00F3h 00F3h 00F3h 00F4h 00F3h 00F3h 00F6h 00F8h 00F8h 00F8h 00F8h 00F8h 00F8h 00F8h 00FBh 00FCh 00FCh 00FCh 00FCh 00FCh 00FCh 00FCh | 00E5h | Port P3 Register | | XXh |
| 00E7h Port P3 Direction Register P4 XXh 00E8h Port P4 Register P4 XXh 00EAh Port P4 Direction Register PD4 00h 00EBh 00ECh 00 00 00EDh 00ECh 00ECh 00ECh 00EFh 00F0h 00ECh 00ECh 00F1h 00F3h 00F3h 00F3h 00F3h 00F4h 00F3h 00F3h 00F6h 00F8h 00F8h 00F8h 00F8h 00F8h 00F8h 00F8h 00FBh 00FCh 00FCh 00FCh 00FCh 00FCh 00FCh 00FCh | 00E6h | Port P2 Direction Register | PD2 | 00h |
| 00E8h Port P4 Register P4 XXh 00E9h 00EAh Port P4 Direction Register PD4 00h 00EBh 00ECh 00EDh 00EDh </td <td></td> <td>Port P3 Direction Register</td> <td></td> <td></td> | | Port P3 Direction Register | | |
| 00E9h O0EAh Port P4 Direction Register PD4 00h 00EBh O0ECh O0EDh O0EDh O0ECh O0EDh O0ECh O0EDh O0ECh O0ECh <td></td> <td></td> <td></td> <td></td> | | | | |
| 00EAh Port P4 Direction Register PD4 00h 00EBh | | Fort F4 Register | F4 | AAII |
| 00EBh 00ECh 00EDh 00Ebh 00EFh 00Eh 00F0h 00F0h 00F1h 00F2h 00F3h 00F4h 00F5h 00F6h 00F7h 00F8h 00F9h 00F9h 00FBh 00FCh 00FCh 00FDh | | | : | 0.01 |
| 00ECh 00EDh 00EFh 00Fh 00F0h 00F0h 00F1h 00F3h 00F3h 00F4h 00F6h 00F6h 00F7h 00F8h 00F9h 00F9h 00FBh 00FCh 00FCh 00FDh | | Port P4 Direction Register | PD4 | 00h |
| 00EDh 00EEh 00Fh 00F0h 00F0h 00F0h 00F1h 00F3h 00F3h 00F4h 00F5h 00F6h 00F7h 00F8h 00F9h 00FAh 00FBh 00FCh 00FDh 00FCh 00FDh 00FCh | | | | |
| 00EEh 00Fh 00F0h 00F0h 00F1h 00F0h 00F2h 00F3h 00F3h 00F4h 00F5h 00F6h 00F7h 00F8h 00F9h 00FAh 00FBh 00FCh 00FDh 00FCh 00FDh 00FCh 00FEh 00FCh | 00ECh | | | |
| 00EEh 00Fh 00F0h 00F0h 00F1h 00F0h 00F2h 00F3h 00F3h 00F4h 00F5h 00F6h 00F7h 00F8h 00F9h 00FAh 00FBh 00FCh 00FDh 00FCh 00FDh 00FCh 00FEh 00FCh | 00EDh | | | |
| 00EFh 00F0h 00F1h 00F2h 00F3h 00F4h 00F5h 00F6h 00F7h 00F8h 00F9h 00FBh 00FCh 00FDh 00FDh | | | | |
| 00F0h 00F1h 00F2h 00F3h 00F4h 00F5h 00F6h 00F7h 00F8h 00F9h 00F8h 00F8h 00FBh 00FCh 00FDh 00FEh | | | | |
| 00F1h 00F2h 00F3h 00F4h 00F4h 00F5h 00F6h 00F7h 00F8h 00F9h 00FAh 00FAh 00FBh 00FBh 00FBh 00FBh 00FCh 00FCh 00FDh 00FCh | | | | |
| 00F2h 00F3h 00F4h 00F5h 00F6h 00F6h 00F7h 00F8h 00F9h 00FAh 00FBh 00FBh 00FBh 00FBh 00FBh 00FBh 00FBh 00FBh 00FBh 00FCh 00FBh 00FBh 00FBh 00FBh 00FBh 00FBh 00FBh 00FBh 00FBh 00FBh 00FBh 00FBh | | | | |
| 00F3h | | | | |
| 00F4h 00F5h 00F6h 00F6h 00F7h 00F8h 00F9h 00FAh 00FAh 00FBh 00FCh 00FCh 00FDh 00FCh 00FEh 00FCh | | | | |
| 00F5h | 00F3h | | | |
| 00F5h | 00F4h | | | |
| 00F6h 00F7h 00F8h 00F9h 00F9h 00FAh 00FBh 00FCh 00FCh 00FDh 00FEh 00FEh | | | | |
| 00F7h | | 1 | | |
| 00F8h | | | | |
| 00F9h | | | | |
| 00FAh | | | | |
| 00FBh | | | | |
| 00FCh | 00FAh | | | |
| 00FCh | 00FBh | | | |
| 00FDh | | | | |
| 00FEh | | + | | + |
| | | | | |
| UUFFN | | | | |
| | 00FFh | | | |

X: Undefined

Note

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (1)

| | 5 | | |
|-------------------------|--|--------------|--------------|
| Address | Register | Symbol | After Reset |
| 0180h | Timer RA Pin Select Register | TRASR | 00h |
| 0181h | Timer RB/RC Pin Select Register | TRBRCSR | 00h |
| 0182h | Timer RC Pin Select Register 0 | TRCPSR0 | 00h |
| 0183h | Timer RC Pin Select Register 1 | TRCPSR1 | 00h |
| 0184h | - | | |
| 0185h | | | |
| 0186h | | | + |
| 0187h | | | |
| | LIADTO D' O L AD L'A | LICOR | 1001 |
| 0188h | UART0 Pin Select Register | U0SR | 00h |
| 0189h | | | |
| 018Ah | UART2 Pin Select Register 0 | U2SR0 | 00h |
| 018Bh | UART2 Pin Select Register 1 | U2SR1 | 00h |
| 018Ch | | | |
| 018Dh | | | |
| 018Eh | INT Interrupt Input Pin Select Register | INTSR | 00h |
| 018Fh | I/O Function Pin Select Register | PINSR | 00h |
| | 1/O Function Fin Select Register | | |
| 0190h | Low-Voltage Signal Mode Control Register | TSMR | 00h |
| 0191h | | | |
| 0192h | | | |
| 0193h | | | |
| 0194h | | | |
| 0195h | | | † |
| 0196h | | | + |
| | | | ļ |
| 0197h | | | 4 |
| 0198h | | | |
| 0199h | | | |
| 019Ah | | | |
| 019Bh | | | |
| 019Ch | | | |
| 019Dh | | | + |
| 019Eh | | | |
| | | | _ |
| 019Fh | | | |
| 01A0h | | | |
| 01A1h | | | |
| 01A2h | | | |
| 01A3h | | | 1 |
| 01A4h | | | |
| 01A5h | | | + |
| 01A6h | | | |
| | | | |
| 01A7h | | | |
| 01A8h | | | |
| 01A9h | | | |
| 01AAh | | | |
| 01ABh | | | |
| 01ACh | | | † |
| 01ADh | | | + |
| | | | |
| 01AEh | | | 4 |
| 01AFh | | | |
| 01B0h | | | |
| 01B1h | | | |
| 01B2h | Flash Memory Status Register | FST | 10000X00b |
| 01B3h | · · · | | |
| 01B4h | Flash Memory Control Register 0 | FMR0 | 00h |
| 01B5h | Flash Memory Control Register 1 | FMR1 | 00h |
| | | | |
| 01B6h | Flash Memory Control Register 2 | FMR2 | 00h |
| 01B7h | | | |
| 01B8h | | | |
| 01B9h | | | |
| 01BAh | | | |
| | I . | | + |
| 01BBh | | | |
| 01BBh | | | |
| 01BBh 01BCh | | | |
| 01BBh 01BCh 01BDh | | | |
| 01BBh 01BCh | | | |

X: Undefined

Note

1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (1)

| Address | Register | Symbol | After Reset |
|-----------------|--------------------------------------|--------|-------------|
| 02C0h | SCU Control Register 0 | SCUCR0 | 00h |
| 02C1h | SCU Mode Register | SCUMR | 00h |
| 02C2h | SCU Timing Control Register 0 | SCTCR0 | 00000011b |
| 02C3h | SCU Timing Control Register 1 | SCTCR1 | 0000001b |
| 02C4h | SCU Timing Control Register 2 | SCTCR2 | 00010000b |
| 02C5h | SCU Timing Control Register 3 | SCTCR3 | 00h |
| 02C6h | SCU Channel Control Register | SCHCR | 00h |
| 02C7h | SCU Channel Control Counter | SCUCHC | 00h |
| 02C8h | SCU Flag Register | SCUFR | 00h |
| 02C9h | SCU Status Counter | SCUSTC | 00h |
| 02CAh | SCU Secondary Counter Set Register | SCSCSR | 00000111b |
| 02CBh | SCU Secondary Counter | SCUSCC | 00000111b |
| 02CCh | | | |
| 02CDh | | | |
| 02CEh | SCU Destination Address Register | SCUDAR | 00h |
| 02CFh | | | 00001100b |
| 02D0h | SCU Data Buffer Register | SCUDBR | 00h |
| 02D1h | | | 00h |
| 02D2h | SCU Primary Counter | SCUPRC | 00h |
| 02D3h | | | 00h |
| 02D4h | | | |
| 02D5h | | | |
| 02D6h | | | |
| 02D7h | | | |
| 02D8h | | | |
| 02D9h | | | |
| 02DAh | | | |
| 02DBh | | | |
| 02DCh | Touch Sensor Input Enable Register 0 | TSIER0 | 00h |
| 02DDh | Touch Sensor Input Enable Register 1 | TSIER1 | 00h |
| 02DEh | Touch Sensor Input Enable Register 2 | TSIER2 | 00h |
| 02DFh | | | |
| : | | | |
| 2C00h | DTC Transfer Vector Area | | XXh |
| 2C01h | DTC Transfer Vector Area | | XXh |
| 2C02h | DTC Transfer Vector Area | | XXh |
| 2C03h | DTC Transfer Vector Area | | XXh |
| 2C04h | DTC Transfer Vector Area | | XXh |
| 2C05h | DTC Transfer Vector Area | | XXh |
| 2C06h | DTC Transfer Vector Area | | XXh |
| 2C07h | DTC Transfer Vector Area | | XXh |
| 2C08h | DTC Transfer Vector Area | | XXh |
| 2C09h | DTC Transfer Vector Area | | XXh |
| 2C0Ah | DTC Transfer Vector Area | | XXh |
| : | DTC Transfer Vector Area | | XXh |
| : | DTC Transfer Vector Area | | XXh |
| 2C3Ah | DTC Transfer Vector Area | | XXh |
| 2C3Bh | DTC Transfer Vector Area | | XXh |
| | DTC Transfer Vector Area | | XXh |
| 2C3Dh | DTC Transfer Vector Area | | XXh |
| 2C3Eh | DTC Transfer Vector Area | | XXh |
| 2C3Fh | DTC Transfer Vector Area | DTCDO | XXh |
| 2C40h | DTC Control Data 0 | DTCD0 | XXh |
| 2C41h | | | XXh |
| 2C42h | | | XXh |
| 2C43h 2C44h | | | XXh |
| | | | XXh |
| 2C45h | | | XXh |
| 2C46h | | | XXh XXh |
| 2C47h 2C48h | DTC Control Data 1 | DTCD1 | XXh |
| 2C48h | DIO CONITOI DATA I | וטטוט | XXh |
| 2C49fi 2C4Ah | | | XXh |
| 2C4An | | | XXh |
| 2C4Bn | | | XXh |
| 2C4Ch 2C4Dh | | | XXh |
| 2C4Dh 2C4Eh | | | XXh |
| 2C4En | | | XXh |
| 204FII | | | AAII |

X: Undefined

The blank areas are reserved and cannot be accessed by users.

Table 4.13 ID Code Areas and Option Function Select Area

| Address | Area Name | Symbol | After Reset |
|---------|---|--------|-------------|
| : | | | |
| FFDBh | Option Function Select Register 2 | OFS2 | (Note 1) |
| : | | | - |
| FFDFh | ID1 | | (Note 2) |
| : | • | | |
| FFE3h | ID2 | | (Note 2) |
| : | | | |
| FFEBh | ID3 | | (Note 2) |
| : | • | | |
| FFEFh | ID4 | | (Note 2) |
| : | • | | |
| FFF3h | ID5 | | (Note 2) |
| : | | | |
| FFF7h | ID6 | | (Note 2) |
| : | • | | • |
| FFFBh | ID7 | | (Note 2) |
| : | 1 | | |
| FFFFh | Option Function Select Register | OFS | (Note 1) |
| | <u>, . </u> | | |

^{1.} The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.

When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user. When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.

^{2.} The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh. When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user. When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

Table 5.2 Recommended Operating Conditions

| 0 | Description | | 0 1111 | Standard | | | 11-2 | | |
|-----------|--------------------------------|---------------------------|----------------|-----------------------|---------------------|----------|------|----------|------|
| Symbol | | Parameter | | | Conditions | Min. | Тур. | Max. | Unit |
| Vcc/AVcc | Supply voltage | | | | | 1.8 | | 5.5 | V |
| Vss/AVss | Supply voltage | | | | | _ | 0 | _ | V |
| VIH | Input "H" voltage | Other th | nan CMOS ir | put | | 0.8 Vcc | _ | Vcc | V |
| | | CMOS | | Input level selection | 4.0 V ≤ Vcc ≤ 5.5 V | 0.5 Vcc | _ | Vcc | V |
| | | input | switching | : 0.35 Vcc | 2.7 V ≤ Vcc < 4.0 V | 0.55 Vcc | _ | Vcc | V |
| | | | function | | 1.8 V ≤ Vcc < 2.7 V | 0.65 Vcc | | Vcc | V |
| | | | (I/O port) | Input level selection | 4.0 V ≤ Vcc ≤ 5.5 V | 0.65 Vcc | | Vcc | V |
| | | | | : 0.5 Vcc | 2.7 V ≤ Vcc < 4.0 V | 0.7 Vcc | | Vcc | V |
| | | | | | 1.8 V ≤ Vcc < 2.7 V | 0.8 Vcc | | Vcc | V |
| | | | | Input level selection | 4.0 V ≤ Vcc ≤ 5.5 V | 0.85 Vcc | | Vcc | V |
| | | | | : 0.7 Vcc | 2.7 V ≤ Vcc < 4.0 V | 0.85 Vcc | | Vcc | V |
| | | | | | 1.8 V ≤ Vcc < 2.7 V | 0.85 Vcc | _ | Vcc | V |
| | | Externa | l clock input | (XOUT) | | 1.2 | _ | Vcc | V |
| VIL | Input "L" voltage | Other th | an CMOS ir | nput | | 0 | _ | 0.2 Vcc | V |
| | | CMOS | Input level | Input level selection | 4.0 V ≤ Vcc ≤ 5.5 V | 0 | _ | 0.2 Vcc | V |
| | | input | switching | : 0.35 Vcc | 2.7 V ≤ Vcc < 4.0 V | 0 | _ | 0.2 Vcc | V |
| | | | function | | 1.8 V ≤ Vcc < 2.7 V | 0 | _ | 0.2 Vcc | V |
| | | | (I/O port) | Input level selection | 4.0 V ≤ Vcc ≤ 5.5 V | 0 | _ | 0.4 Vcc | V |
| | | | | : 0.5 Vcc | 2.7 V ≤ Vcc < 4.0 V | 0 | _ | 0.3 Vcc | V |
| | | | | | 1.8 V ≤ Vcc < 2.7 V | 0 | _ | 0.2 Vcc | V |
| | | | | Input level selection | 4.0 V ≤ Vcc ≤ 5.5 V | 0 | | 0.55 Vcc | V |
| | | | | : 0.7 Vcc | 2.7 V ≤ Vcc < 4.0 V | 0 | | 0.45 Vcc | V |
| | | | | | 1.8 V ≤ Vcc < 2.7 V | 0 | | 0.35 Vcc | V |
| | | Externa | l clock input | (XOUT) | | 0 | _ | 0.4 Vcc | V |
| IOH(sum) | Peak sum output "H" current | Sum of all pins IOH(peak) | | | | _ | _ | -160 | mA |
| IOH(sum) | Average sum output "H" current | Sum of | all pins Iон(а | vg) | | _ | _ | -80 | mA |
| IOH(peak) | Peak output "H" | Drive ca | apacity Low | | | _ | _ | -10 | mA |
| , , | current | | apacity High | | | _ | | -40 | mA |
| IOH(avg) | Average output | Drive ca | apacity Low | | | _ | | -5 | mA |
| | "H" current | Drive ca | apacity High | | | _ | _ | -20 | mA |
| IOL(sum) | Peak sum output "L" current | Sum of | all pins IOL(p | eak) | | _ | _ | 160 | mA |
| IOL(sum) | Average sum output "L" current | Sum of | all pins IOL(a | vg) | | _ | _ | 80 | mA |
| IOL(peak) | Peak output "L" | Drive ca | apacity Low | | | _ | _ | 10 | mA |
| | current | | apacity High | | | _ | _ | 40 | mA |
| IOL(avg) | Average output | Drive ca | apacity Low | | | _ | _ | 5 | mA |
| | "L" current | Drive ca | apacity High | | | _ | _ | 20 | mA |
| f(XIN) | XIN clock input osc | cillation fr | equency | | 2.7 V ≤ Vcc ≤ 5.5 V | _ | _ | 20 | MHz |
| | | | | | 1.8 V ≤ Vcc < 2.7 V | _ | _ | 5 | MHz |
| fOCO40M | When used as the | count so | urce for time | er RC ⁽³⁾ | 2.7 V ≤ Vcc ≤ 5.5 V | 32 | _ | 40 | MHz |
| fOCO-F | fOCO-F frequency | | | | 2.7 V ≤ Vcc ≤ 5.5 V | _ | _ | 20 | MHz |
| | | | | | 1.8 V ≤ Vcc < 2.7 V | _ | _ | 5 | MHz |
| _ | System clock frequ | iency | | | 2.7 V ≤ Vcc ≤ 5.5 V | _ | _ | 20 | MHz |
| | | • | | | 1.8 V ≤ Vcc < 2.7 V | _ | _ | 5 | MHz |
| f(BCLK) | CPU clock frequer | су | | | 2.7 V ≤ Vcc ≤ 5.5 V | _ | _ | 20 | MHz |
| | | - | | | 1.8 V ≤ Vcc < 2.7 V | _ | _ | 5 | MHz |

- 1. Vcc = 1.8 V to 5.5 V at Topr = -20°C to 85°C (N version), unless otherwise specified.
- 2. The average output current indicates the average value of current measured during 100 ms.
- 3. fOCO40M can be used as the count source for timer RC in the range of Vcc = 2.7 V to 5.5 V.

R8C/33T Group 5. Electrical Characteristics

Table 5.3 A/D Converter Characteristics

| Cymphol | Doromotor | | Cond | itiono | Standard | | | Unit |
|---------|---------------------------|-------------|---|---------------------------------------|----------|------|------|------|
| Symbol | Parameter | | Conditions | | Min. | Тур. | Max. | Unit |
| _ | Resolution | | Vref = AVcc | | _ | _ | 10 | Bit |
| _ | Absolute accuracy | 10-bit mode | Vref = AVcc = 5.0 V | AN0 to AN7 input AN8 to AN11 input | _ | _ | ±3 | LSB |
| | | | Vref = AVcc = 3.3 V | AN0 to AN7 input AN8 to AN11 input | _ | _ | ±5 | LSB |
| | | | Vref = AVcc = 3.0 V | AN0 to AN7 input AN8 to AN11 input | _ | _ | ±5 | LSB |
| | | | Vref = AVcc = 2.2 V | AN0 to AN7 input AN8 to AN11 input | _ | _ | ±5 | LSB |
| | | 8-bit mode | Vref = AVcc = 5.0 V | AN0 to AN7 input AN8 to AN11 input | _ | _ | ±2 | LSB |
| | | | Vref = AVcc = 3.3 V | AN0 to AN7 input AN8 to AN11 input | _ | _ | ±2 | LSB |
| | | | Vref = AVcc = 3.0 V | AN0 to AN7 input AN8 to AN11 input | _ | _ | ±2 | LSB |
| | | | Vref = AVcc = 2.2 V | AN0 to AN7 input AN8 to AN11 input | _ | _ | ±2 | LSB |
| φAD | A/D conversion clock | | 4.0 V ≤ Vref = AVcc ≤ 5.5 V (2) | | 2 | _ | 20 | MHz |
| | | | 3.2 V ≤ Vref = AVcc ≤ 5.5 V (2) | | 2 | _ | 16 | MHz |
| | | | | 2.7 V ≤ Vref = AVcc ≤ 5.5 V (2) | | _ | 10 | MHz |
| | | | 2.2 V ≤ Vref = AVcc ≤ 5.5 V (2) | | 2 | _ | 5 | MHz |
| _ | Tolerance level impedance | е | | | _ | 3 | _ | kΩ |
| tconv | Conversion time | 10-bit mode | Vref = AVcc = 5.0 V, ¢ | AD = 20 MHz | 2.2 | _ | _ | μS |
| | | 8-bit mode | Vref = AVcc = 5.0 V, (| AD = 20 MHz | 2.2 | | | ms |
| tsamp | Sampling time | | φAD = 20 MHz | | 8.0 | _ | _ | μS |
| IVref | Vref current | | Vcc = 5.0 V, XIN = f1 | = φAD = 20 MHz | _ | 45 | _ | μА |
| Vref | Reference voltage | | | | 2.2 | _ | AVcc | V |
| VIA | Analog input voltage (3) | | | | 0 | _ | Vref | V |
| OCVREF | On-chip reference voltage | | $2 \text{ MHz} \le \phi \text{AD} \le 4 \text{ MH}$ | z | 1.19 | 1.34 | 1.49 | V |

- 1. Vcc/AVcc = Vref = 2.2 V to 5.5 V, Vss = 0 V at Topr = -20°C to 85°C (N version), unless otherwise specified.
- 2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-consumption current mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
- 3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

R8C/33T Group 5. Electrical Characteristics

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

| Cumbal | Parameter | Conditions | | I lait | | |
|----------------------|--|----------------------------|-----------|--------|-----------------------------|-------|
| Symbol | Parameter | Conditions | Min. | Тур. | Max. | Unit |
| _ | Program/erase endurance (2) | | 1,000 (3) | _ | _ | times |
| _ | Byte program time | | _ | 80 | 500 | μS |
| _ | Block erase time | | _ | 0.3 | _ | S |
| td(SR-SUS) | Time delay from suspend request until suspend | | _ | _ | 5 + CPU clock × 3 cycles | ms |
| _ | Interval from erase start/restart until following suspend request | | 0 | _ | _ | μS |
| _ | Time from suspend until erase restart | | _ | _ | 30 + CPU clock × 1 cycle | μS |
| td(CMDRST -READY) | Time from when command is forcibly terminated until reading is enabled | | _ | _ | 30 + CPU clock × 1 cycle | μS |
| _ | Program, erase voltage | | 2.7 | _ | 5.5 | V |
| _ | Read voltage | | 1.8 | _ | 5.5 | V |
| _ | Program, erase temperature | | 0 | _ | 60 | °C |
| _ | Data hold time (7) | Ambient temperature = 55°C | 20 | _ | _ | year |

Notes:

- 1. Vcc = 2.7 V to 5.5 V at Topr = 0°C to 60°C, unless otherwise specified.
- 2. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | | Unit | | |
|----------|---|---|------|------|------|-------|
| Syllibol | Faranietei | Condition | Min. | Тур. | Max. | Offic |
| Vdet0 | Voltage detection level Vdet0_0 (2) | | 1.80 | 1.90 | 2.05 | V |
| | Voltage detection level Vdet0_1 (2) | | 2.15 | 2.35 | 2.50 | V |
| | Voltage detection level Vdet0_2 (2) | | 2.70 | 2.85 | 3.05 | V |
| | Voltage detection level Vdet0_3 (2) | | 3.55 | 3.80 | 4.05 | V |
| _ | Voltage detection 0 circuit response time (4) | At the falling of Vcc from 5 V to (Vdet0_0 - 0.1) V | _ | 6 | 150 | μS |
| _ | Voltage detection circuit self power consumption | VCA25 = 1, Vcc = 5.0 V | _ | 1.5 | _ | μΑ |
| td(E-A) | Waiting time until voltage detection circuit operation starts (3) | | _ | _ | 100 | μS |

Notes:

- 1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20° C to 85°C (N version).
- 2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
- 3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
- 4. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | | Standard | I | Unit |
|---------|---|---|------|----------|------|------|
| Symbol | Parameter | Condition | Min. | Тур. | Max. | Unit |
| Vdet1 | Voltage detection level Vdet1_0 (2) | At the falling of Vcc | 2.00 | 2.20 | 2.40 | V |
| | Voltage detection level Vdet1_1 (2) | At the falling of Vcc | 2.15 | 2.35 | 2.55 | V |
| | Voltage detection level Vdet1_2 (2) | At the falling of Vcc | 2.30 | 2.50 | 2.70 | V |
| | Voltage detection level Vdet1_3 (2) | At the falling of Vcc | 2.45 | 2.65 | 2.85 | V |
| | Voltage detection level Vdet1_4 (2) | At the falling of Vcc | 2.60 | 2.80 | 3.00 | V |
| | Voltage detection level Vdet1_5 (2) | At the falling of Vcc | 2.75 | 2.95 | 3.15 | V |
| | Voltage detection level Vdet1_6 (2) | At the falling of Vcc | 2.85 | 3.10 | 3.40 | V |
| | Voltage detection level Vdet1_7 (2) | At the falling of Vcc | 3.00 | 3.25 | 3.55 | V |
| | Voltage detection level Vdet1_8 (2) | At the falling of Vcc | 3.15 | 3.40 | 3.70 | V |
| | Voltage detection level Vdet1_9 (2) | At the falling of Vcc | 3.30 | 3.55 | 3.85 | V |
| | Voltage detection level Vdet1_A (2) | At the falling of Vcc | 3.45 | 3.70 | 4.00 | V |
| | Voltage detection level Vdet1_B (2) | At the falling of Vcc | 3.60 | 3.85 | 4.15 | V |
| | Voltage detection level Vdet1_C (2) | At the falling of Vcc | 3.75 | 4.00 | 4.30 | V |
| | Voltage detection level Vdet1_D (2) | At the falling of Vcc | 3.90 | 4.15 | 4.45 | V |
| | Voltage detection level Vdet1_E (2) | At the falling of Vcc | 4.05 | 4.30 | 4.60 | V |
| | Voltage detection level Vdet1_F (2) | At the falling of Vcc | 4.20 | 4.45 | 4.75 | V |
| _ | Hysteresis width at the rising of Vcc in voltage | Vdet1_0 to Vdet1_5 selected | _ | 0.07 | _ | V |
| | detection 1 circuit | Vdet1_6 to Vdet1_F selected | _ | 0.10 | _ | V |
| | Voltage detection 1 circuit response time (3) | At the falling of Vcc from 5 V to (Vdet1_0 - 0.1) V | _ | 60 | 150 | μ\$ |
| _ | Voltage detection circuit self power consumption | VCA26 = 1, Vcc = 5.0 V | _ | 1.7 | _ | μΑ |
| td(E-A) | Waiting time until voltage detection circuit operation starts (4) | | _ | _ | 100 | μS |

- 1. The measurement condition is Vcc = 1.8 V to 5.5 V and $Topr = -20 ^{\circ}\text{C}$ to $85 ^{\circ}\text{C}$ (N version).
- 2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
- 3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
- 4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

| Table | 5 17 | Serial | Interface |
|--------------|--------|--------|-----------|
| Iable | J. I / | Seliai | michiace |

| Symbol | Parameter | Stan | Unit | |
|----------|------------------------|------|------|-------|
| Symbol | Falanetei | Min. | Max. | Offic |
| tc(CK) | CLKi input cycle time | 200 | _ | ns |
| tW(CKH) | CLKi input "H" width | 100 | _ | ns |
| tW(CKL) | CLKi input "L" width | 100 | _ | ns |
| td(C-Q) | TXDi output delay time | _ | 50 | ns |
| th(C-Q) | TXDi hold time | 0 | _ | ns |
| tsu(D-C) | RXDi input setup time | 50 | _ | ns |
| th(C-D) | RXDi input hold time | 90 | _ | ns |

i = 0 to 2

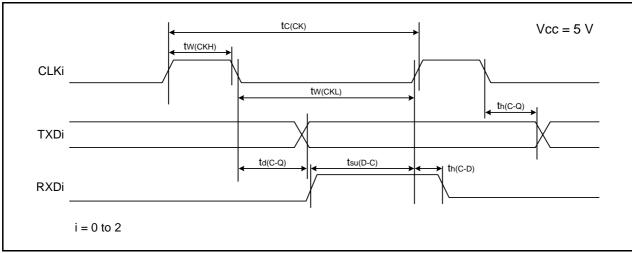


Figure 5.6 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.18 External Interrupt $\overline{\text{INTi}}$ (i = 0 to 3) Input, Key Input Interrupt $\overline{\text{Kli}}$ (i = 0 to 3)

| Symbol | Symbol Parameter | | Standard | | |
|---------|---|--------------------|----------|------|--|
| Symbol | Faidilletei | Min. | Max. | Unit | |
| tW(INH) | INTi input "H" width, Kli input "H" width | 250 ⁽¹⁾ | _ | ns | |
| tW(INL) | INTi input "L" width, Kli input "L" width | 250 (2) | - | ns | |

- 1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

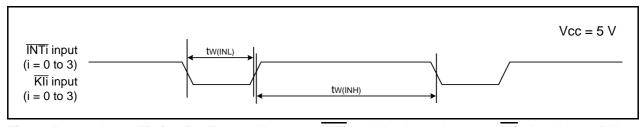


Figure 5.7 Input Timing for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 5 V

Table 5.19 Electrical Characteristics (3) [2.7 V \leq Vcc < 4.2 V]

| Symbol | | Parameter | Conditio | .n | Standard | | | Unit |
|----------|---------------------|--|--|---------------|-----------|---------------|------|------|
| Syllibol | | Falailletei | 5333 | | Min. | Min. Typ. Max | | |
| Vон | Output "H" | Other than XOUT | Drive capacity High | Iон = −5 mA | Vcc - 0.5 | _ | Vcc | V |
| | voltage | | Drive capacity Low | Iон = −1 mA | Vcc - 0.5 | _ | Vcc | V |
| | | XOUT | | IOH = -200 μA | 1.0 | _ | Vcc | V |
| Vol | Output "L" | Other than XOUT | Drive capacity High | IoL = 5 mA | _ | _ | 0.5 | V |
| | voltage | | Drive capacity Low | IoL = 1 mA | _ | _ | 0.5 | V |
| | | XOUT | | IOL = 200 μA | _ | _ | 0.5 | V |
| VT+-VT- | Hysteresis | INTO, INT1, INT2, INT3, KIO, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SCL2, SDA2 | Vcc = 3.0 V | | 0.1 | 0.4 | | V |
| | | RESET | Vcc = 3.0 V | | 0.1 | 0.5 | | V |
| Iн | Input "H" current | | $V_1 = 3 \text{ V}, \text{ Vcc} = 3.0 \text{ V}$ | | _ | | 4.0 | μΑ |
| lı∟ | Input "L" current | | $V_1 = 0 \ V, \ V_{CC} = 3.0 \ V$ | | _ | _ | -4.0 | μΑ |
| RPULLUP | Pull-up resis | stance | VI = 0 V, Vcc = 3.0 V | | 42 | 84 | 168 | kΩ |
| RfXIN | Feedback resistance | XIN | | | _ | 0.3 | | ΜΩ |
| VRAM | RAM hold v | oltage | During stop mode | | 1.8 | _ | | V |

^{1. 2.7} V ≤ Vcc < 4.2 V at Topr = −20°C to 85°C (N version), f(XIN) = 10 MHz, unless otherwise specified.

R8C/33T Group 5. Electrical Characteristics

Timing requirements

(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C)

Table 5.21 External Clock Input (XOUT)

| Symbol | Parameter | | Standard | |
|-----------|-----------------------|------|----------|------|
| Symbol | | Min. | Max. | Unit |
| tc(XOUT) | XOUT input cycle time | 50 | _ | ns |
| twh(xout) | XOUT input "H" width | 24 | _ | ns |
| twl(xout) | XOUT input "L" width | 24 | _ | ns |

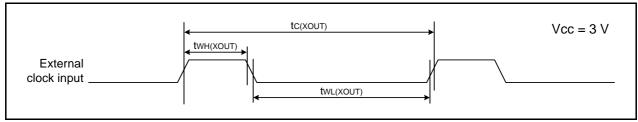


Figure 5.8 External Clock Input Timing Diagram when Vcc = 3 V

Table 5.22 TRAIO Input

| Symbol | Symbol Parameter | | Standard | |
|------------|------------------------|-----|----------|------|
| Symbol | | | Max. | Unit |
| tc(TRAIO) | TRAIO input cycle time | 300 | _ | ns |
| twh(traio) | TRAIO input "H" width | 120 | _ | ns |
| tWL(TRAIO) | TRAIO input "L" width | 120 | _ | ns |

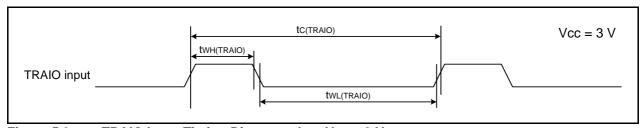


Figure 5.9 TRAIO Input Timing Diagram when Vcc = 3 V

| Table 5.23 Serial Interface |
|-----------------------------|
|-----------------------------|

| Symbol | Parameter | | Standard | | |
|----------|------------------------|------|----------|------|--|
| Symbol | raiainetei | Min. | Max. | Unit | |
| tc(CK) | CLKi input cycle time | 300 | _ | ns | |
| tW(CKH) | CLKi input "H" width | 150 | _ | ns | |
| tW(CKL) | CLKi Input "L" width | 150 | _ | ns | |
| td(C-Q) | TXDi output delay time | _ | 80 | ns | |
| th(C-Q) | TXDi hold time | 0 | _ | ns | |
| tsu(D-C) | RXDi input setup time | 70 | _ | ns | |
| th(C-D) | RXDi input hold time | 90 | _ | ns | |

i = 0 to 2

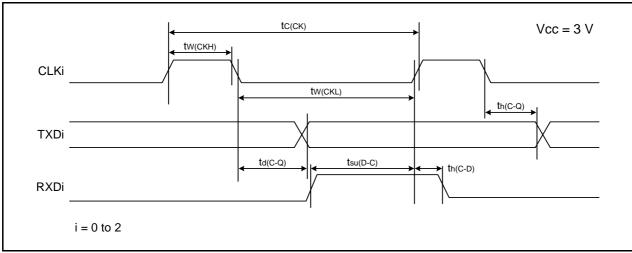


Figure 5.10 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.24 External Interrupt $\overline{\text{INTi}}$ (i = 0 to 3) Input, Key Input Interrupt $\overline{\text{Kli}}$ (i = 0 to 3)

| Symbol | Symbol Parameter | | Standard | | |
|---------|---|---------|----------|------|--|
| Symbol | Faidilletei | Min. | Max. | Unit | |
| tW(INH) | INTi input "H" width, Kli input "H" width | 380 (1) | _ | ns | |
| tW(INL) | INTi input "L" width, Kli input "L" width | 380 (2) | - | ns | |

- 1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

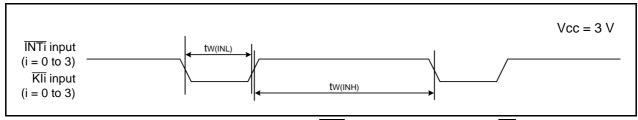
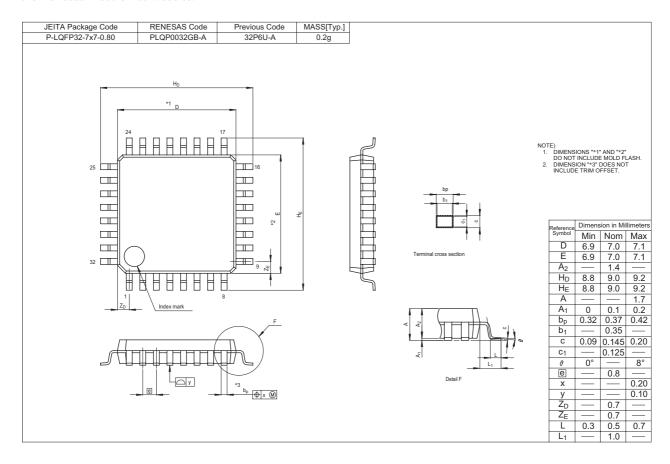


Figure 5.11 Input Timing for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 3 V

R8C/33T Group Package Dimensions

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Electronics website.



| RF\ | /121 | ON | HIST | TORY |
|-----|-------|-----|------|-------------|
| | / IOI | OIN | ПІО | |

R8C/33T Group Datasheet

| Rev. | Date | Description | |
|------|--------------|-------------|---|
| | | Page | Summary |
| 1.00 | Mar 16, 2010 | _ | First Edition issued |
| 1.10 | Apr 26, 2011 | All pages | "UART1" deleted |
| | | 3 | Table 1.2 revised, Note 1 deleted |
| | | 4 | Table 1.3, Note 1, Figure 1.1 revised |
| | | 5 | Figure 1.2 revised |
| | | 6 | Figure 1.3 revised |
| | | 7 | Table 1.4 revised |
| | | 8 | Table 1.5 revised |
| | | 12 | 3.1 "The internal ROM with address 0FFFFh." deleted |
| | | 14 | Table 4.2 revised |
| | | 18 | Table 4.6 revised |
| | | 19 | Table 4.7 revised |
| | | 26 | Table 5.1 revised |
| | | 27 | Note 1 revised |
| | | 29 | Table 5.3, Note 1 revised |
| | | 31 | Table 5.5, Note 1, Note 7 revised, and Note 8 added |
| | | 32 | Note 1 of Table 5.6 and Table 5.7 revised |
| | | 33 | Note 1 of Table 5.8 and Table 5.9 revised |
| | | 34 | Table 5.10, Note 1 of Table 5.10 and Table 5.11 revised |
| | | 35 | Table 5.13, Note 1 revised |
| | | 36 | Table 5.14 revised |
| | | 39 | Table 5.19, Note 1 revised |
| | | 40 | Table 5.20 revised |
| | | 43 | Table 5.25, Note 1 revised |
| | | 44 | Table 5.26 revised |
| | | | |

All trademarks and registered trademarks are the property of their respective owners.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

 The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

— When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Notice

- 1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
- 2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or
- 3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
- 4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the
- 5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
- 6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
- 7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc
 - Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools personal electronic equipment; and industrial robots.
 - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
 - Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical "Specific": implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
- 8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
- 9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult please evaluate the safety of the final products or system manufactured by you.
- 10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
- 11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics
- 12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.
- (Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries
- (Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics



SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information

enesas Electronics America Inc. 80 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A. dl: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited 1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited Dukes Meadow, Millboard Road, Boume End, Buckinghamshire, SL8 5FH, U.K Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-2035-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No. 1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-5887-7589

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2868-9318, Fax: +852-2886-9022/9044

Renesas Electronics Taiwan Co., Ltd. 13F, No. 363, Fu Shing North Road, Taipei, Taiv Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd. 1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632 Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd. 11F., Samik Lavied' or Bidg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea Tel: 482-2-558-3737, Fax: 482-2-558-5141