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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21336tnfp-30

1.2 Product List

Table 1.3 lists Product List for R8C/33T Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/33T Group.

Table 1.3 Product List for R8C/33T Group

Current of Apr 2011

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21334TNFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0032GB-A	N version
R5F21335TNFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0032GB-A	
R5F21336TNFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0032GB-A	
R5F21334TNXXXFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0032GB-A	N version Factory-programming product ⁽¹⁾
R5F21335TNXXXFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0032GB-A	
R5F21336TNXXXFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0032GB-A	

Note:

1. The user ROM is programmed before shipment.

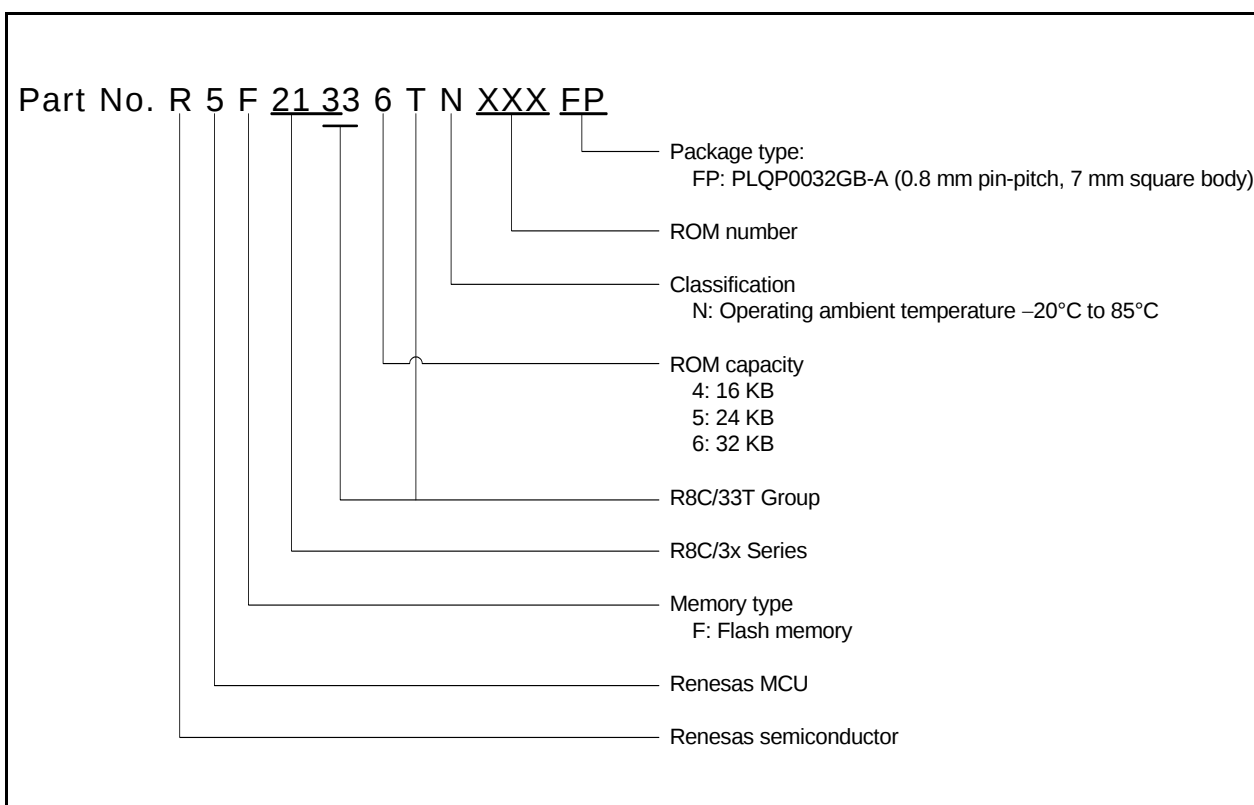


Figure 1.1 Part Number, Memory Size, and Package of R8C/33T Group

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.4 outlines the Pin Name Information by Pin Number.

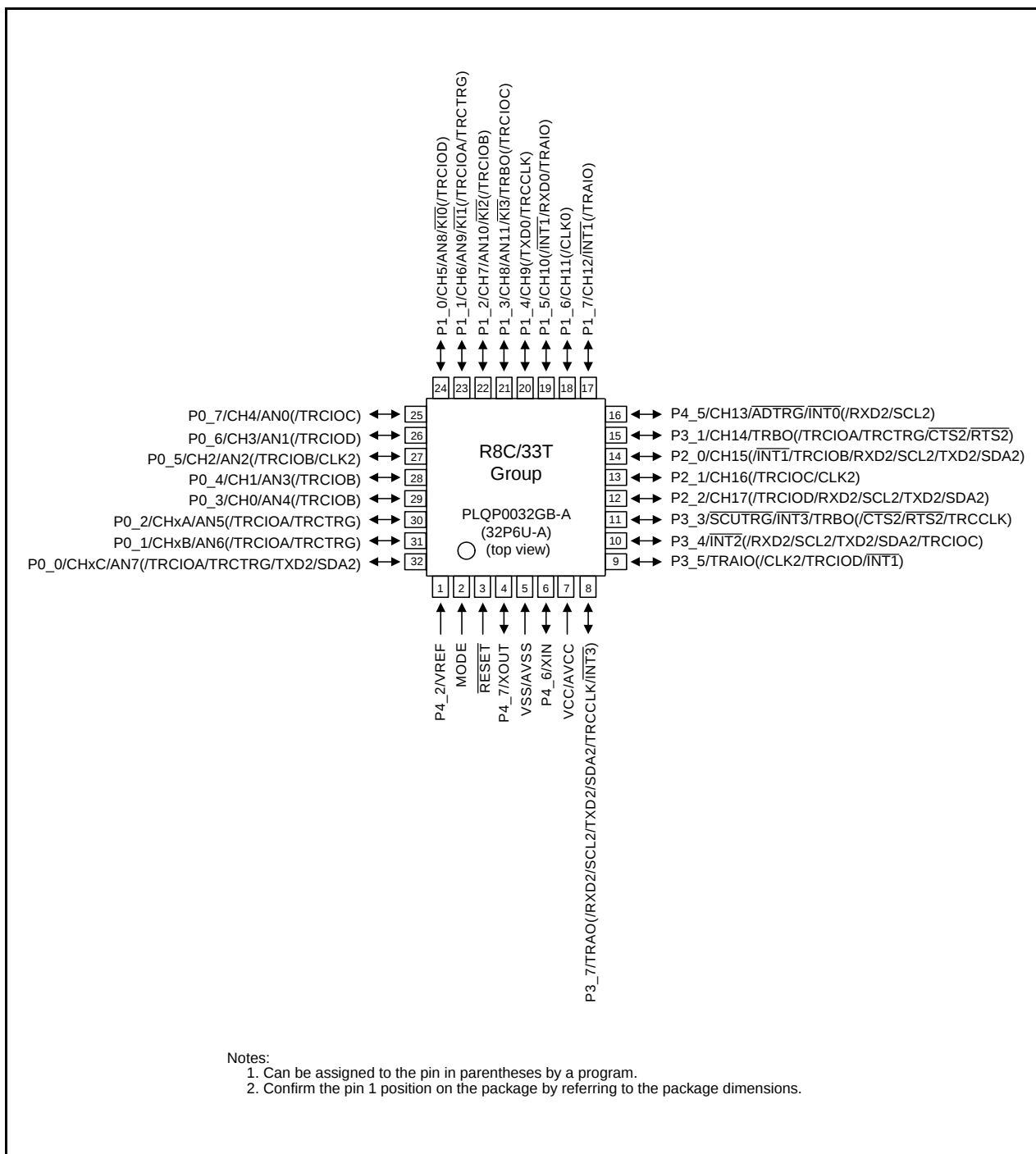


Figure 1.3 Pin Assignment (Top View)

1.5 Pin Functions

Table 1.5 lists Pin Functions.

Table 1.5 Pin Functions

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. ⁽¹⁾ To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
INT interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RB, and RC input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRA0	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Serial interface	CLK0, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD2	I	Serial data input pins
	TXD0, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I ² C mode clock I/O pin
	SDA2	I/O	I ² C mode data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
	$\overline{\text{ADTRG}}$	I	AD external trigger input pin
Sensor control unit	CHxA, CHxB, CHxC	I/O	Control pins for electrostatic capacitive touch detection
	CH0 to CH17	I	Electrostatic capacitive touch detection pins
	$\overline{\text{SCUTRG}}$	I	Sensor control unit external trigger input
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_2, P3_1, P3_3 to P3_5, P3_7, P4_5 to P4_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. All ports can be used as LED drive ports.
Input port	P4_2	I	Input-only port

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

Table 4.2 SFR Information (2) ⁽¹⁾

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah			
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh			
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah	Sensor Control Unit Interrupt Control Register	SCUIC	XXXXX000b
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.3 SFR Information (3) ⁽¹⁾

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h			
0119h			
011Ah			
011Bh			
011Ch			
011Dh			
011Eh			
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) ⁽¹⁾

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch			
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h	Low-Voltage Signal Mode Control Register	TSMR	00h
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) ⁽¹⁾

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h	Port P2 Drive Capacity Control Register	P2DRR	00h
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h			
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) ⁽¹⁾

Address	Register	Symbol	After Reset
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter			Conditions	Standard			Unit	
					Min.	Typ.	Max.		
Vcc/AVcc	Supply voltage				1.8	—	5.5	V	
Vss/AVss	Supply voltage				—	0	—	V	
VIH	Input “H” voltage	Other than CMOS input				0.8 Vcc	—	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	—	Vcc	V
			Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V	
			Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	—	Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	—	Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	—	Vcc	V	
	External clock input (XOUT)				1.2	—	Vcc	V	
VIL	Input “L” voltage	Other than CMOS input				0	—	0.2 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
			Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V	
			Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.55 Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0	—	0.45 Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0	—	0.35 Vcc	V	
	External clock input (XOUT)				0	—	0.4 Vcc	V	
IOH(sum)	Peak sum output “H” current	Sum of all pins IOH(peak)			—	—	−160	mA	
IOH(sum)	Average sum output “H” current	Sum of all pins IOH(avg)			—	—	−80	mA	
IOH(peak)	Peak output “H” current	Drive capacity Low			—	—	−10	mA	
		Drive capacity High			—	—	−40	mA	
IOH(avg)	Average output “H” current	Drive capacity Low			—	—	−5	mA	
		Drive capacity High			—	—	−20	mA	
IOL(sum)	Peak sum output “L” current	Sum of all pins IOL(peak)			—	—	160	mA	
IOL(sum)	Average sum output “L” current	Sum of all pins IOL(avg)			—	—	80	mA	
IOL(peak)	Peak output “L” current	Drive capacity Low			—	—	10	mA	
		Drive capacity High			—	—	40	mA	
IOL(avg)	Average output “L” current	Drive capacity Low			—	—	5	mA	
		Drive capacity High			—	—	20	mA	
f(XIN)	XIN clock input oscillation frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	
fOCO40M	When used as the count source for timer RC (3)			2.7 V ≤ Vcc ≤ 5.5 V	32	—	40	MHz	
fOCO-F	fOCO-F frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	
—	System clock frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	
f(BCLK)	CPU clock frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	

Notes:

1. V_{CC} = 1.8 V to 5.5 V at T_{opr} = −20°C to 85°C (N version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. f_{OCO40M} can be used as the count source for timer RC in the range of V_{CC} = 2.7 V to 5.5 V.

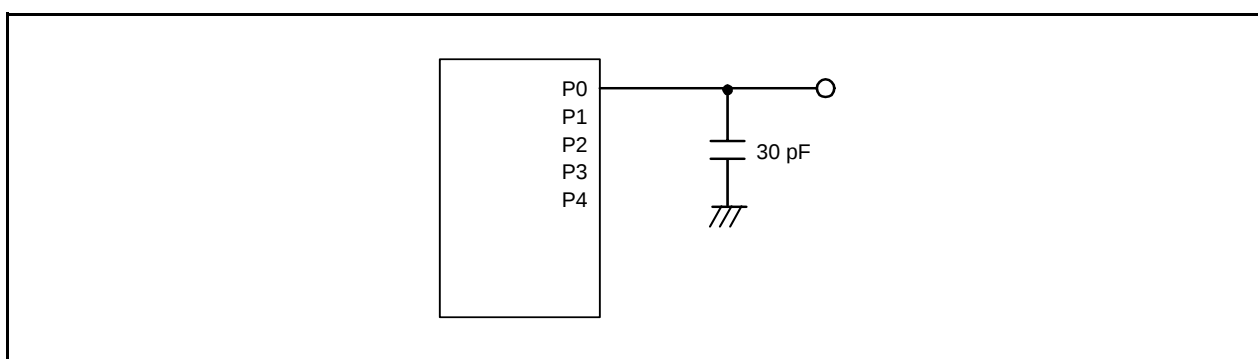


Figure 5.1 Ports P0 to P4 Timing Measurement Circuit

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVcc		—	—	10	Bit
—	Absolute accuracy	10-bit mode	Vref = AVcc = 5.0 V	AN0 to AN7 input AN8 to AN11 input	—	—	±3	LSB
			Vref = AVcc = 3.3 V	AN0 to AN7 input AN8 to AN11 input	—	—	±5	LSB
			Vref = AVcc = 3.0 V	AN0 to AN7 input AN8 to AN11 input	—	—	±5	LSB
			Vref = AVcc = 2.2 V	AN0 to AN7 input AN8 to AN11 input	—	—	±5	LSB
		8-bit mode	Vref = AVcc = 5.0 V	AN0 to AN7 input AN8 to AN11 input	—	—	±2	LSB
			Vref = AVcc = 3.3 V	AN0 to AN7 input AN8 to AN11 input	—	—	±2	LSB
			Vref = AVcc = 3.0 V	AN0 to AN7 input AN8 to AN11 input	—	—	±2	LSB
			Vref = AVcc = 2.2 V	AN0 to AN7 input AN8 to AN11 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ Vref = AVcc ≤ 5.5 V ⁽²⁾		2	—	20	MHz
			3.2 V ≤ Vref = AVcc ≤ 5.5 V ⁽²⁾		2	—	16	MHz
			2.7 V ≤ Vref = AVcc ≤ 5.5 V ⁽²⁾		2	—	10	MHz
			2.2 V ≤ Vref = AVcc ≤ 5.5 V ⁽²⁾		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVcc = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVcc = 5.0 V, φAD = 20 MHz		2.2	—	—	ms
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5.0 V, XIN = f1 = φAD = 20 MHz		—	45	—	μA
Vref	Reference voltage				2.2	—	AVcc	V
VIA	Analog input voltage ⁽³⁾				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

1. Vcc/AVcc = Vref = 2.2 V to 5.5 V, Vss = 0 V at Topr = −20°C to 85°C (N version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-consumption current mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	—	—	year

Notes:

1. V_{CC} = 2.7 V to 5.5 V at T_{opr} = 0°C to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time ⁽²⁾	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	—	20	150	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = –20°C to 85°C (N version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.9 Power-on Reset Circuit ⁽²⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
trth	External power Vcc rise gradient	(Note 1)	0	—	50000	mV/msec

Notes:

1. The measurement condition is Topr = –20°C to 85°C (N version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

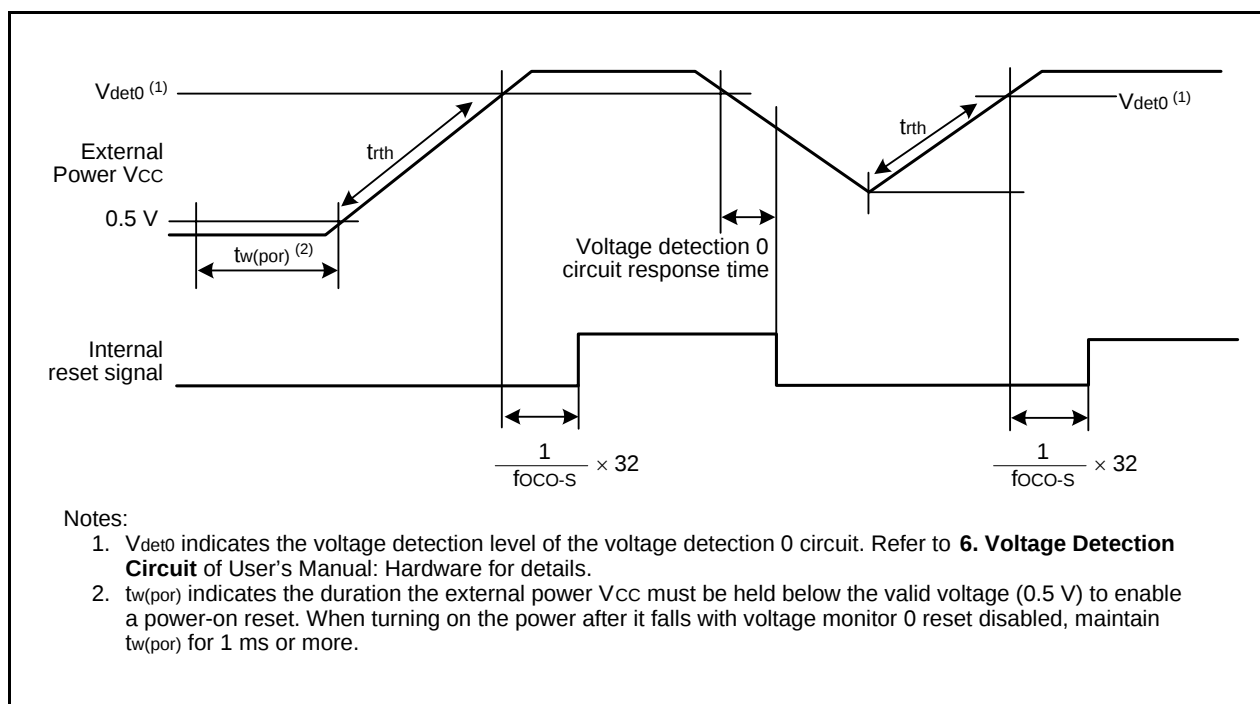
**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

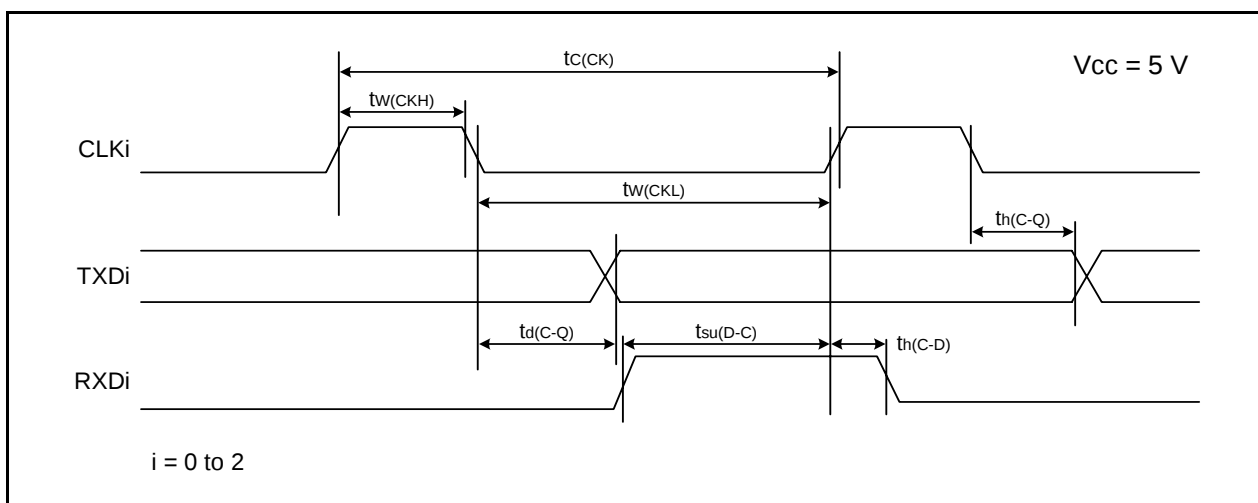
Table 5.14 Electrical Characteristics (2) [$3.3\text{ V} \leq V_{CC} \leq 5.5\text{ V}$]
($T_{opr} = -20^{\circ}\text{C}$ to 85°C (N version), unless otherwise specified.)

Symbol	Parameter	Condition			Standard			Unit
					Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 V to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	6.5	15	mA	
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	5.3	12.5	mA	
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.6	—	mA	
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3	—	mA	
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.2	—	mA	
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA	
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7	15	mA	
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3	—	mA	
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTTRD = MSTTRC = 1	—	1	—	mA	
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	400	μA	
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	100	μA	
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	90	μA	
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	μA	
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2	5.0	μA	
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	5	—	μA	

Table 5.17 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 2

**Figure 5.6 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.18 External Interrupt $\overline{INT_i}$ (i = 0 to 3) Input, Key Input Interrupt $\overline{KLi}$ (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input "H" width, $\overline{KLi}$ input "H" width	250 (1)	—	ns
$t_{w(INL)}$	$\overline{INT_i}$ input "L" width, $\overline{KLi}$ input "L" width	250 (2)	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INT_i}$ input filter select bit, use an $\overline{INT_i}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INT_i}$ input filter select bit, use an $\overline{INT_i}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

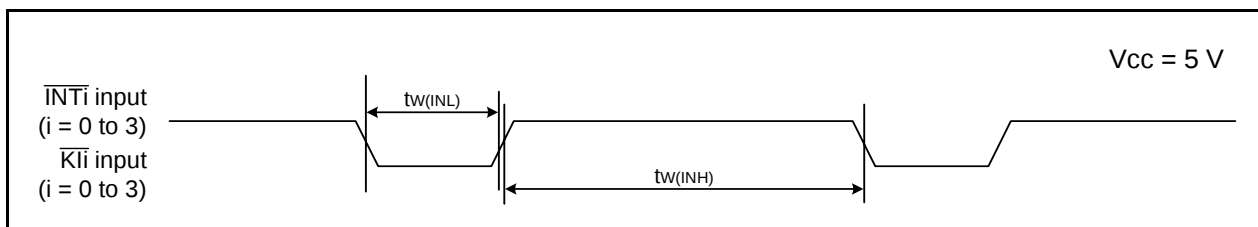
**Figure 5.7 Input Timing for External Interrupt $\overline{INT_i}$ and Key Input Interrupt $\overline{KLi}$ when Vcc = 5 V**

Table 5.19 Electrical Characteristics (3) [$2.7\text{ V} \leq V_{CC} < 4.2\text{ V}$]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I _{OH} = -5 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT		I _{OH} = -200 μ A	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I _{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
		XOUT		I _{OL} = 200 μ A	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}}, \overline{\text{INT3}}, \overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}}, \overline{\text{TRAIO}}, \overline{\text{TRBO}}, \overline{\text{TRCIOA}}, \overline{\text{TRCIOB}}, \overline{\text{TRCIOA}}, \overline{\text{TRCIOC}}, \overline{\text{TRCIOD}}, \overline{\text{TRCTRG}}, \overline{\text{TRCCLK}}, \overline{\text{ADTRG}}, \overline{\text{RXD0}}, \overline{\text{RXD2}}, \overline{\text{CLK0}}, \overline{\text{CLK2}}, \overline{\text{SCL2}}, \overline{\text{SDA2}}$	V _{CC} = 3.0 V		0.1	0.4	—	V
		RESET	V _{CC} = 3.0 V		0.1	0.5	—	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3.0 V		—	—	4.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3.0 V		—	—	-4.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3.0 V		42	84	168	k Ω
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. $2.7\text{ V} \leq V_{CC} < 4.2\text{ V}$ at T_{opr} = -20°C to 85°C (N version), f(XIN) = 10 MHz, unless otherwise specified.

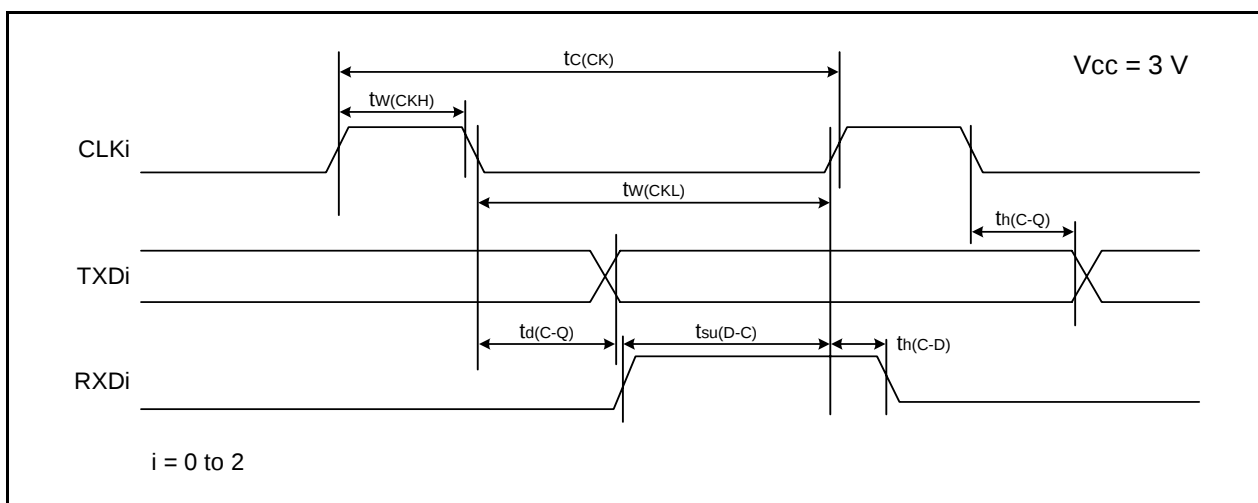
Table 5.20 Electrical Characteristics (4) [$2.7\text{ V} \leq V_{CC} < 3.3\text{ V}$]
($T_{opr} = -20^{\circ}\text{C}$ to 85°C (N version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current ($V_{CC} = 2.7\text{ V}$ to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	—	3.5	10	mA
			—	1.5	7.5	mA
		High-speed on-chip oscillator mode	—	7	15	mA
			—	3	—	mA
			—	4	—	mA
			—	1.5	—	mA
			—	1	—	mA
		Low-speed on-chip oscillator mode	—	90	390	μA
		Wait mode	—	15	90	μA
			—	4	80	μA
			—	3.5	—	μA
		Stop mode	—	2	5.0	μA
			—	5	—	μA

Table 5.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 2

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.24 External Interrupt $\overline{INT_i}$ (i = 0 to 3) Input, Key Input Interrupt $\overline{KLi}$ (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input "H" width, $\overline{KLi}$ input "H" width	380 (1)	—	ns
$t_{w(INL)}$	$\overline{INT_i}$ input "L" width, $\overline{KLi}$ input "L" width	380 (2)	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INT_i}$ input filter select bit, use an $\overline{INT_i}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INT_i}$ input filter select bit, use an $\overline{INT_i}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

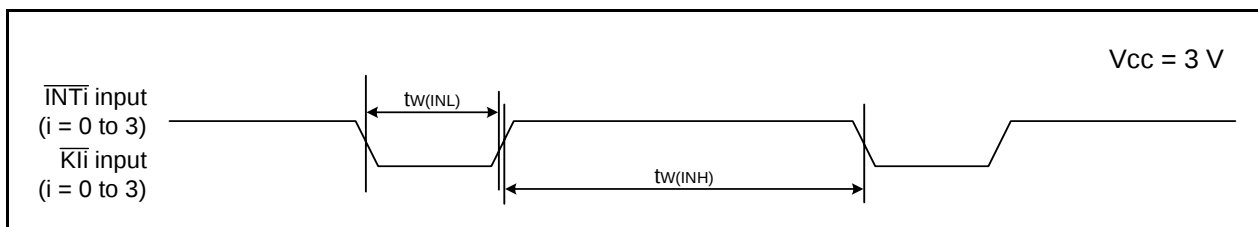
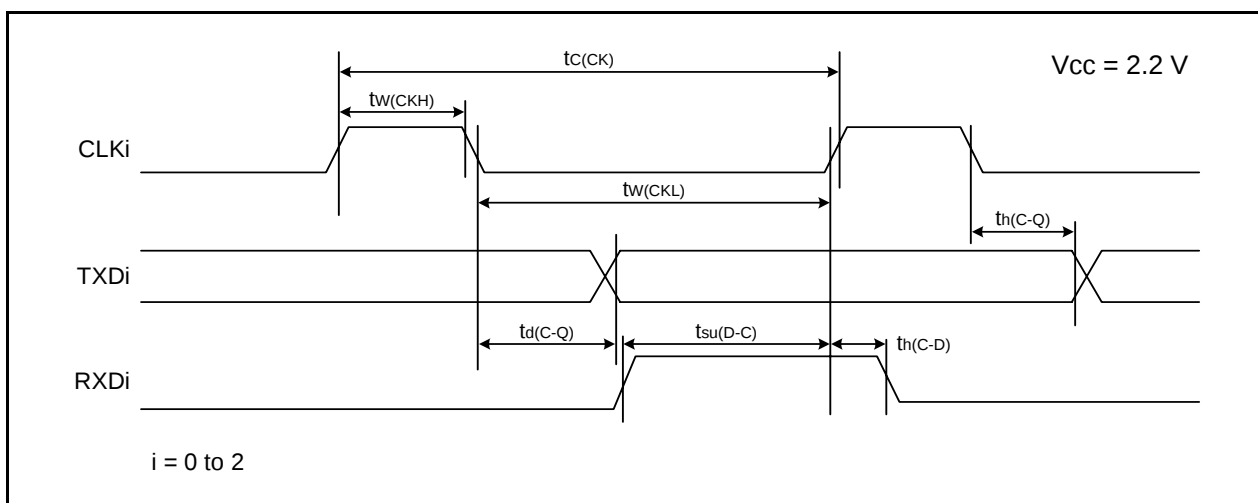
**Figure 5.11 Input Timing for External Interrupt $\overline{INT_i}$ and Key Input Interrupt $\overline{KLi}$ when Vcc = 3 V**

Table 5.29 Serial Interface

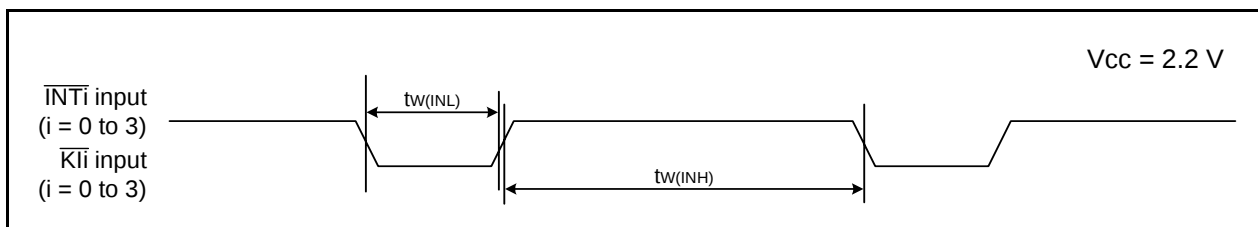
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.14 Serial Interface Timing Diagram when $V_{cc} = 2.2 \text{ V}$** **Table 5.30 External Interrupt $\overline{INTi}$ ($i = 0 \text{ to } 3$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0 \text{ to } 3$)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	1000 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	1000 ⁽²⁾	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

**Figure 5.15 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when $V_{cc} = 2.2 \text{ V}$**