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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Cap Sense, POR, PWM, Temp Sensor, WDT
Number of I/O	39
Program Memory Size	15KB (15K x 8)
Program Memory Type	FLASH
EEPROM Size	32 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f704-gq

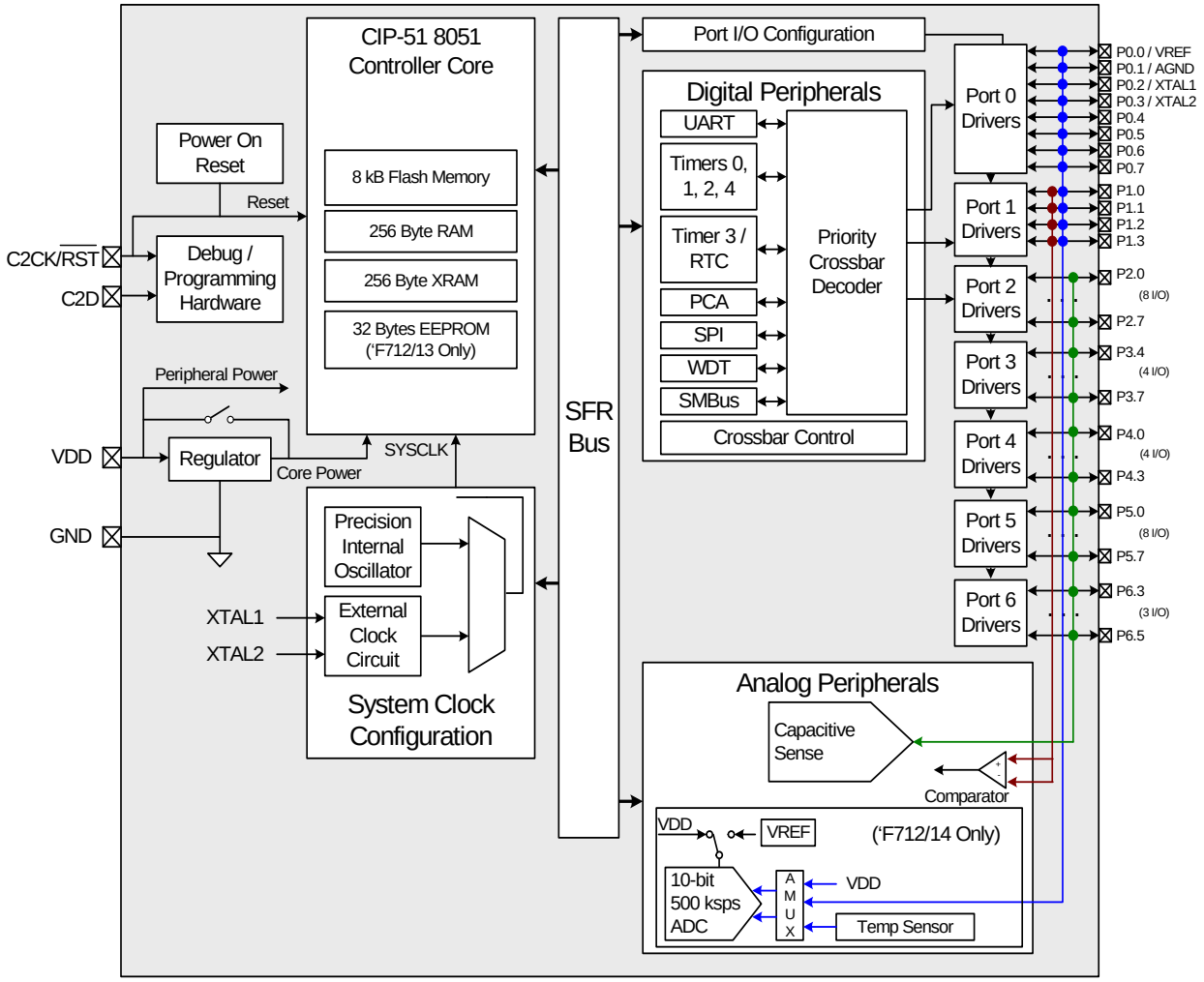

Figure 1.6. C8051F712/13/14/15 Block Diagram

7. QFN-32 Package Specifications

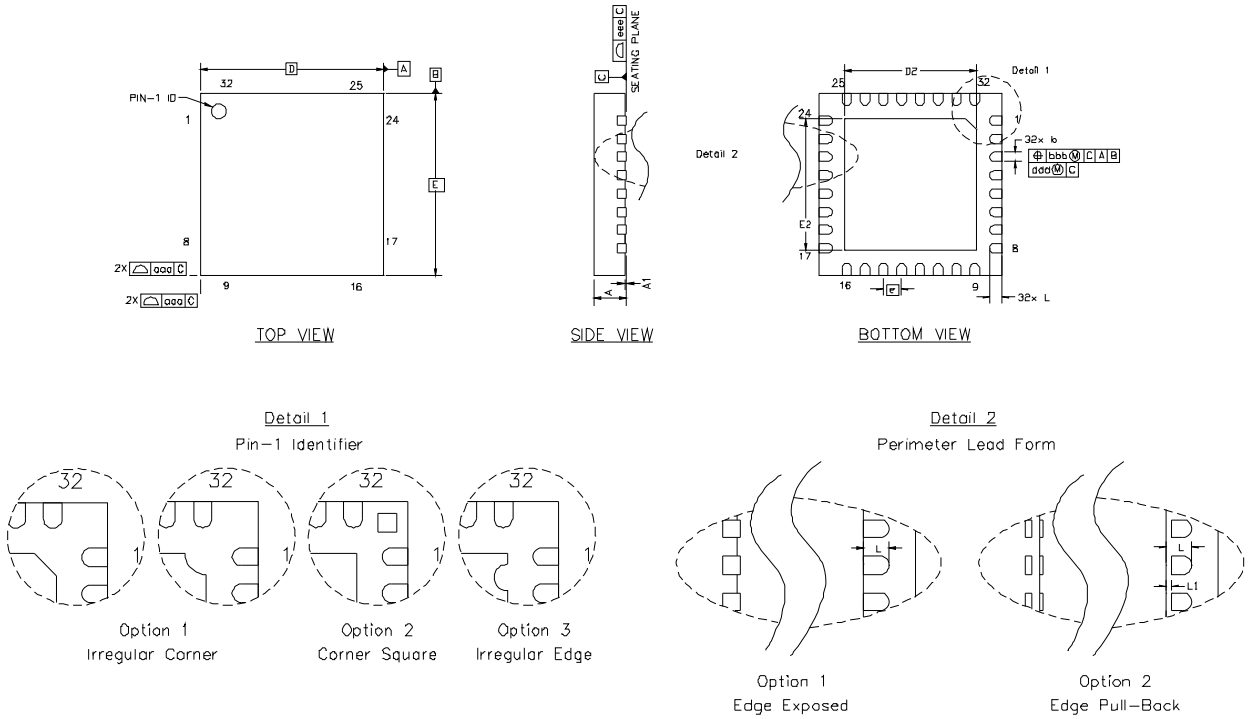

Figure 7.1. QFN-32 Package Drawing

Table 7.1. QFN-32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		5.00 BSC.	
D2	3.50	3.60	3.70
e		0.50 BSC.	
E		5.00 BSC.	

Dimension	Min	Typ	Max
E2	3.50	3.60	3.70
L	0.30	0.35	0.40
L1	0.00	—	0.10
aaa		0.15	
bbb		0.10	
ddd		0.05	
eee		0.08	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, L and L1 which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Electrical Characteristics

9.1. Absolute Maximum Specifications

Table 9.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on $\overline{\text{RST}}$ or any Port I/O Pin (except P0.3) with respect to GND		–0.3	—	V_{DD} + 2.0	V
Voltage on P0.3 with respect to GND		–0.3	—	V_{DD} + 0.3	V
Voltage on V_{DD} with respect to GND	Regulator in Normal Mode Regulator in Bypass Mode	–0.3 –0.3	— —	4.2 1.98	V V
Maximum Total current through V_{DD} and GND		—	—	500	mA
Maximum output current sunk by $\overline{\text{RST}}$ or any Port pin		—	—	100	mA

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

10.5. ADC0 Analog Multiplexer

ADC0 on the C8051F700/2/4/6/8 and C8051F710/2/4/6 uses an analog input multiplexer to select the positive input to the ADC. Any of the following may be selected as the positive input: Port 0 or Port 1 I/O pins, the on-chip temperature sensor, or the positive power supply (V_{DD}). The ADC0 input channel is selected in the ADC0MX register described in SFR Definition 10.9.

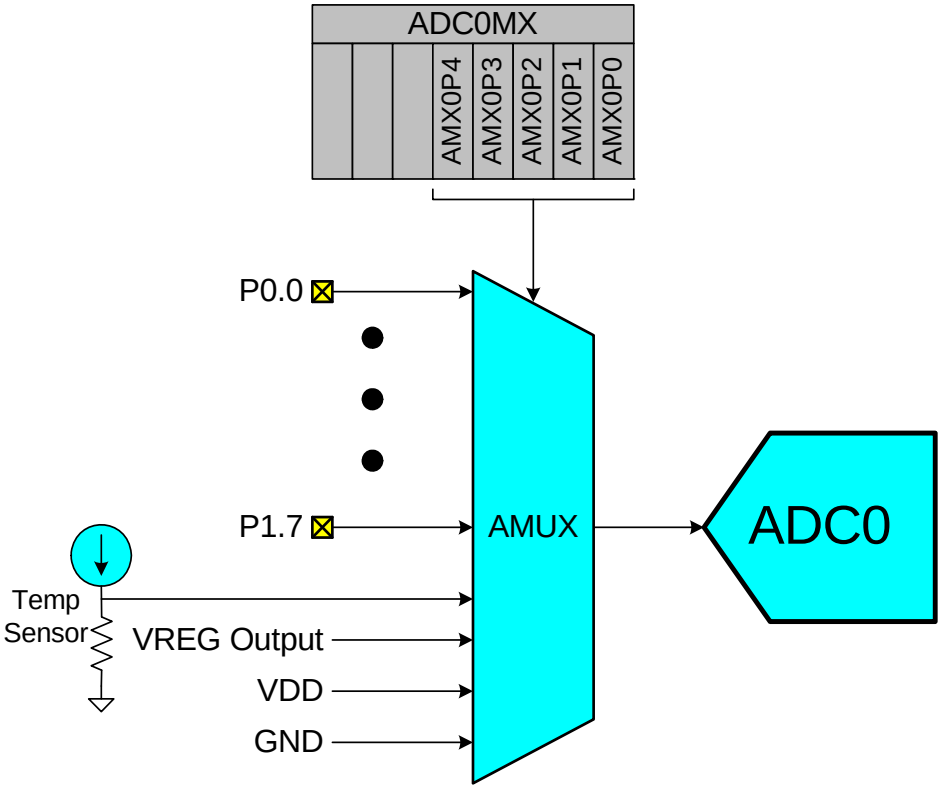

Figure 10.6. ADC0 Multiplexer Block Diagram

Important Note About ADC0 Input Configuration: Port pins selected as ADC0 inputs should be configured as analog inputs, and should be skipped by the Digital Crossbar. To configure a Port pin for analog input, set the corresponding bit in register PnMDIN to 0. To force the Crossbar to skip a Port pin, set the corresponding bit in register PnSKIP to 1. See Section “28. Port Input/Output” on page 180 for more Port I/O configuration details.

SFR Definition 15.1. CS0CN: Capacitive Sense Control

Bit	7	6	5	4	3	2	1	0
Name	CS0EN	CS0PME	CS0INT	CS0BUSY	CS0CMPEN			CS0CMPF
Type	R/W	R/W	R/W	R/W	R/W	R	R	R
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9A; SFR Page = 0

Bit	Name	Description
7	CS0EN	**CS0 Enable.** 0: CS0 disabled and in low-power mode. 1: CS0 enabled and ready to convert.
6	CS0PME	**CS0 Pin Monitor Event.** Set if any converter re-try requests have occurred due to a pin monitor event. This bit remains set until cleared by firmware.
5	CS0INT	**CS0 Interrupt Flag.** 0: CS0 has not completed a data conversion since the last time CS0INT was cleared. 1: CS0 has completed a data conversion. This bit is not automatically cleared by hardware.
4	CS0BUSY	**CS0 Busy.** Read: 0: CS0 conversion is complete or a conversion is not currently in progress. 1: CS0 conversion is in progress. Write: 0: No effect. 1: Initiates CS0 conversion if CS0CM[2:0] = 000b, 110b, or 111b.
3	CS0CMPEN	**CS0 Digital Comparator Enable Bit.** Enables the digital comparator, which compares accumulated CS0 conversion output to the value stored in CS0THH:CS0THL. 0: CS0 digital comparator disabled. 1: CS0 digital comparator enabled.
2:1	Unused	Read = 00b; Write = Don't care
0	CS0CMPF	**CS0 Digital Comparator Interrupt Flag.** 0: CS0 result is smaller than the value set by CS0THH and CS0THL since the last time CS0CMPF was cleared. 1: CS0 result is greater than the value set by CS0THH and CS0THL since the last time CS0CMPF was cleared.

19. In-System Device Identification

The C8051F70x/71x has SFRs that identify the device family and derivative. These SFRs can be read by firmware at runtime to determine the capabilities of the MCU that is executing code. This allows the same firmware image to run on MCUs with different memory sizes and peripherals, and dynamically changing functionality to suit the capabilities of that MCU.

In order for firmware to identify the MCU, it must read three SFRs. HWID describes the MCU's family, DERIVID describes the specific derivative within that device family, and REVID describes the hardware revision of the MCU.

SFR Definition 19.1. HWID: Hardware Identification Byte

Bit	7	6	5	4	3	2	1	0
Name	HWID[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	1	1	1	1	0

SFR Address = 0xC4; SFR Page = F

Bit	Name	Description
7:0	**HWID[7:0]**	**Hardware Identification Byte.** Describes the MCU family. 0x1E: Devices covered in this document (C8051F70x/71x)

SFR Definition 19.2. DERIVID: Derivative Identification Byte

Bit	7	6	5	4	3	2	1	0
Name	DERIVID[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SFR Address = 0xEC; SFR Page = F

Bit	Name	Description
7:0	**DERIVID[7:0]**	**Derivative Identification Byte.** Shows the C8051F70x/71x derivative being used. 0xD0: C8051F700; 0xD1: C8051F701; 0xD2: C8051F702; 0xD3: C8051F703 0xD4: C8051F704; 0xD5: C8051F705; 0xD6: C8051F706; 0xD7: C8051F707 0xD8: C8051F708; 0xD9: C8051F709; 0xDA: C8051F710; 0xDB: C8051F711 0xDC: C8051F712; 0xDD: C8051F713; 0xDE: C8051F714; 0xDF: C8051F715 0xE0: C8051F716; 0xE1: C8051F717

20. Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). The SFRs provide control and data exchange with the C8051F70x/71x's resources and peripherals. The CIP-51 controller core duplicates the SFRs found in a typical 8051 implementation as well as implementing additional SFRs used to configure and access the sub-systems unique to the C8051F70x/71x. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 20.1 lists the SFRs implemented in the C8051F70x/71x device family.

The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g., P0, TCON, SCON0, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the data sheet, as indicated in Table 20.2, for a detailed description of each register.

Table 20.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Page	Description	Page
P0MDIN	0xF1	F	Port 0 Input Mode Configuration	195
P0MDOUT	0xA4	F	Port 0 Output Mode Configuration	196
P0SKIP	0xD4	F	Port 0 Skip	196
P1	0x90	All Pages	Port 1 Latch	197
P1DRV	0xFA	F	Port 1 Drive Strength	199
P1MASK	0xE2	0	P0 Mask	193
P1MAT	0xE1	0	P1 Match	194
P1MDIN	0xF2	F	Port 1 Input Mode Configuration	198
P1MDOUT	0xA5	F	Port 1 Output Mode Configuration	198
P1SKIP	0xD5	F	Port 1 Skip	199
P2	0xA0	All Pages	Port 2 Latch	200
P2DRV	0xFB	F	Port 2 Drive Strength	202
P2MDIN	0xF3	F	Port 2 Input Mode Configuration	200
P2MDOUT	0xA6	F	Port 2 Output Mode Configuration	201
P2SKIP	0xD6	F	Port 2 Skip	201
P3	0xB0	All Pages	Port 3 Latch	202
P3DRV	0xFC	F	Port 3 Drive Strength	204
P3MDIN	0xF4	F	Port 3 Input Mode Configuration	203
P3MDOUT	0xAF	F	Port 3 Output Mode Configuration	203
P4	0xAC	All Pages	Port 4 Latch	204
P4DRV	0xFD	F	Port 4 Drive Strength	206
P4MDIN	0xF5	F	Port 4 Input Mode Configuration	205
P4MDOUT	0x9A	F	Port 4 Output Mode Configuration	205
P5	0xB3	All Pages	Port 5 Latch	206
P5DRV	0xFE	F	Port 5 Drive Strength	208
P5MDIN	0xF6	F	Port 5 Input Mode Configuration	207
P5MDOUT	0x9B	F	Port 5 Output Mode Configuration	207
P6	0xB2	All Pages	Port 6 Latch	208
P6DRV	0xC1	F	Port 6 Drive Strength	210
P6MDIN	0xF7	F	Port 6 Input Mode Configuration	209
P6MDOUT	0x9C	F	Port 6 Output Mode Configuration	209
PCA0CN	0xD8	All Pages	PCA Control	295
PCA0CPH0	0xFC	0	PCA Capture 0 High	300
PCA0CPH1	0xEA	0	PCA Capture 1 High	300
PCA0CPH2	0xEC	0	PCA Capture 2 High	300
PCA0CPL0	0xFB	0	PCA Capture 0 Low	300
PCA0CPL1	0xE9	0	PCA Capture 1 Low	300
PCA0CPL2	0xEB	0	PCA Capture 2 Low	300

SFR Definition 21.2. IP: Interrupt Priority

Bit	7	6	5	4	3	2	1	0
Name		PSPI0	PT2	PS0	PT1	PX1	PT0	PX0
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

SFR Address = 0xB8; SFR Page = All Pages; Bit-Addressable

Bit	Name	Function
7	Unused	Read = 1b, Write = Don't Care.
6	PSPI0	**Serial Peripheral Interface (SPI0) Interrupt Priority Control.** This bit sets the priority of the SPI0 interrupt. 0: SPI0 interrupt set to low priority level. 1: SPI0 interrupt set to high priority level.
5	PT2	**Timer 2 Interrupt Priority Control.** This bit sets the priority of the Timer 2 interrupt. 0: Timer 2 interrupt set to low priority level. 1: Timer 2 interrupt set to high priority level.
4	PS0	**UART0 Interrupt Priority Control.** This bit sets the priority of the UART0 interrupt. 0: UART0 interrupt set to low priority level. 1: UART0 interrupt set to high priority level.
3	PT1	**Timer 1 Interrupt Priority Control.** This bit sets the priority of the Timer 1 interrupt. 0: Timer 1 interrupt set to low priority level. 1: Timer 1 interrupt set to high priority level.
2	PX1	**External Interrupt 1 Priority Control.** This bit sets the priority of the External Interrupt 1 interrupt. 0: External Interrupt 1 set to low priority level. 1: External Interrupt 1 set to high priority level.
1	PT0	**Timer 0 Interrupt Priority Control.** This bit sets the priority of the Timer 0 interrupt. 0: Timer 0 interrupt set to low priority level. 1: Timer 0 interrupt set to high priority level.
0	PX0	**External Interrupt 0 Priority Control.** This bit sets the priority of the External Interrupt 0 interrupt. 0: External Interrupt 0 set to low priority level. 1: External Interrupt 0 set to high priority level.

SFR Definition 23.3. EECNTL: EEPROM Control

Bit	7	6	5	4	3	2	1	0
Name	EEEN					EEREAD	EEWRT	AUTOINC
Type	R/W	R				R/W		
Reset	0	0	0	0	0	0	0	1

SFR Address = 0xC5; SFR Page = F

Bit	Name	Description
7	EEEN	**EEPROM Enable.** 0: EEPROM control logic disabled. 1: EEPROM control logic enabled. EEPROM reads and writes can be performed.
6:4	Reserved	Reserved. Read = variable; Write = Don't Care
3	Reserved	Reserved. Read = 0b, Write = 0
2	EEREAD	**EEPROM 32-Byte Read.** 0: Does nothing. 1: 32 bytes of EEPROM Data will be read from Flash to internal RAM.
1	EEWRITE	**EEPROM 32-Byte Write.** 0: Does nothing. 1: 32 bytes of EEPROM Data will be written from internal RAM to Flash.
0	AUTOINC	**Auto Increment.** 0: Disable auto-increment. 1: Enable auto-increment.

SFR Definition 23.4. EEKEY: EEPROM Protect Key

Bit	7	6	5	4	3	2	1	0
Name	EEKEY						EEPSTATE/EEKEY	
Type	W						R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC6; SFR Page = F

Bit	Name	Description	Write	Read
7:0	EEKEY	**EEPROM Key.** Protects the EEPROM from inadvertent writes and erases.	The sequence 0x55 0xAA must be written to enable EEPROM writes and erases	
1:0	EEPSTATE	**EEPROM Protection State.** These bytes show whether Flash writes/erases have been enabled, disabled, or locked.		00: Write/Erase is not enabled 01: The first key has been written 10: Write/Erase is enabled 11: EEPROM is locked from further writes/erases

26. Watchdog Timer

The MCU includes a programmable Watchdog Timer (WDT) running off the system clock. A WDT overflow will force the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT will overflow and cause a reset.

Following a reset the WDT is automatically enabled and running with the default maximum time interval. If desired the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the /RST pin is unaffected by this reset.

The WDT consists of a 21-bit timer running from the programmed system clock. The timer measures the period between specific writes to its control register. If this period exceeds the programmed limit, a WDT reset is generated. The WDT can be enabled and disabled as needed in software, or can be permanently enabled if desired. Watchdog features are controlled via the Watchdog Timer Control Register (WDTCN) shown in SFR Definition 26.1.

26.1. Enable/Reset WDT

The watchdog timer is both enabled and reset by writing 0xA5 to the WDTCN register. The user's application software should include periodic writes of 0xA5 to WDTCN as needed to prevent a watchdog timer overflow. The WDT is enabled and reset as a result of any system reset.

26.2. Disable WDT

Writing 0xDE followed by 0xAD to the WDTCN register disables the WDT. The following code segment illustrates disabling the WDT:

```
CLR EA           ; disable all interrupts
MOV WDTCN,#0DEh  ; disable software watchdog timer
MOV WDTCN,#0ADh
SETB EA          ; re-enable interrupts
```

The writes of 0xDE and 0xAD must occur within 4 clock cycles of each other, or the disable operation is ignored. Interrupts should be disabled during this procedure to avoid delay between the two writes.

26.3. Disable WDT Lockout

Writing 0xFF to WDTCN locks out the disable feature. Once locked out, the disable operation is ignored until the next system reset. Writing 0xFF does not enable or reset the watchdog timer. Applications always intending to use the watchdog should write 0xFF to WDTCN in the initialization code.

26.4. Setting WDT Interval

WDTCN.[2:0] control the watchdog timeout interval. The interval is given by the following equation:

4^(3+WDTCN[2-0]) x Tsysclk ;where T_{sysclk} is the system clock period.

For a 3 MHz system clock, this provides an interval range of 0.021 to 349.5 ms. WDTCN.7 must be logic 0 when setting this interval. Reading WDTCN returns the programmed interval. WDTCN.[2:0] reads 111b after a system reset.

SFR Definition 27.1. CLKSEL: Clock Select

Bit	7	6	5	4	3	2	1	0
Name	CLKRDY	CLKDIV[2:0]			Reserved	CLKSEL[2:0]		
Type	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xBD; SFR Page= F

Bit	Name	Function
7	CLKRDY	**System Clock Divider Clock Ready Flag.** 0: The selected clock divide setting has not been applied to the system clock. 1: The selected clock divide setting has been applied to the system clock.
6:4	CLKDIV	**System Clock Divider Bits.** Selects the clock division to be applied to the selected source (internal or external). 000: Selected clock is divided by 1. 001: Selected clock is divided by 2. 010: Selected clock is divided by 4. 011: Selected clock is divided by 8. 100: Selected clock is divided by 16. 101: Selected clock is divided by 32. 110: Selected clock is divided by 64. 111: Selected clock is divided by 128.
3	Reserved	Read = 0b. Must write 0b.
2:0	CLKSEL[2:0]	**System Clock Select.** Selects the oscillator to be used as the undivided system clock source. 000: Internal Oscillator 001: External Oscillator All other values reserved.

SFR Definition 28.1. XBR0: Port I/O Crossbar Register 0

Bit	7	6	5	4	3	2	1	0
Name			CP0AE	CP0E	SYSCKE	SMB0E	SPI0E	URT0E
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE1; SFR Page = F

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care.
5	CP0AE	**Comparator0 Asynchronous Output Enable.** 0: Asynchronous CP0 unavailable at Port pin. 1: Asynchronous CP0 routed to Port pin.
4	CP0E	**Comparator0 Output Enable.** 0: CP0 unavailable at Port pin. 1: CP0 routed to Port pin.
3	SYSCKE	**$\overline{\text{SYSCLK}}$ Output Enable.** 0: $\overline{\text{SYSCLK}}$ unavailable at Port pin. 1: $\overline{\text{SYSCLK}}$ output routed to Port pin.
2	SMB0E	**SMBus I/O Enable.** 0: SMBus I/O unavailable at Port pins. 1: SMBus I/O routed to Port pins.
1	SPI0E	**SPI I/O Enable.** 0: SPI I/O unavailable at Port pins. 1: SPI I/O routed to Port pins. Note that the SPI can be assigned either 3 or 4 GPIO pins.
0	URT0E	**UART I/O Output Enable.** 0: UART I/O unavailable at Port pin. 1: UART TX0, RX0 routed to Port pins P0.4 and P0.5.

28.5. Port Match

Port match functionality allows system events to be triggered by a logic value change on P0 or P1. A software controlled value stored in the PnMATCH registers specifies the expected or normal logic values of P0 and P1. A Port mismatch event occurs if the logic levels of the Port's input pins no longer match the software controlled value. This allows Software to be notified if a certain change or pattern occurs on P0 or P1 input pins regardless of the XBRn settings.

The PnMASK registers can be used to individually select which P0 and P1 pins should be compared against the PnMATCH registers. A Port mismatch event is generated if (P0 & P0MASK) does not equal (P0MATCH & P0MASK) or if (P1 & P1MASK) does not equal (P1MATCH & P1MASK).

A Port mismatch event may be used to generate an interrupt or wake the device from a low power mode, such as IDLE or SUSPEND. See the Interrupts and Power Options chapters for more details on interrupt and wake-up sources.

SFR Definition 28.3. P0MASK: Port 0 Mask Register

Bit	7	6	5	4	3	2	1	0
Name	P0MASK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF4; SFR Page = 0

Bit	Name	Function
7:0	P0MASK[7:0]	**Port 0 Mask Value.** Selects P0 pins to be compared to the corresponding bits in P0MAT. 0: P0.n pin logic value is ignored and cannot cause a Port Mismatch event. 1: P0.n pin logic value is compared to P0MAT.n.

29.3. Preparing for a CRC Calculation

To prepare CRC0 for a CRC calculation, software should select the desired polynomial and set the initial value of the result. Two polynomials are available: 0x1021 (16-bit) and 0x04C11DB7 (32-bit). The CRC0 result may be initialized to one of two values: 0x00000000 or 0xFFFFFFFF. The following steps can be used to initialize CRC0.

1. Select a polynomial (Set CRC0SEL to 0 for 32-bit or 1 for 16-bit).
2. Select the initial result value (Set CRC0VAL to 0 for 0x00000000 or 1 for 0xFFFFFFFF).
3. Set the result to its initial value (Write 1 to CRC0INIT).

29.4. Performing a CRC Calculation

Once CRC0 is initialized, the input data stream is sequentially written to CRC0IN, one byte at a time. The CRC0 result is automatically updated after each byte is written. The CRC engine may also be configured to automatically perform a CRC on one or more Flash sectors. The following steps can be used to automatically perform a CRC on Flash memory.

1. Prepare CRC0 for a CRC calculation as shown above.
2. Write the index of the starting page to CRC0AUTO.
3. Set the AUTOEN bit in CRC0AUTO.
4. Write the number of Flash sectors to perform in the CRC calculation to CRC0CNT.

Note: Each Flash sector is 512 bytes.

5. Write any value to CRC0CN (or OR its contents with 0x00) to initiate the CRC calculation. The CPU will not execute code any additional code until the CRC operation completes.
6. Clear the AUTOEN bit in CRC0AUTO.
7. Read the CRC result using the procedure below.

29.5. Accessing the CRC0 Result

The internal CRC0 result is 32-bits (CRC0SEL = 0b) or 16-bits (CRC0SEL = 1b). The CRC0PNT bits select the byte that is targeted by read and write operations on CRC0DAT and increment after each read or write. The calculation result will remain in the internal CR0 result register until it is set, overwritten, or additional data is written to CRC0IN.

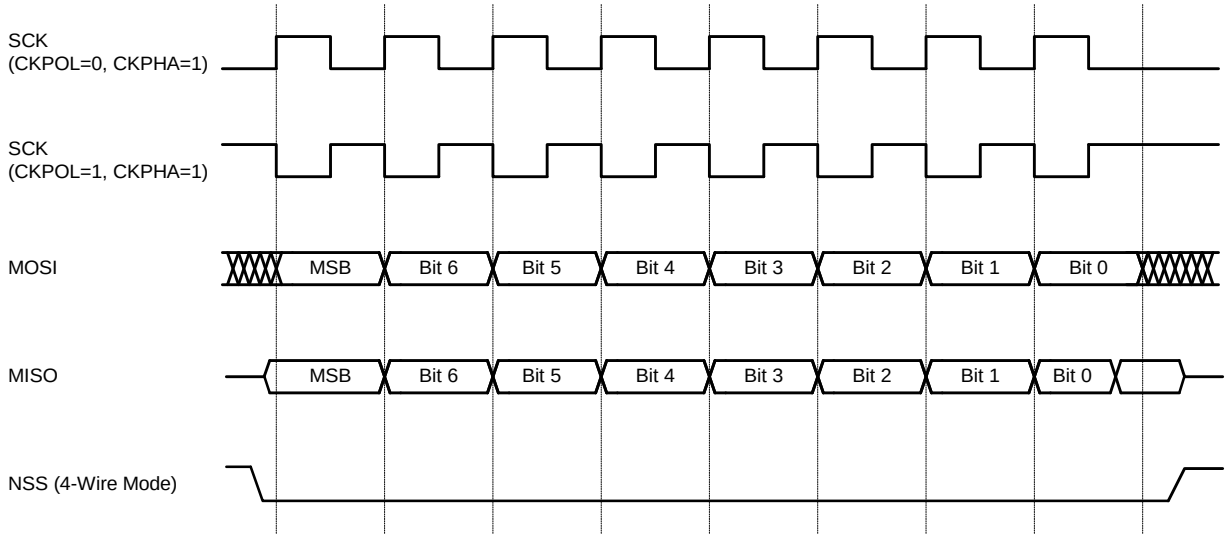

Figure 31.7. Slave Mode Data/Clock Timing (CKPHA = 1)

31.6. SPI Special Function Registers

SPI0 is accessed and controlled through four special function registers in the system controller: SPI0CN Control Register, SPI0DAT Data Register, SPI0CFG Configuration Register, and SPI0CKR Clock Rate Register. The four special function registers related to the operation of the SPI0 Bus are described in the following figures.

Table 31.1. SPI Slave Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode Timing (See Figure 31.8 and Figure 31.9)				
T_{MCKH}	SCK High Time	1 x T_{SYSCLK}	—	ns
T_{MCKL}	SCK Low Time	1 x T_{SYSCLK}	—	ns
T_{MIS}	MISO Valid to SCK Shift Edge	1 x T_{SYSCLK} + 20	—	ns
T_{MIH}	SCK Shift Edge to MISO Change	0	—	ns
Slave Mode Timing (See Figure 31.10 and Figure 31.11)				
T_{SE}	NSS Falling to First SCK Edge	2 x T_{SYSCLK}	—	ns
T_{SD}	Last SCK Edge to NSS Rising	2 x T_{SYSCLK}	—	ns
T_{SEZ}	NSS Falling to MISO Valid	—	4 x T_{SYSCLK}	ns
T_{SDZ}	NSS Rising to MISO High-Z	—	4 x T_{SYSCLK}	ns
T_{CKH}	SCK High Time	5 x T_{SYSCLK}	—	ns
T_{CKL}	SCK Low Time	5 x T_{SYSCLK}	—	ns
T_{SIS}	MOSI Valid to SCK Sample Edge	2 x T_{SYSCLK}	—	ns
T_{SIH}	SCK Sample Edge to MOSI Change	2 x T_{SYSCLK}	—	ns
T_{SOH}	SCK Shift Edge to MISO Change	—	4 x T_{SYSCLK}	ns
T_{SLH}	Last SCK Edge to MISO Change (CKPHA = 1 ONLY)	6 x T_{SYSCLK}	8 x T_{SYSCLK}	ns
Note: T_{SYSCLK} is equal to one period of the device system clock (SYSCLK).				

SFR Definition 33.11. TMR2L: Timer 2 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCC; SFR Page = 0

Bit	Name	Function
7:0	TMR2L[7:0]	**Timer 2 Low Byte.** In 16-bit mode, the TMR2L register contains the low byte of the 16-bit Timer 2. In 8-bit mode, TMR2L contains the 8-bit low byte timer value.

SFR Definition 33.12. TMR2H Timer 2 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCD; SFR Page = 0

Bit	Name	Function
7:0	TMR2H[7:0]	**Timer 2 Low Byte.** In 16-bit mode, the TMR2H register contains the high byte of the 16-bit Timer 2. In 8-bit mode, TMR2H contains the 8-bit high byte timer value.

34.3.5.2. 9/10/11-bit Pulse Width Modulator Mode

The duty cycle of the PWM output signal in 9/10/11-bit PWM mode should be varied by writing to an "Auto-Reload" Register, which is dual-mapped into the PCA0CPHn and PCA0CPLn register locations. The data written to define the duty cycle should be right-justified in the registers. The auto-reload registers are accessed (read or written) when the bit ARSEL in PCA0PWM is set to 1. The capture/compare registers are accessed when ARSEL is set to 0.

When the least-significant N bits of the PCA0 counter match the value in the associated module's capture/compare register (PCA0CPn), the output on CEXn is asserted high. When the counter overflows from the Nth bit, CEXn is asserted low (see Figure 34.9). Upon an overflow from the Nth bit, the COVF flag is set, and the value stored in the module's auto-reload register is loaded into the capture/compare register. The value of N is determined by the CLSEL bits in register PCA0PWM.

The 9, 10 or 11-bit PWM mode is selected by setting the ECOMn and PWMn bits in the PCA0CPMn register, and setting the CLSEL bits in register PCA0PWM to the desired cycle length (other than 8-bits). If the MATn bit is set to 1, the CCFn flag for the module will be set each time a comparator match (rising edge) occurs. The COVF flag in PCA0PWM can be used to detect the overflow (falling edge), which will occur every 512 (9-bit), 1024 (10-bit) or 2048 (11-bit) PCA clock cycles. The duty cycle for 9/10/11-Bit PWM Mode is given in Equation 34.2, where N is the number of bits in the PWM cycle.

Important Note About PCA0CPHn and PCA0CPLn Registers: When writing a 16-bit value to the PCA0CPn registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(2^N - PCA0CPn)}{2^N}$$

Equation 34.3. 9, 10, and 11-Bit PWM Duty Cycle

A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

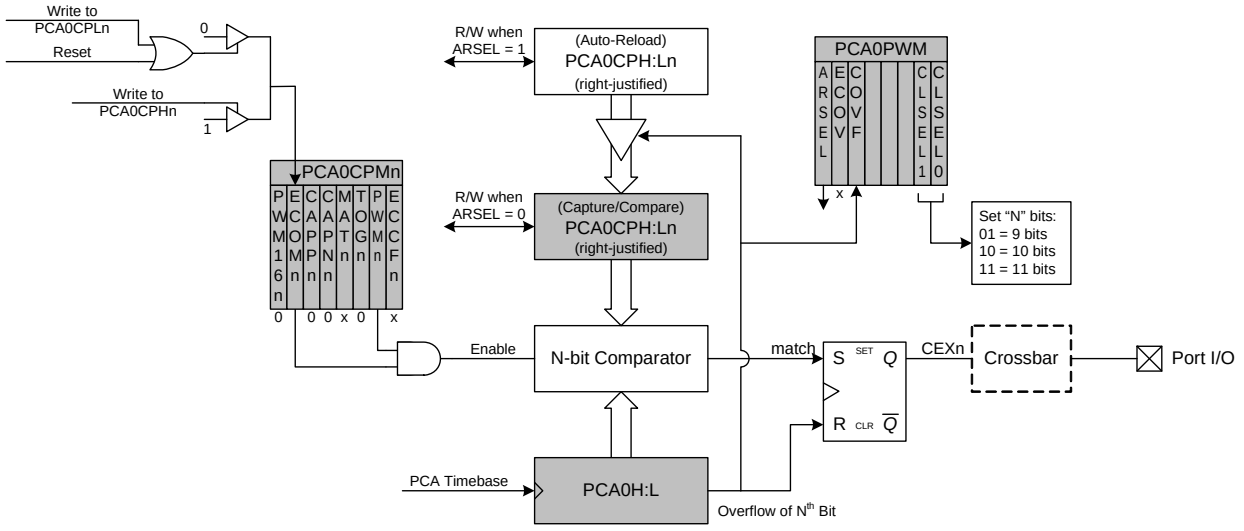

Figure 34.9. PCA 9, 10 and 11-Bit PWM Mode Diagram