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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	Cap Sense, POR, PWM, Temp Sensor, WDT
Number of I/O	54
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f710-gq

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



8. QFN-24 Package Specifications



Figure 8.1. QFN-24 Package Drawing

Dimension	Min	Тур	Max	Dimension	Min	Тур	Max
A	0.70	0.75	0.80	L	0.30	0.40	0.50
A1	0.00	0.02	0.05	L1	0.00		0.15
b	0.18	0.25	0.30	aaa	_	_	0.15
D		4.00 BSC.		bbb	_	—	0.10
D2	2.55	2.70	2.80	ddd	_	—	0.05
е		0.50 BSC.		eee	_	—	0.08
E	4.00 BSC.			Z	_	0.24	—
E2	2.55	2.70	2.80	Y	_	0.18	

Table 8.1. QFN-24 Package Dimensions

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



SFR Definition 10.9. ADC0MX: AMUX0 Channel Select

Bit	7	6	5	4	3	2	1	0	
Name				AMX0P[4:0]					
Туре	R	R	R		R/W				
Reset	0	0	0	1	1	1	1	1	

SFR Address = 0xBB; SFR Page = 0

Bit	Name		Fur	nction	
7:5	Unused	Read = 000b; Write	= Don't Care.		
4:0	AMX0P[4:0]	AMUX0 Positive In	put Selection.		
			64-Pin Devices	48-Pin Devices	32-Pin Devices
		00000	P0.0	P0.0	_
		00001	P0.1	P0.1	_
		00010	P0.2	P0.2	_
		00011	P0.3	P0.3	P0.3
		00100	P0.4	P0.4	P0.4
		00101	P0.5	P0.5	P0.5
		00110	P0.6	P0.6	_
		00111	P0.7	P0.7	_
		01000	P1.0	P1.0	_
		01001	P1.1	P1.1	_
		01010	P1.2	P1.2	_
		01011	P1.3	P1.3	_
		01100	P1.4	—	_
		01101	P1.5	—	_
		01110	P1.6	—	_
		01111	P1.7	—	_
		10000	Temp Sensor	Temp Sensor	Temp Sensor
		10001	VREG Output	VREG Output	VREG Output
		10010	VDD	VDD	VDD
		10011	GND	GND	GND
		10100–11111		no input selected	



SFR Definition 14.3. CPT0MX: Comparator0 MUX Selection

Bit	7	6	5	4	3	2		1	0	
Nam	e		CMX0N[2:0]				CMX	0P[2:0]		
Туре	, R		R/W R R/W							
Rese	et 0	0	0	0	0	0		0 0		
SFR A	ddress = 0x9	F; SFR Pa	ge = 0				•			
Bit	Name				Function					
7	Unused	Read = 0b	o; Write = don't c	are.						
6:4	CMX0N[2:0]	Compara	tor0 Negative Ir	nput MUX	Selection.					
			64-Pin Devices	s 48-Piı	n Devices	32-Pin Dev	ices	24-Pir	1 Devices	
		000	P1.1		P1.1	—			—	
		001	P1.3		P1.3	—			_	
		010	P1.5		_	—	- –		—	
		011	P1.7		—	P2.0 (see note)		P2.0 (see not		
		100-111	No input	No	o input	No input		No	o input	
			selected.	se	lected.	selected		se	ected.	
3	Unused	Read = $0t$; vvrite = don't c	are.						
2:0	CMX0P[2:0]	Compara	tor0 Positive In	put MUX	Selection.	•				
			64-Pin Devices	s 48-Pir	n Devices	32-Pin Devi	ices	24-Pir	1 Devices	
		000	P1.0		P1.0	—			—	
		001	P1.2		P1.2	—			—	
		010	P1.4			—			—	
		011	P1.6			(P1.6—see r	note)	(P1.6–	-see note)	
		100-111	No input	No	o input	No inpu	t	No input		
			selected.	se	lected.	selected		se	ected.	
Note:	On 32 and 24- near the GND the selection of desired supply internally.	pin devices, or VDD sup of P2.0 as th rail. Althou	P2.0 can be used ply rails. The P1.6 e negative input. F gh P1.6 is not con	as the neg setting for 1.6 should nected to a	ative compa the positive be configure device pin in	rator input, for o input should be ed for push-pull n these packag	detecti e used l mode es, it is	ing low-le in conju and driv s still a v	evel signals action with ven to the alid signal	



15. Capacitive Sense (CS0)

The Capacitive Sense subsystem uses a capacitance-to-digital circuit to determine the capacitance on a port pin. The module can take measurements from different port pins using the module's analog multiplexer. The module is enabled only when the CS0EN bit (CS0CN) is set to 1. Otherwise the module is in a low-power shutdown state. The module can be configured to take measurements on one port pin or a group of port pins, using auto-scan. A selectable gain circuit allows the designer to adjust the maximum allowable capacitance. An accumulator is also included, which can be configured to average multiple conversions on an input channel. Interrupts can be generated when CS0 completes a conversion or when the measured value crosses a threshold defined in CS0THH:L.



Figure 15.1. CS0 Block Diagram



15.8. Adjusting CS0 For Special Situations

There are several configuration options in the CS0 module designed to modify the operation of the circuit and address special situations. In particular, any circuit with more than 500 Ω of series impedance between the sensor and the device pin may require adjustments for optimal performance. Typical applications which may require adjustments include the following:

- Touch panel sensors fabricated using a resistive conductor such as indium-tin-oxide (ITO).
- Circuits using a high-value series resistor to isolate the sensor element for high ESD protection.

Most systems will require no fine tuning, and the default settings for CS0DT, CS0DR, and CS0IA should be used.



Mnemonic	Description	Bytes	Clock Cycles
Arithmetic Operations		1	•
ADD A, Rn	Add register to A	1	1
ADD A, direct	Add direct byte to A	2	2
ADD A, @Ri	Add indirect RAM to A	1	2
ADD A, #data	Add immediate to A	2	2
ADDC A, Rn	Add register to A with carry	1	1
ADDC A, direct	Add direct byte to A with carry	2	2
ADDC A, @Ri	Add indirect RAM to A with carry	1	2
ADDC A, #data	Add immediate to A with carry	2	2
SUBB A, Rn	Subtract register from A with borrow	1	1
SUBB A, direct	Subtract direct byte from A with borrow	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	1	2
SUBB A, #data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	2
INC @Ri	Increment indirect RAM	1	2
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	2
DEC @Ri	Decrement indirect RAM	1	2
INC DPTR	Increment Data Pointer	1	1
MUL AB	Multiply A and B	1	4
DIV AB	Divide A by B	1	8
DA A	Decimal adjust A	1	1
Logical Operations			
ANL A, Rn	AND Register to A	1	1
ANL A, direct	AND direct byte to A	2	2
ANL A, @Ri	AND indirect RAM to A	1	2
ANL A, #data	AND immediate to A	2	2
ANL direct, A	AND A to direct byte	2	2
ANL direct, #data	AND immediate to direct byte	3	3
ORL A, Rn	OR Register to A	1	1
ORL A, direct	OR direct byte to A	2	2
ORL A, @Ri	OR indirect RAM to A	1	2
ORL A, #data	OR immediate to A	2	2
ORL direct, A	OR A to direct byte	2	2
ORL direct, #data	OR immediate to direct byte	3	3
XRL A, Rn	Exclusive-OR Register to A	1	1
XRL A, direct	Exclusive-OR direct byte to A	2	2
XRL A, @Ri	Exclusive-OR indirect RAM to A	1	2
XRL A, #data	Exclusive-OR immediate to A	2	2
XRL direct, A	Exclusive-OR A to direct byte	2	2

Table 16.1. CIP-51 Instruction Set Summary







Figure 18.9. Multiplexed 8-Bit MOVX with Bank Select Timing





19. In-System Device Identification

The C8051F70x/71x has SFRs that identify the device family and derivative. These SFRs can be read by firmware at runtime to determine the capabilities of the MCU that is executing code. This allows the same firmware image to run on MCUs with different memory sizes and peripherals, and dynamically changing functionality to suit the capabilities of that MCU.

In order for firmware to identify the MCU, it must read three SFRs. HWID describes the MCU's family, DERIVID describes the specific derivative within that device family, and REVID describes the hardware revision of the MCU.

SFR Definition 19.1. HWID: Hardware Identification Byte

Bit	7	6	5	4	3	2	1	0
Name				HWI	D[7:0]			
Туре	R	R	R	R	R	R	R	R
Reset	0	0	0	1	1	1	1	0

SFR Address = 0xC4; SFR Page = F

Bit	Name	Description
7:0	HWID[7:0]	Hardware Identification Byte.
		Describes the MCU family. 0x1E: Devices covered in this document (C8051F70x/71x)

SFR Definition 19.2. DERIVID: Derivative Identification Byte

Bit	7	6	5	4	3	2	1	0
Name				DERIV	ID[7:0]			
Туре	R	R	R	R	R	R	R	R
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SFR Address = 0xEC; SFR Page = F

Name	Description
DERIVID[7:0]	Derivative Identification Byte.
	Shows the C8051F70x/71x derivative being used.
	0xD0: C8051F700; 0xD1: C8051F701; 0xD2: C8051F702; 0xD3: C8051F703
	0xD4: C8051F704; 0xD5: C8051F705; 0xD6: C8051F706; 0xD7: C8051F707
	0xD8: C8051F708; 0xD9: C8051F709; 0xDA: C8051F710; 0xDB: C8051F711
	0xDC: C8051F712; 0xDD: C8051F713; 0xDE: C8051F714; 0xDF: C8051F715
	0xE0: C8051F716; 0xE1: C8051F717
	Name DERIVID[7:0]



SFR Definition 21.2. IP: Interrupt Priority

Bit	7	6	5	4	3	2	1	0
Name		PSPI0	PT2	PS0	PT1	PX1	PT0	PX0
Туре	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

SFR Address = 0xB8; SFR Page = All Pages; Bit-Addressable

Bit	Name	Function
7	Unused	Read = 1b, Write = Don't Care.
6	PSPI0	Serial Peripheral Interface (SPI0) Interrupt Priority Control. This bit sets the priority of the SPI0 interrupt. 0: SPI0 interrupt set to low priority level. 1: SPI0 interrupt set to high priority level.
5	PT2	Timer 2 Interrupt Priority Control.This bit sets the priority of the Timer 2 interrupt.0: Timer 2 interrupt set to low priority level.1: Timer 2 interrupt set to high priority level.
4	PS0	UART0 Interrupt Priority Control. This bit sets the priority of the UART0 interrupt. 0: UART0 interrupt set to low priority level. 1: UART0 interrupt set to high priority level.
3	PT1	Timer 1 Interrupt Priority Control.This bit sets the priority of the Timer 1 interrupt.0: Timer 1 interrupt set to low priority level.1: Timer 1 interrupt set to high priority level.
2	PX1	External Interrupt 1 Priority Control. This bit sets the priority of the External Interrupt 1 interrupt. 0: External Interrupt 1 set to low priority level. 1: External Interrupt 1 set to high priority level.
1	PT0	Timer 0 Interrupt Priority Control.This bit sets the priority of the Timer 0 interrupt.0: Timer 0 interrupt set to low priority level.1: Timer 0 interrupt set to high priority level.
0	PX0	External Interrupt 0 Priority Control. This bit sets the priority of the External Interrupt 0 interrupt. 0: External Interrupt 0 set to low priority level. 1: External Interrupt 0 set to high priority level.



25.2. Power-Fail Reset / V_{DD} Monitor

When a power-down transition or power irregularity causes V_{DD} to drop below V_{RST} , the power supply monitor will drive the \overline{RST} pin low and hold the CIP-51 in a reset state (see Figure 25.2). When V_{DD} returns to a level above V_{RST} , the CIP-51 will be released from the reset state. Even though internal data memory contents are not altered by the power-fail reset, it is impossible to determine if V_{DD} dropped below the level required for data retention. If the PORSF flag reads 1, the data may no longer be valid. The V_{DD} monitor is enabled after power-on resets. Its defined state (enabled/disabled) is not altered by any other reset source. For example, if the V_{DD} monitor is disabled by code and a software reset is performed, the V_{DD} monitor will still be disabled after the reset.

Important Note: If the V_{DD} monitor is being turned on from a disabled state, it should be enabled before it is selected as a reset source. Selecting the V_{DD} monitor as a reset source before it is enabled and stabilized may cause a system reset. In some applications, this reset may be undesirable. If this is not desirable in the application, a delay should be introduced between enabling the monitor and selecting it as a reset source. The procedure for enabling the V_{DD} monitor and configuring it as a reset source from a disabled state is shown below:

- 1. Enable the V_{DD} monitor (VDMEN bit in VDM0CN = 1).
- 2. If necessary, wait for the V_{DD} monitor to stabilize.
- 3. Select the V_{DD} monitor as a reset source (PORSF bit in RSTSRC = 1).

See Figure 25.2 for V_{DD} monitor timing; note that the power-on-reset delay is not incurred after a V_{DD} monitor reset. See Section "9. Electrical Characteristics" on page 47 for complete electrical characteristics of the V_{DD} monitor.



SFR Definition 28.6. P1MAT: Port 1 Match Register

Bit	7	6	5	4	3	2	1	0
Name	P1MAT[7:0]							
Туре	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xE1; SFR Page = 0

Bit	Name	Function
7:0	P1MAT[7:0]	Port 1 Match Value.
		Match comparison value used on Port 1 for bits in P1MASK which are set to 1. 0: P1.n pin logic value is compared with logic LOW. 1: P1.n pin logic value is compared with logic HIGH.

28.6. Special Function Registers for Accessing and Configuring Port I/O

All Port I/O are accessed through corresponding special function registers (SFRs) that are both byte addressable and bit addressable. When writing to a Port, the value written to the SFR is latched to maintain the output data value at each pin. When reading, the logic levels of the Port's input pins are returned regardless of the XBRn settings (i.e., even when the pin is assigned to another signal by the Crossbar, the Port register can always read its corresponding Port I/O pin). The exception to this is the execution of the read-modify-write instructions that target a Port Latch register as the destination. The read-modify-write instructions when operating on a Port SFR are the following: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ and MOV, CLR or SETB, when the destination is an individual bit in a Port SFR. For these instructions, the value of the latch register (not the pin) is read, modified, and written back to the SFR.

Each Port has a corresponding PnSKIP register which allows its individual Port pins to be assigned to digital functions or skipped by the Crossbar. All Port pins used for analog functions, GPIO, or dedicated digital functions such as the EMIF should have their PnSKIP bit set to 1.

The Port input mode of the I/O pins is defined using the Port Input Mode registers (PnMDIN). Each Port cell can be configured for analog or digital I/O. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic.

The output driver characteristics of the I/O pins are defined using the Port Output Mode registers (PnMD-OUT). Each Port Output driver can be configured as either open drain or push-pull. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. The only exception to this is the SMBus (SDA, SCL) pins, which are configured as open-drain regardless of the PnMDOUT settings.



SFR Definition 28.13. P1MDIN: Port 1 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDIN[7:0]							
Туре	R/W							
Reset	1*	1	1	1	1	1	1	1

SFR Address = 0xF2; SFR Page = F

Bit	Name	Function			
7:0	P1MDIN[7:0]	Analog Configuration Bits for P1.7–P1.0 (respectively).			
		Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled.			
		0: Corresponding P1.n pin is configured for analog mode.			
		1: Corresponding P1.n pin is not configured for analog mode.			
Note:	 On C8051F716 and C8051F717 devices, P1.7 will default to analog mode. If the P1MDIN register is written on the C8051F716 and C8051F717 devices, P1.7 should always be configured as analog. 				

SFR Definition 28.14. P1MDOUT: Port 1 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDOUT[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA5; SFR Page = F

Bit	Name	Function
7:0	P1MDOUT[7:0]	Output Configuration Bits for P1.7–P1.0 (respectively).
		These bits are ignored if the corresponding bit in register P1MDIN is logic 0.
		0: Corresponding P1.n Output is open-drain.
		1: Corresponding P1.n Output is push-pull.



29. Cyclic Redundancy Check Unit (CRC0)

C8051F70x/71x devices include a cyclic redundancy check unit (CRC0) that can perform a CRC using a 16-bit or 32-bit polynomial. CRC0 accepts a stream of 8-bit data written to the CRC0IN register. CRC0 posts the 16-bit or 32-bit result to an internal register. The internal result register may be accessed indirectly using the CRC0PNT bits and CRC0DAT register, as shown in Figure 29.1. CRC0 also has a bit reverse register for quick data manipulation.



Figure 29.1. CRC0 Block Diagram



SFR Definition 29.1. CRC0CN: CRC0 Control

Bit	7	6	5	4	3	2	1	0
Name				CRC0SEL	CRC0INIT	CRC0VAL	CRC0P	NT[1:0]
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x91; SFR Page = F

Bit	Name	Function
7:5	Unused	Read = 000b; Write = Don't Care.
4	CRC0SEL	CRC0 Polynomial Select Bit.
		This bit selects the CRC0 polynomial and result length (32-bit or 16-bit). 0: CRC0 uses the 32-bit polynomial 0x04C11DB7 for calculating the CRC result
		1: CRC0 uses the 16-bit polynomial 0x1021 for calculating the CRC result.
3	CRC0INIT	CRC0 Result Initialization Bit.
		Writing a 1 to this bit initializes the entire CRC result based on CRC0VAL.
2	CRC0VAL	CRC0 Set Value Initialization Bit.
		This bit selects the set value of the CRC result.
		0: CRC result is set to 0x00000000 on write of 1 to CRC0INIT.
		1: CRC result is set to 0xFFFFFFF on write of 1 to CRC0INIT.
1:0	CRC0PNT[1:0]	CRC0 Result Pointer.
		Specifies the byte of the CRC result to be read/written on the next access to
		CRC0DAL. The value of these bits will auto-increment upon each read or write. For CRC0SEL = 0°
		00: CRC0DAT accesses bits 7–0 of the 32-bit CRC result.
		01: CRC0DAT accesses bits 15–8 of the 32-bit CRC result.
		10: CRC0DAT accesses bits 23–16 of the 32-bit CRC result.
		11: CRC0DAT accesses bits 31–24 of the 32-bit CRC result.
		For CRC0SEL = 1:
		00: CRC0DAT accesses bits 7–0 of the 16-bit CRC result.
		01: CRC0DAT accesses bits 15–8 of the 16-bit CRC result.
		10: CRC0DAT accesses bits 7–0 of the 16-bit CRC result.
		11: CRC0DAT accesses bits 15–8 of the 16-bit CRC result.



SMBCS1	SMBCS0	SMBus Clock Source
0	0	Timer 0 Overflow
0	1	Timer 1 Overflow
1	0	Timer 2 High Byte Overflow
1	1	Timer 2 Low Byte Overflow

Table 30.1. SMBus Clock Source Selection

The SMBCS1–0 bits select the SMBus clock source, which is used only when operating as a master or when the Free Timeout detection is enabled. When operating as a master, overflows from the selected source determine the absolute minimum SCL low and high times as defined in Equation 30.1.The selected clock source may be shared by other peripherals so long as the timer is left running at all times. For example, Timer 1 overflows may generate the SMBus and UART baud rates simultaneously. Timer configuration is covered in Section "33. Timers" on page 262.

$$T_{HighMin} = T_{LowMin} = \frac{1}{f_{ClockSourceOverflow}}$$

Equation 30.1. Minimum SCL High and Low Times

The selected clock source should be configured to establish the minimum SCL High and Low times as per Equation 30.1. When the interface is operating as a master (and SCL is not driven or extended by any other devices on the bus), the typical SMBus bit rate is approximated by Equation 30.2.

$$BitRate = \frac{f_{ClockSourceOverflow}}{3}$$

Equation 30.2. Typical SMBus Bit Rate

Figure 30.4 shows the typical SCL generation described by Equation 30.2. Notice that T_{HIGH} is typically twice as large as T_{LOW} . The actual SCL output may vary due to other devices on the bus (SCL may be extended low by slower slave devices, or driven low by contending master devices). The bit rate when operating as a master will never exceed the limits defined by equation Equation 30.1.



Figure 30.4. Typical SMBus SCL Generation

Setting the EXTHOLD bit extends the minimum setup and hold times for the SDA line. The minimum SDA setup time defines the absolute minimum time that SDA is stable before SCL transitions from low-to-high. The minimum SDA hold time defines the absolute minimum time that the current SDA value remains stable after SCL transitions from high-to-low. EXTHOLD should be set so that the minimum setup and hold times meet the SMBus Specification requirements of 250 ns and 300 ns, respectively. Table 30.2 shows the minimum setup and hold times meet the SMBus Specification requirements of 250 ns and 300 ns, respectively.





Figure 31.4. 4-Wire Single Master Mode and Slave Mode Connection Diagram

31.3. SPI0 Slave Mode Operation

When SPI0 is enabled and not configured as a master, it will operate as a SPI slave. As a slave, bytes are shifted in through the MOSI pin and out through the MISO pin by a master device controlling the SCK signal. A bit counter in the SPI0 logic counts SCK edges. When 8 bits have been shifted through the shift register, the SPIF flag is set to logic 1, and the byte is copied into the receive buffer. Data is read from the receive buffer by reading SPI0DAT. A slave device cannot initiate transfers. Data to be transferred to the master device is pre-loaded into the shift register by writing to SPI0DAT. Writes to SPI0DAT are double-buffered, and are placed in the transmit buffer first. If the shift register is empty, the contents of the transmit buffer will immediately be transferred into the shift register. When the shift register already contains data, the SPI will load the shift register with the transmit buffer's contents after the last SCK edge of the next (or current) SPI transfer.

When configured as a slave, SPI0 can be configured for 4-wire or 3-wire operation. The default, 4-wire slave mode, is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In 4-wire mode, the NSS signal is routed to a port pin and configured as a digital input. SPI0 is enabled when NSS is logic 0, and disabled when NSS is logic 1. The bit counter is reset on a falling edge of NSS. The NSS signal must be driven low at least 2 system clocks before the first active edge of SCK for each byte transfer. Figure 31.4 shows a connection diagram between two slave devices in 4-wire slave mode and a master device.

3-wire slave mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. NSS is not used in this mode, and is not mapped to an external port pin through the crossbar. Since there is no way of uniquely addressing the device in 3-wire slave mode, SPI0 must be the only slave device present on the bus. It is important to note that in 3-wire slave mode there is no external means of resetting the bit counter that determines when a full byte has been received. The bit counter can only be reset by disabling and re-enabling SPI0 with the SPIEN bit. Figure 31.3 shows a connection diagram between a slave device in 3-wire slave mode and a master device.



SFR Definition 31.1. SPI0CFG: SPI0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	SPIBSY	MSTEN	СКРНА	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT
Туре	R	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	0	1	1	1

SFR Address = 0xA1; SFR Page = 0

Bit	Name	Function
7	SPIBSY	SPI Busy.
		This bit is set to logic 1 when a SPI transfer is in progress (master or slave mode).
6	MSTEN	Master Mode Enable.
		0: Disable master mode. Operate in slave mode.
5	СКРНА	SPIU CIOCK Phase.
		1: Data centered on second edge of SCK period.
4	CKPOI	SPI0 Clock Polarity.
		0: SCK line low in idle state.
		1: SCK line high in idle state.
3	SLVSEL	Slave Selected Flag.
		This bit is set to logic 1 whenever the NSS pin is low indicating SPI0 is the selected
		slave. It is cleared to logic 0 when NSS is high (slave not selected). This bit does
		sion of the pin input.
2	NSSIN	NSS Instantaneous Pin Input.
_	neent	This bit mimics the instantaneous value that is present on the NSS port pin at the
		time that the register is read. This input is not de-glitched.
1	SRMT	Shift Register Empty (valid in slave mode only).
		This bit will be set to logic 1 when all data has been transferred in/out of the shift
		register, and there is no new information available to read from the transmit buffer
		the shift register from the transmit buffer or by a transition on SCK. SRMT = 1 when
		in Master Mode.
0	RXBMT	Receive Buffer Empty (valid in slave mode only).
		This bit will be set to logic 1 when the receive buffer has been read and contains no
		new information. If there is new information available in the receive buffer that has
Net		not been read, this bit will return to logic U. RABINT = 1 when in Master Mode.
Note:	in slave mode, of sampled one SV	Data on MOSI is sampled in the center of each data bit. In master mode, data on MISO is
	See Table 31.1	for timing parameters.



34.3.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.



Figure 34.5. PCA Software Timer Mode Diagram

