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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Cap Sense, POR, PWM, Temp Sensor, WDT
Number of I/O	39
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	32 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f712-gq

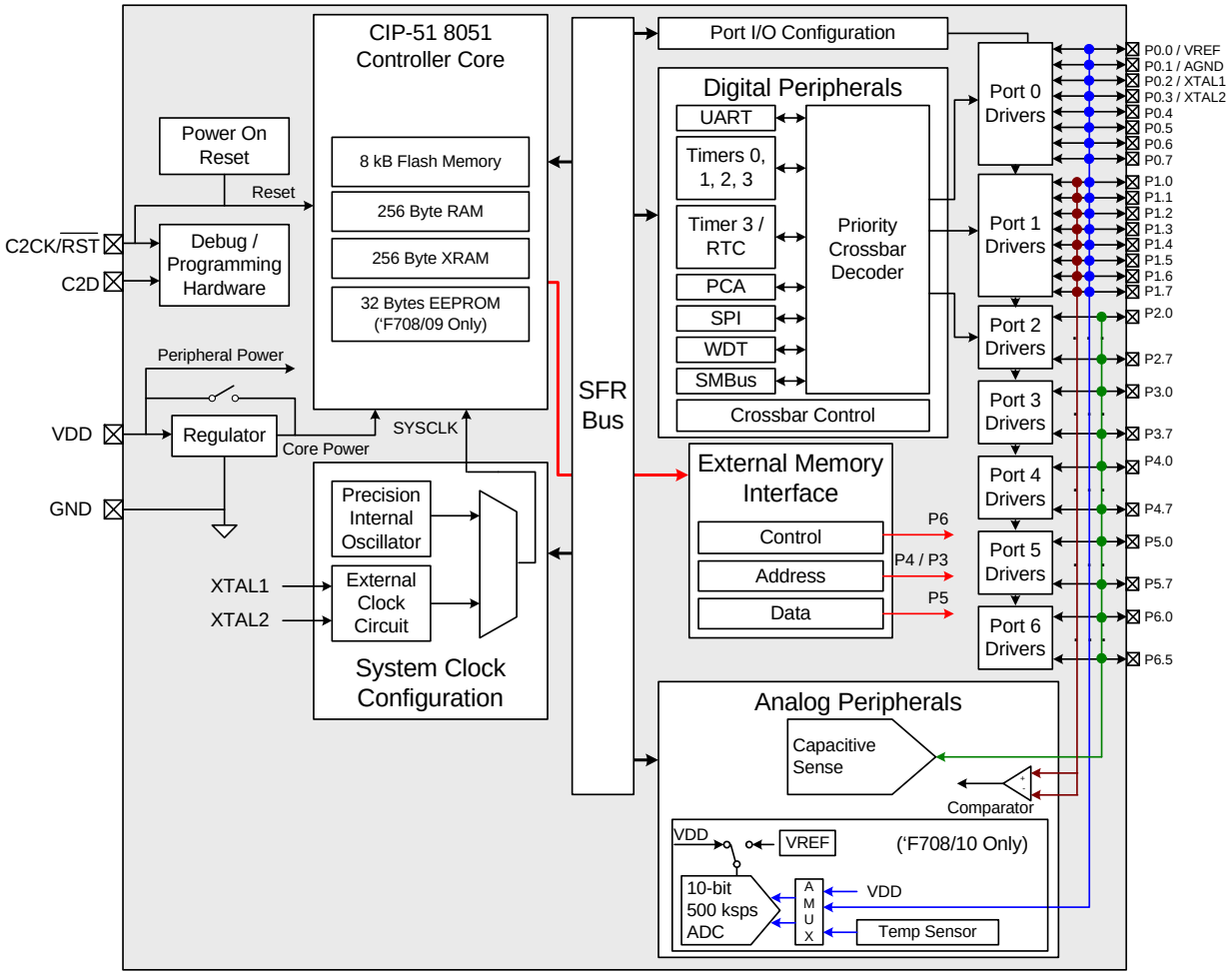

Figure 1.5. C8051F708/09/10/11 Block Diagram

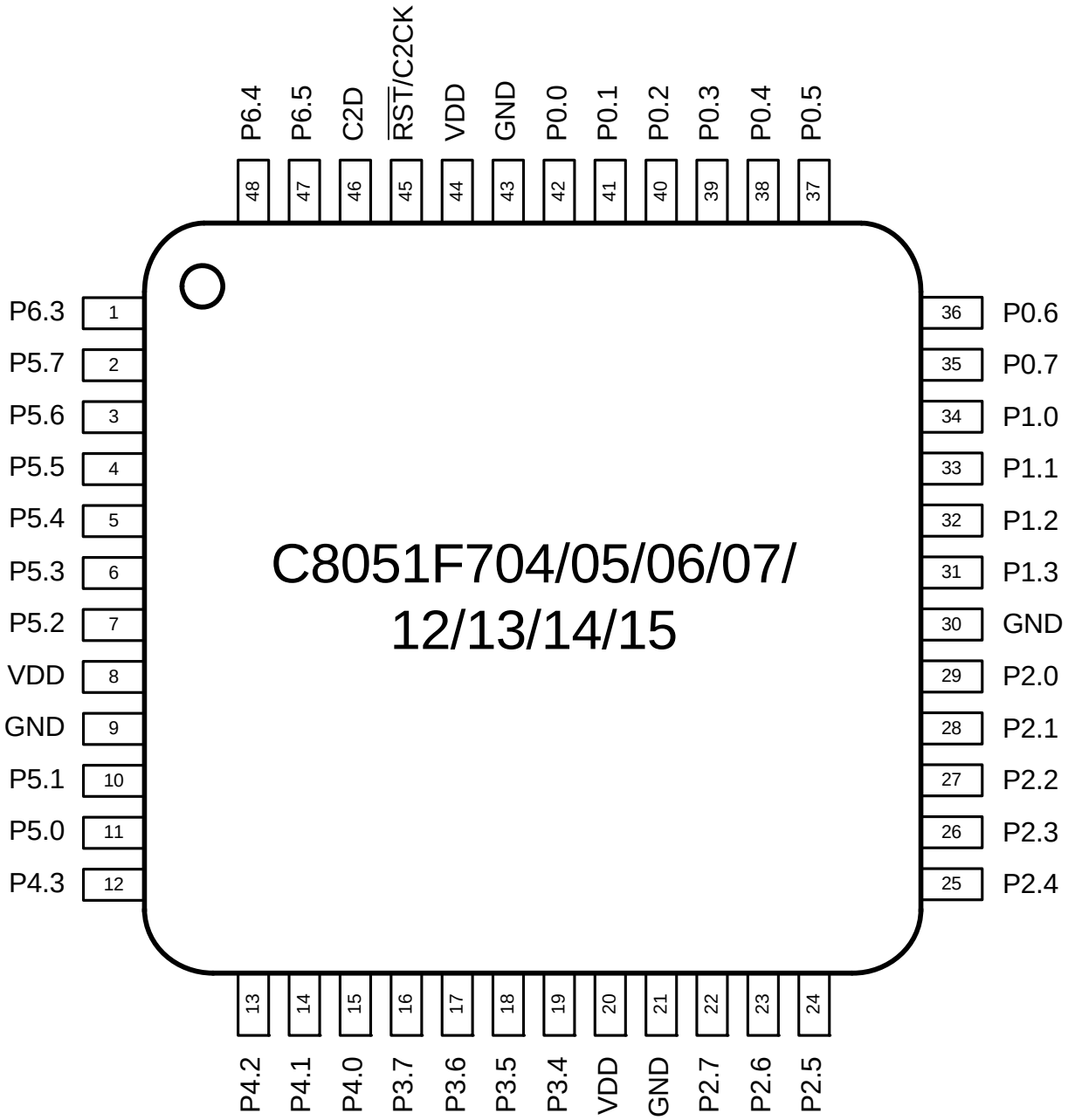

Figure 3.2. C8051F7xx-GQ QFP48 Pinout Diagram (Top View)

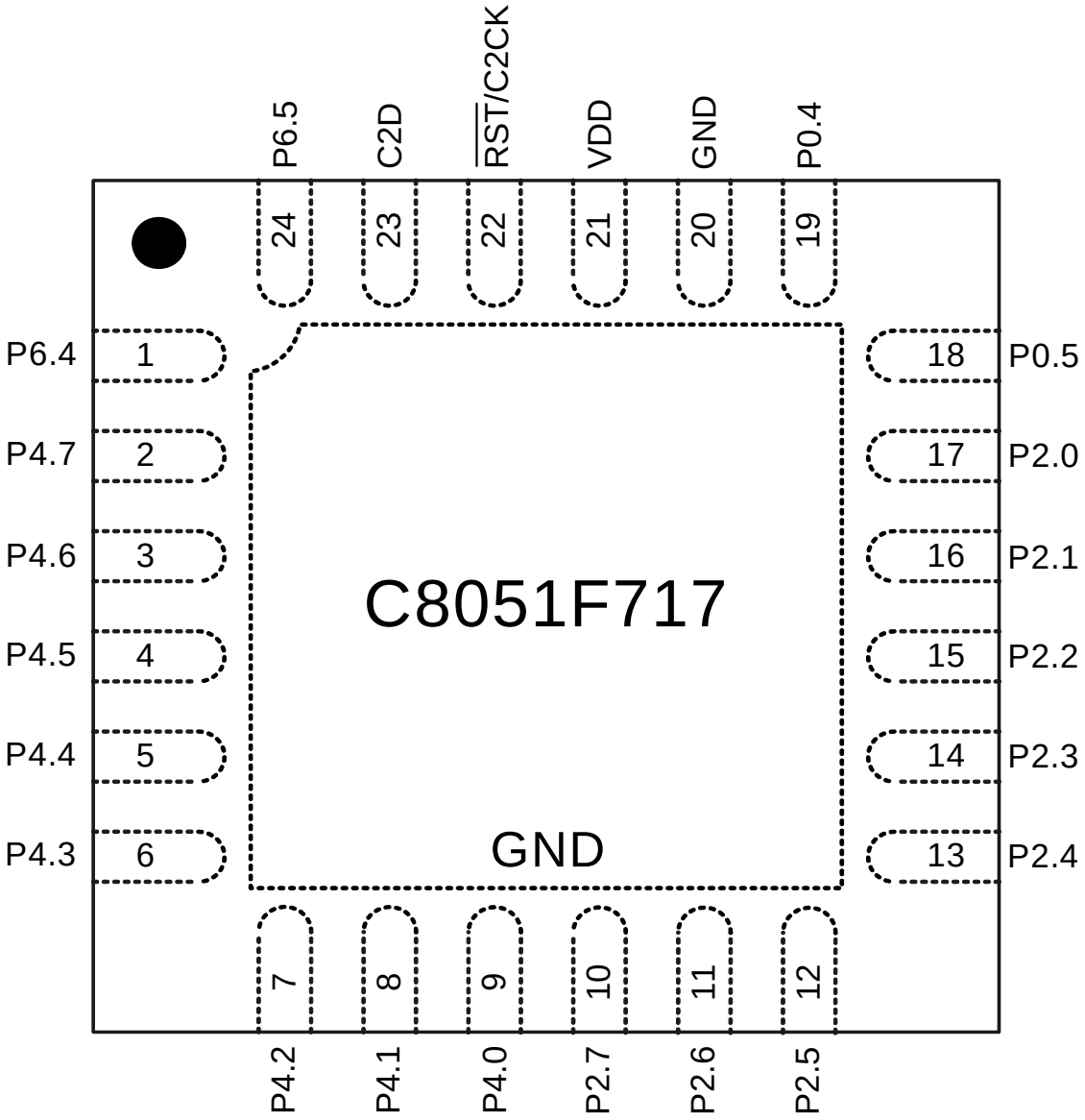

Figure 3.5. C8051F717-GM QFN24 Pinout Diagram (Top View)

Table 9.8. Capacitive Sense Electrical Characteristics

V_{DD} = 1.8 to 3.6 V; T_A = –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Single Conversion Time[1]	12-bit Mode	20	29	40	µs
	13-bit Mode (default)	21	31	42.5	
	14-bit Mode	23	33	45	
	16-bit Mode	26	38	50	
Number of Channels	64-pin Packages		38		Channels
	48-pin Packages		27		
	32-pin Packages		26		
	24-pin Packages		18		
Capacitance per Code	Default Configuration	—	1	—	fF
External Capacitive Load	CS0CG = 111b (Default)	—	—	45	pF
	CS0CG = 000b	—	—	500	pF
External Series Impedance	CS0CG = 111b (Default)	—	—	50	kΩ
Quantization Noise[1,2]	RMS	—	3	—	fF
	Peak-to-Peak	—	20	—	fF
Power Supply Current	CS module bias current, 25 °C	—	50	60	µA
	CS module alone, maximum code output, 25 °C	—	90	105	µA
	Wake-on-CS threshold (suspend mode with regulator and CS module on)[3]	—	130	145	µA

Notes:

1. Conversion time is specified with the default configuration.
2. RMS Noise is equivalent to one standard deviation. Peak-to-peak noise encompasses ±3.3 standard deviations. The RMS noise value is specified with the default configuration.
3. Includes only current from regulator, CS module, and MCU in suspend mode.

SFR Definition 10.1. ADC0CF: ADC0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD0SC[4:0]					AD0LJST	AD08BE	AMP0GN0
Type	R/W					R/W	R/W	R/W
Reset	1	1	1	1	1	0	0	1

SFR Address = 0xBC; SFR Page = F

Bit	Name	Function
7:3	AD0SC[4:0]	**ADC0 SAR Conversion Clock Period Bits.** SAR Conversion clock is derived from system clock by the following equation, where *AD0SC* refers to the 5-bit value held in bits AD0SC4–0. SAR Conversion clock requirements are given in the ADC specification table. $AD0SC = \frac{SYSCLK}{CLK_{SAR}} - 1$
2	AD0LJST	**ADC0 Left Justify Select.** 0: Data in ADC0H:ADC0L registers are right-justified. 1: Data in ADC0H:ADC0L registers are left-justified. **Note:** The AD0LJST bit is only valid for 10-bit mode (AD08BE = 0).
1	AD08BE	**8-Bit Mode Enable.** 0: ADC operates in 10-bit mode (normal). 1: ADC operates in 8-bit mode. **Note:** When AD08BE is set to 1, the AD0LJST bit is ignored.
0	AMP0GN0	**ADC Gain Control Bit.** 0: Gain = 0.5 1: Gain = 1

11. Temperature Sensor

An on-chip temperature sensor is included on the C8051F700/2/4/6/8 and C8051F710/2/4/6 which can be directly accessed via the ADC multiplexer in single-ended configuration. To use the ADC to measure the temperature sensor, the ADC mux channel should be configured to connect to the temperature sensor. The temperature sensor transfer function is shown in Figure 11.1. The output voltage (V_{TEMP}) is the positive ADC input when the ADC multiplexer is set correctly. The TEMPE bit in register REF0CN enables/disables the temperature sensor, as described in SFR Definition 12.1. While disabled, the temperature sensor defaults to a high impedance state and any ADC measurements performed on the sensor will result in meaningless data. Refer to Table 9.12 for the slope and offset parameters of the temperature sensor.

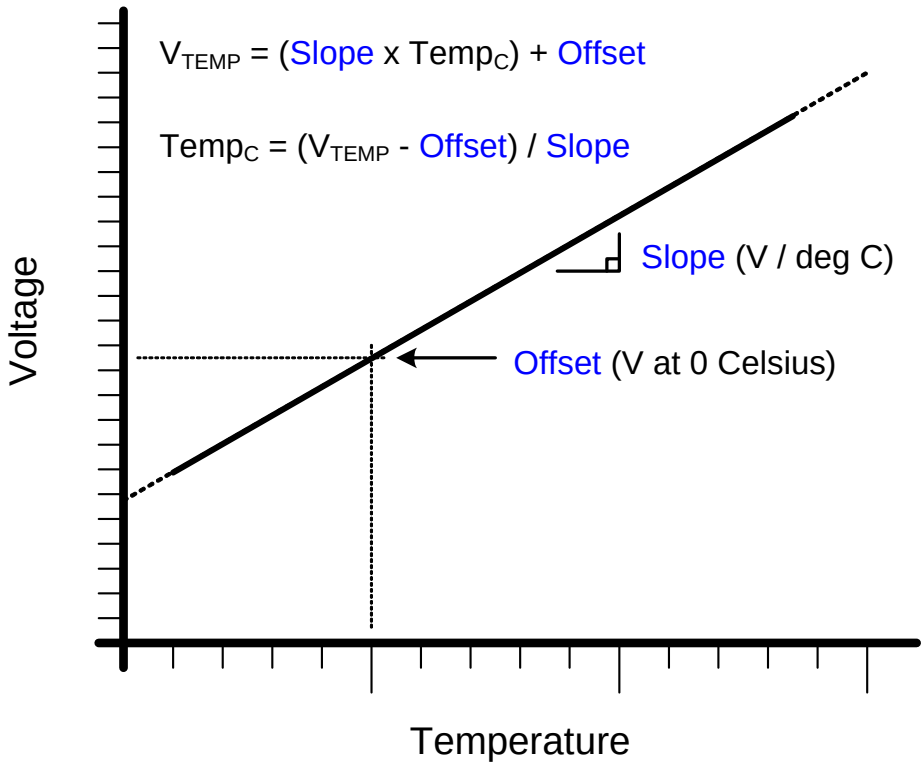

Figure 11.1. Temperature Sensor Transfer Function

11.1. Calibration

The uncalibrated temperature sensor output is extremely linear and suitable for relative temperature measurements (see Table 5.1 for linearity specifications). For absolute temperature measurements, offset and/or gain calibration is recommended. Typically a 1-point (offset) calibration includes the following steps:

1. Control/measure the ambient temperature (this temperature must be known).
2. Power the device, and delay for a few seconds to allow for self-heating.
3. Perform an ADC conversion with the temperature sensor selected as the ADC's input.
4. Calculate the offset characteristics, and store this value in non-volatile memory for use with subsequent temperature sensor measurements.

Figure 5.3 shows the typical temperature sensor error assuming a 1-point calibration at 0 °C.

15. Capacitive Sense (CS0)

The Capacitive Sense subsystem uses a capacitance-to-digital circuit to determine the capacitance on a port pin. The module can take measurements from different port pins using the module's analog multiplexer. The module is enabled only when the CS0EN bit (CS0CN) is set to 1. Otherwise the module is in a low-power shutdown state. The module can be configured to take measurements on one port pin or a group of port pins, using auto-scan. A selectable gain circuit allows the designer to adjust the maximum allowable capacitance. An accumulator is also included, which can be configured to average multiple conversions on an input channel. Interrupts can be generated when CS0 completes a conversion or when the measured value crosses a threshold defined in CS0THH:L.

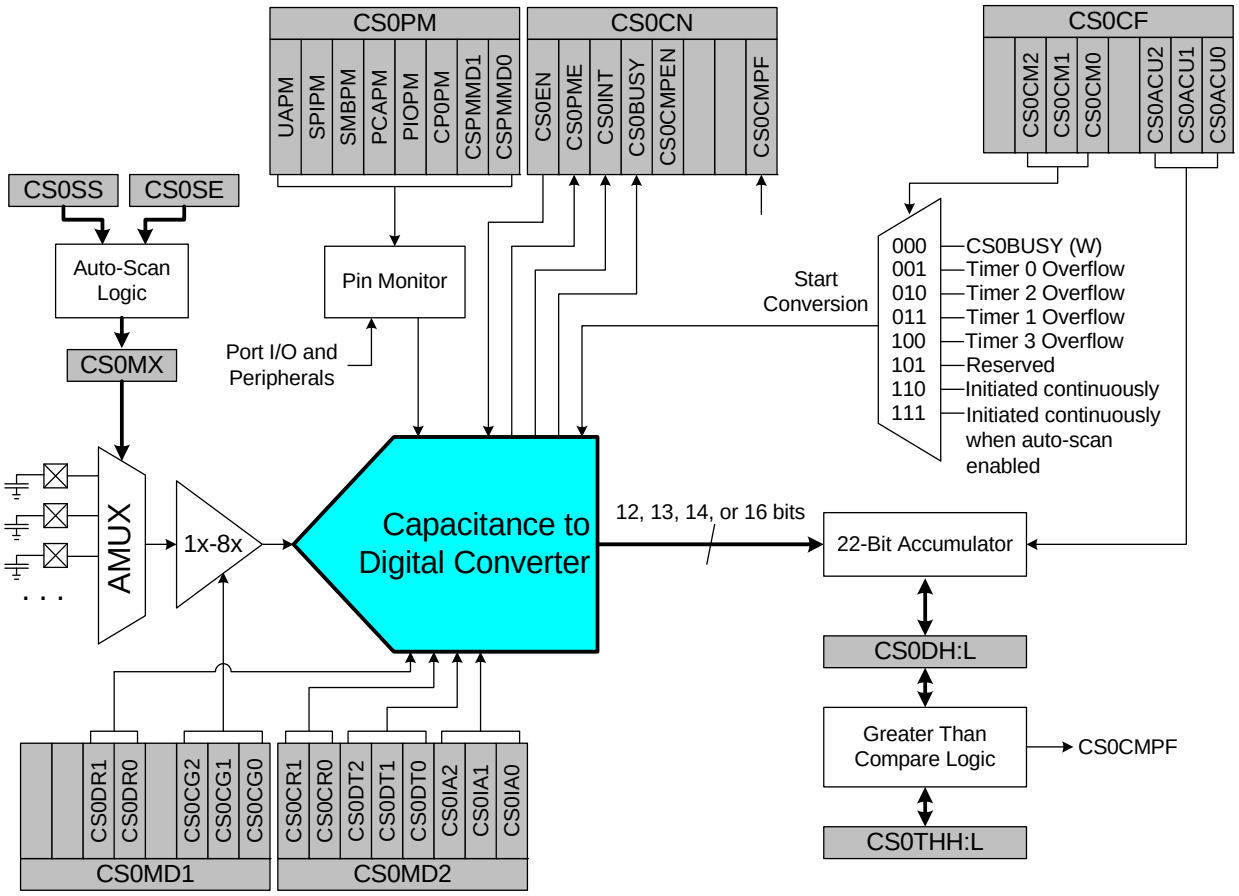

Figure 15.1. CS0 Block Diagram

If CS0BUSY is used to initiate conversions, and then polled to determine if the conversion is finished, at least one clock cycle must be inserted between setting CS0BUSY to 1 and polling the CS0BUSY bit.

Conversions can be configured to be initiated continuously through one of two methods. CS0 can be configured to convert at a single channel continuously or it can be configured to convert continuously with auto-scan enabled. When configured to convert continuously, conversions will begin after the CS0BUSY bit in CS0CF has been set. An interrupt will be generated if CS0 conversion complete interrupts are enabled by setting the ECSCPT bit (EIE2.0).

The CS0 module uses a method of successive approximation to determine the value of an external capacitance. The number of bits the CS0 module converts is adjustable using the CS0CR bits in register CS0MD2. Conversions are 13 bits long by default, but they can be adjusted to 12, 13, 14, or 16 bits depending on the needs of the application. Unconverted bits will be set to 0. Shorter conversion lengths produce faster conversion rates, and vice-versa. Applications can take advantage of faster conversion rates when the unconverted bits fall below the noise floor.

Note: CS0 conversion complete interrupt behavior depends on the settings of the CS0 accumulator. If CS0 is configured to accumulate multiple conversions on an input channel, a CS0 conversion complete interrupt will be generated only after the last conversion completes.

SFR Definition 15.12. CS0MX: Capacitive Sense Mux Channel Select

Bit	7	6	5	4	3	2	1	0
Name	CS0UC		CS0MX[5:0]					
Type	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9C; SFR Page = 0

Bit	Name	Description
7	CS0UC	**CS0 Unconnected.** Disconnects CS0 from all port pins, regardless of the selected channel. 0: CS0 connected to port pins 1: CS0 disconnected from port pins
6	Reserved	Write = 0b
5:0	CS0MX[5:0]	**CS0 Mux Channel Select.** Selects one of the 38 input channels for Capacitive Sense conversion.

Value	64-pin	48-pin	32-pin	24-pin	Value	64-pin	48-pin	32-pin	24-pin
000000	P2.0	P2.0	P2.0	P2.0	**010011**	P4.3	P4.3	—	P4.3
000001	P2.1	P2.1	P2.1	P2.1	**010100**	P4.4	—	—	P4.4
000010	P2.2	P2.2	P2.2	P2.2	**010101**	P4.5	—	—	P4.5
000011	P2.3	P2.3	P2.3	P2.3	**010110**	P4.6	—	—	P4.6
000100	P2.4	P2.4	P2.4	P2.4	**010111**	P4.7	—	—	P4.7
000101	P2.5	P2.5	P2.5	P2.5	**011000**	P5.0	P5.0	P5.0	—
000110	P2.6	P2.6	P2.6	P2.6	**011001**	P5.1	P5.1	P5.1	—
000111	P2.7	P2.7	P2.7	P2.7	**011010**	P5.2	P5.2	P5.2	—
001000	P3.0	—	P3.0	—	**011011**	P5.3	P5.3	P5.3	—
001001	P3.1	—	P3.1	—	**011100**	P5.4	P5.4	P5.4	—
001010	P3.2	—	P3.2	—	**011101**	P5.5	P5.5	P5.5	—
001011	P3.3	—	P3.3	—	**011110**	P5.6	P5.6	P5.6	—
001100	P3.4	P3.4	P3.4	—	**011111**	P5.7	P5.7	P5.7	—
001101	P3.5	P3.5	P3.5	—	**100000**	P6.0	—	—	—
001110	P3.6	P3.6	P3.6	—	**100001**	P6.1	—	—	—
001111	P3.7	P3.7	—	—	**100010**	P6.2	—	—	—
010000	P4.0	P4.0	—	P4.0	**100011**	P6.3	P6.3	P6.3	—
010001	P4.1	P4.1	—	P4.1	**100100**	P6.4	P6.4	P6.4	P6.4
010010	P4.2	P4.2	—	P4.2	**100101**	P6.5	P6.5	P6.5	P6.5

SFR Definition 19.3. REVID: Hardware Revision Identification Byte

Bit	7	6	5	4	3	2	1	0
Name	REVID[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SFR Address = 0xAD; SFR Page = F

Bit	Name	Description
7:0	**REVID[7:0]**	**Hardware Revision Identification Byte.** Shows the C8051F70x/71x hardware revision being used. For example, 0x00 = Revision A.

SFR Definition 23.2. EEDATA: EEPROM Byte Data

Bit	7	6	5	4	3	2	1	0
Name	EEDATA[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xD1; SFR Page = All Pages

Bit	Name	Description	Write	Read
7:0	EEDATA[7:0]	**E2PROM Data** The EEDATA register is used to read bytes from the EEPROM space and write bytes to EEPROM space.	Writes byte to location stored in EEADDR.	Returns contents at location stored in EEADDR.

28. Port Input/Output

Digital and analog resources are available through 64 I/O pins. Each of the Port pins P0.0–P2.7 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources, or assigned to an analog function as shown in Figure 28.4. The designer has complete control over which functions are assigned, limited only by the number of physical I/O pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. The state of a Port I/O pin can always be read in the corresponding Port latch, regardless of the Crossbar settings.

The Crossbar assigns the selected internal digital resources to the I/O pins based on the Priority Decoder. The registers XBR0 and XBR1, defined in SFR Definition 28.1 and SFR Definition 28.2, are used to select internal digital functions.

All Port I/Os except P0.3 are tolerant of voltages up to 2 V above the V_{DD} supply (refer to Figure 28.2 for the Port cell circuit). The Port I/O cells are configured as either push-pull or open-drain in the Port Output Mode registers (PnMDOUT, where n = 0,1). Complete Electrical Specifications for Port I/O are given in Section “9. Electrical Characteristics” on page 47.

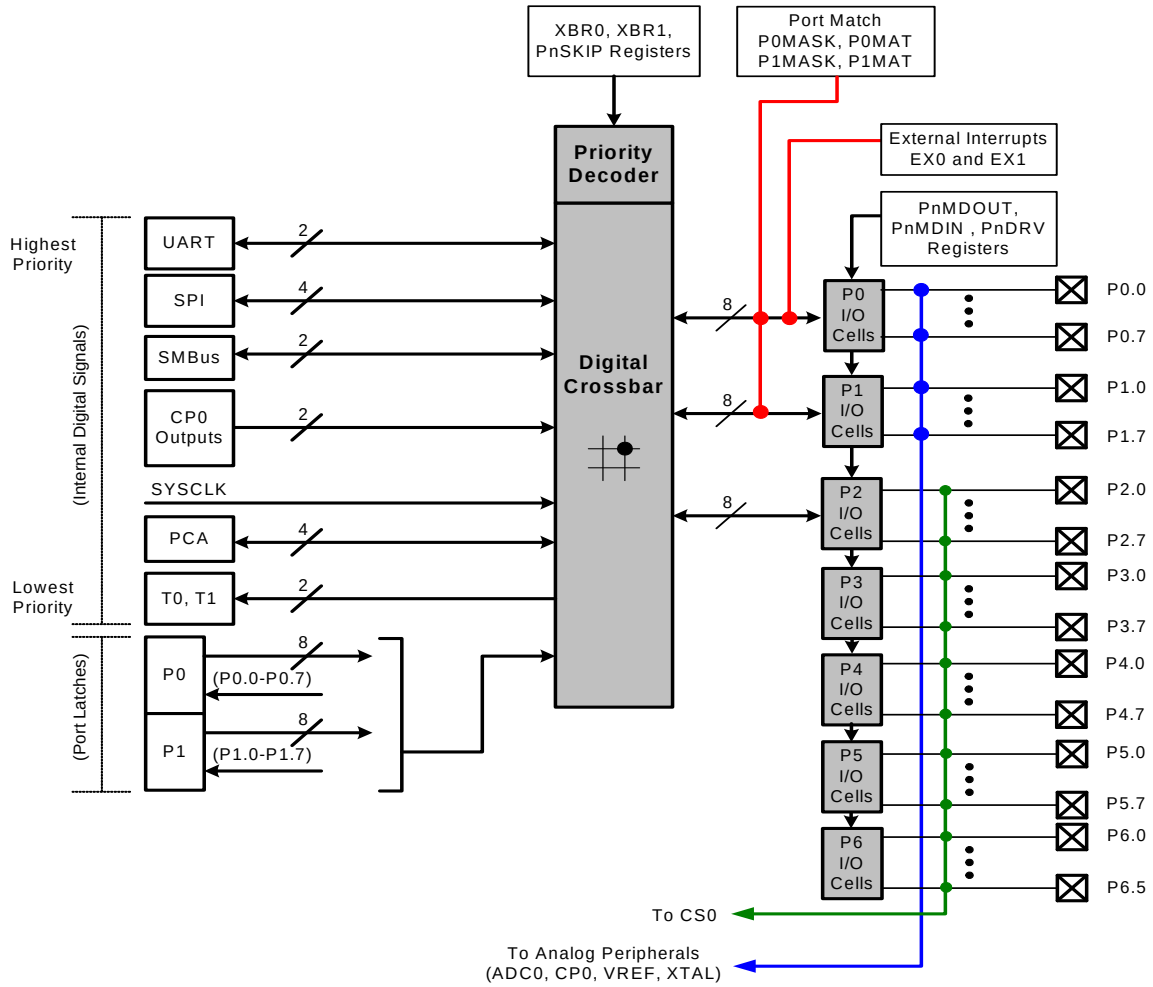

Figure 28.1. Port I/O Functional Block Diagram

SFR Definition 28.33. P5DRV: Port 5 Drive Strength

Bit	7	6	5	4	3	2	1	0
Name	P5DRV[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xFE; SFR Page = F

Bit	Name	Function
7:0	P5DRV[7:0]	**Drive Strength Configuration Bits for P5.7–P5.0 (respectively).** Configures digital I/O Port cells to high or low output drive strength. 0: Corresponding P5.n Output has low output drive strength. 1: Corresponding P5.n Output has high output drive strength.

SFR Definition 28.34. P6: Port 6

Bit	7	6	5	4	3	2	1	0
Name			P6[5:0]					
Type	R	R	R/W					
Reset	0	0	1	1	1	1	1	1

SFR Address = 0xB2; SFR Page = All Pages

Bit	Name	Description	Write	Read
7:6	Unused	Read = 00b; Write = Don't Care		
5:0	P6[5:0]	**Port 6 Data.** Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P6.n Port pin is logic LOW. 1: P6.n Port pin is logic HIGH.

29.1. 16-bit CRC Algorithm

The C8051F70x/71x CRC unit calculates the 16-bit CRC MSB-first, using a poly of 0x1021. The following describes the 16-bit CRC algorithm performed by the hardware:

1. XOR the most-significant byte of the current CRC result with the input byte. If this is the first iteration of the CRC unit, the current CRC result will be the set initial value (0x0000 or 0xFFFF).
2. If the MSB of the CRC result is set, left-shift the CRC result, and then XOR the CRC result with the polynomial (0x1021).
3. If the MSB of the CRC result is not set, left-shift the CRC result.
4. Repeat at Step 2 for the number of input bits (8).

For example, the 16-bit C8051F70x/71x CRC algorithm can be described by the following code:

```
unsigned short UpdateCRC (unsigned short CRC_acc, unsigned char CRC_input){
   unsigned char i;                    // loop counter
   #define POLY 0x1021
   // Create the CRC "dividend" for polynomial arithmetic (binary arithmetic
   // with no carries)
   CRC_acc = CRC_acc ^ (CRC_input << 8);
   // "Divide" the poly into the dividend using CRC XOR subtraction
   // CRC_acc holds the "remainder" of each divide
   // Only complete this division for 8 bits since input is 1 byte
   for (i = 0; i < 8; i++)
   {
      // Check if the MSB is set (if MSB is 1, then the POLY can "divide"
      // into the "dividend")
      if ((CRC_acc & 0x8000) == 0x8000)
      {
         // if so, shift the CRC value, and XOR "subtract" the poly
         CRC_acc = CRC_acc << 1;
         CRC_acc ^= POLY;
      }
      else
      {
         // if not, just shift the CRC value
         CRC_acc = CRC_acc << 1;
      }
   }
   return CRC_acc; // Return the final remainder (CRC value)
}
```

Table 29.1 lists example input values and the associated outputs using the 16-bit C8051F70x/71x CRC algorithm (an initial value of 0xFFFF is used):

Table 29.1. Example 16-bit CRC Outputs

Input	Output
0x63	0xBD35
0xAA, 0xBB, 0xCC	0x6CF6
0x00, 0x00, 0xAA, 0xBB, 0xCC	0xB166

29.6. CRC0 Bit Reverse Feature

CRC0 includes hardware to reverse the bit order of each bit in a byte as shown in Figure 29.1. Each byte of data written to CRC0FLIP is read back bit reversed. For example, if 0xC0 is written to CRC0FLIP, the data read back is 0x03. Bit reversal is a useful mathematical function used in algorithms such as the FFT.

SFR Definition 29.6. CRC0FLIP: CRC Bit Flip

Bit	7	6	5	4	3	2	1	0
Name	CRC0FLIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x95; SFR Page = F

Bit	Name	Function
7:0	CRC0FLIP[7:0]	**CRC0 Bit Flip.** Any byte written to CRC0FLIP is read back in a bit-reversed order, i.e. the written LSB becomes the MSB. For example: If 0xC0 is written to CRC0FLIP, the data read back will be 0x03. If 0x05 is written to CRC0FLIP, the data read back will be 0xA0.

Table 30.6. SMBus Status Decoding: Hardware ACK Enabled (EHACK = 1) (Continued)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Master Receiver	1000	0	0	1	A master data byte was received; ACK sent.	Set ACK for next data byte; Read SMB0DAT.	0	0	1	1000
						Set NACK to indicate next data byte as the last data byte; Read SMB0DAT.	0	0	0	1000
						Initiate repeated START.	1	0	0	1110
						Switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	X	1100
		0	0	0	A master data byte was received; NACK sent (last byte).	Read SMB0DAT; send STOP.	0	1	0	—
						Read SMB0DAT; Send STOP followed by START.	1	1	0	1110
						Initiate repeated START.	1	0	0	1110
						Switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	X	1100
Slave Transmitter	0100	0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	X	0001
		0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	X	0100
		0	1	X	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	X	0001
	0101	0	X	X	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	X	—

32.3. Multiprocessor Communications

9-Bit UART mode supports multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0.

Setting the MCE0 bit (SCON0.5) of a slave processor configures its UART such that when a stop bit is received, the UART will generate an interrupt only if the ninth bit is logic 1 (RB80 = 1) signifying an address byte has been received. In the UART interrupt handler, software will compare the received address with the slave's own assigned 8-bit address. If the addresses match, the slave will clear its MCE0 bit to enable interrupts on the reception of the following data byte(s). Slaves that weren't addressed leave their MCE0 bits set and do not generate interrupts on the reception of the following data bytes, thereby ignoring the data. Once the entire message is received, the addressed slave resets its MCE0 bit to ignore all transmissions until it receives the next address byte.

Multiple addresses can be assigned to a single slave and/or a single address can be assigned to multiple slaves, thereby enabling "broadcast" transmissions to more than one slave simultaneously. The master processor can be configured to receive all transmissions or a protocol can be implemented such that the master/slave role is temporarily reversed to enable half-duplex transmission between the original master and slave(s).

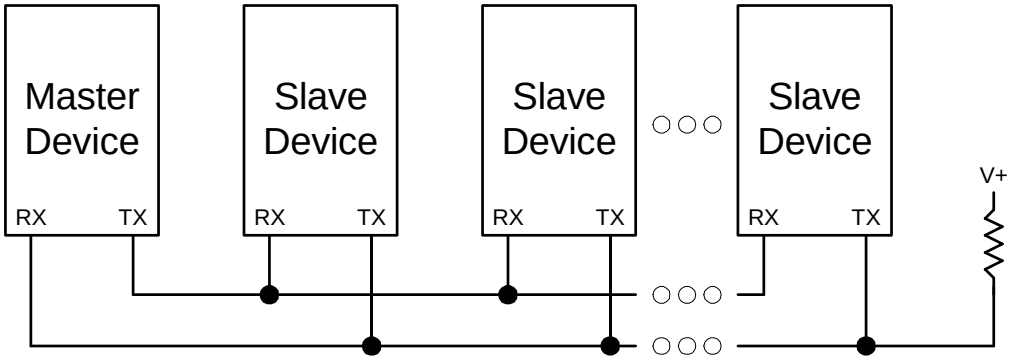

Figure 32.6. UART Multi-Processor Mode Interconnect Diagram

SFR Definition 33.11. TMR2L: Timer 2 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCC; SFR Page = 0

Bit	Name	Function
7:0	TMR2L[7:0]	**Timer 2 Low Byte.** In 16-bit mode, the TMR2L register contains the low byte of the 16-bit Timer 2. In 8-bit mode, TMR2L contains the 8-bit low byte timer value.

SFR Definition 33.12. TMR2H Timer 2 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCD; SFR Page = 0

Bit	Name	Function
7:0	TMR2H[7:0]	**Timer 2 Low Byte.** In 16-bit mode, the TMR2H register contains the high byte of the 16-bit Timer 2. In 8-bit mode, TMR2H contains the 8-bit high byte timer value.

SFR Definition 33.14. TMR3RLL: Timer 3 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x92; SFR Page = 0

Bit	Name	Function
7:0	TMR3RLL[7:0]	**Timer 3 Reload Register Low Byte.** TMR3RLL holds the low byte of the reload value for Timer 3.

SFR Definition 33.15. TMR3RLH: Timer 3 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x93; SFR Page = 0

Bit	Name	Function
7:0	TMR3RLH[7:0]	**Timer 3 Reload Register High Byte.** TMR3RLH holds the high byte of the reload value for Timer 3.

DOCUMENT CHANGE LIST

Revision 0.5 to Revision 1.0

- Updated “Electrical Characteristics” on page 47.
- Updated “Port Input/Output” on page 180.

Revision 0.4 to Revision 0.5

- Removed Incorrect Pin Connections in Figure 1.4 on page 21 and Figure 1.6 on page 23.
- Updated Specifications in Section “9. Electrical Characteristics” on page 47.
- Updated Section “15. Capacitive Sense (CS0)” on page 80 for clarity.
- Corrected “CJNE A, direct, rel” instruction timing in Table 16.1.
- Noted that a minimum SYSCLK speed is required for Flash writes or erases in Section “22.1. Programming The Flash Memory” on page 148, and for EEPROM writes in Section “23.3. Interfacing with the EEPROM” on page 155.
- Corrected P0.3 overvoltage capabilities throughout document.

Revision 0.3 to Revision 0.4

- Updated Section “15. Capacitive Sense (CS0)” on page 80 to reflect Revision B enhancements.
- Added C8051F716 and C8051F717 devices, package information, and features.
- Updated Register 19.1, “HWID: Hardware Identification Byte,” on page 128.
- Corrected minor typographical and formatting errors throughout document.

Revision 0.2 to Revision 0.3

- Corrected Dimension D in the QFN-48 Package Specifications.
- Updated Table 9.1 on page 47.
- Updated Register 10.1, “ADC0CF: ADC0 Configuration,” on page 59.
- Updated Register 14.3, “CPT0MX: Comparator0 MUX Selection,” on page 79.
- Updated Section “28.1.1. Port Pins Configured for Analog I/O” on page 181.
- Updated Register 35.2, “DEVICEID: C2 Device ID,” on page 302.