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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	Cap Sense, POR, PWM, WDT
Number of I/O	39
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	32 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f713-gq

List of Tables

Table 2.1. Product Selection Guide	27
Table 3.1. Pin Definitions for the C8051F70x/71x	28
Table 4.1. TQFP-64 Package Dimensions	37
Table 4.2. TQFP-64 PCB Land Pattern Dimensions	38
Table 5.1. TQFP-48 Package Dimensions	39
Table 5.2. TQFP-48 PCB Land Pattern Dimensions	40
Table 6.1. QFN-48 Package Dimensions	41
Table 6.2. QFN-48 PCB Land Pattern Dimensions	42
Table 7.1. QFN-32 Package Dimensions	43
Table 7.2. QFN-32 PCB Land Pattern Dimensions	44
Table 8.1. QFN-24 Package Dimensions	45
Table 8.2. QFN-24 PCB Land Pattern Dimensions	46
Table 9.1. Absolute Maximum Ratings	47
Table 9.2. Global Electrical Characteristics	48
Table 9.3. Port I/O DC Electrical Characteristics	49
Table 9.4. Reset Electrical Characteristics	49
Table 9.5. Internal Voltage Regulator Electrical Characteristics	50
Table 9.6. Flash Electrical Characteristics	50
Table 9.7. Internal High-Frequency Oscillator Electrical Characteristics	50
Table 9.8. Capacitive Sense Electrical Characteristics	51
Table 9.9. EEPROM Electrical Characteristics	52
Table 9.10. ADC0 Electrical Characteristics	52
Table 9.11. Power Management Electrical Characteristics	53
Table 9.12. Temperature Sensor Electrical Characteristics	53
Table 9.13. Voltage Reference Electrical Characteristics	53
Table 9.14. Comparator Electrical Characteristics	54
Table 15.1. Gain Setting vs. Maximum Capacitance and Conversion Time	81
Table 15.2. Operation with Auto-scan and Accumulate	85
Table 16.1. CIP-51 Instruction Set Summary	100
Table 18.1. AC Parameters for External Memory Interface	126
Table 18.2. EMIF Pinout (C8051F700/1/2/3/8/9 and C8051F710/1)	127
Table 20.1. Special Function Register (SFR) Memory Map	131
Table 20.2. Special Function Registers	132
Table 21.1. Interrupt Summary	139
Table 22.1. Flash Security Summary	150
Table 28.1. Port I/O Assignment for Analog Functions	183
Table 28.2. Port I/O Assignment for Digital Functions	184
Table 28.3. Port I/O Assignment for External Event Trigger Functions	184
Table 29.1. Example 16-bit CRC Outputs	212
Table 29.2. Example 32-bit CRC Outputs	213
Table 30.1. SMBus Clock Source Selection	223
Table 30.2. Minimum SDA Setup and Hold Times	224
Table 30.3. Sources for Hardware Changes to SMB0CN	228

List of Registers

SFR Definition 10.1. ADC0CF: ADC0 Configuration	59
SFR Definition 10.2. ADC0H: ADC0 Data Word MSB	60
SFR Definition 10.3. ADC0L: ADC0 Data Word LSB	60
SFR Definition 10.4. ADC0CN: ADC0 Control	61
SFR Definition 10.5. ADC0GTH: ADC0 Greater-Than Data High Byte	62
SFR Definition 10.6. ADC0GTL: ADC0 Greater-Than Data Low Byte	62
SFR Definition 10.7. ADC0LTH: ADC0 Less-Than Data High Byte	63
SFR Definition 10.8. ADC0LTL: ADC0 Less-Than Data Low Byte	63
SFR Definition 10.9. ADC0MX: AMUX0 Channel Select	66
SFR Definition 12.1. REF0CN: Voltage Reference Control	71
SFR Definition 13.1. REG0CN: Voltage Regulator Control	73
SFR Definition 14.1. CPT0CN: Comparator0 Control	76
SFR Definition 14.2. CPT0MD: Comparator0 Mode Selection	77
SFR Definition 14.3. CPT0MX: Comparator0 MUX Selection	79
SFR Definition 15.1. CS0CN: Capacitive Sense Control	88
SFR Definition 15.2. CS0CF: Capacitive Sense Configuration	89
SFR Definition 15.3. CS0DH: Capacitive Sense Data High Byte	90
SFR Definition 15.4. CS0DL: Capacitive Sense Data Low Byte	90
SFR Definition 15.5. CS0SS: Capacitive Sense Auto-Scan Start Channel	91
SFR Definition 15.6. CS0SE: Capacitive Sense Auto-Scan End Channel	91
SFR Definition 15.7. CS0THH: Capacitive Sense Comparator Threshold High Byte ...	92
SFR Definition 15.8. CS0THL: Capacitive Sense Comparator Threshold Low Byte	92
SFR Definition 15.9. CS0PM: Capacitive Sense Pin Monitor	93
SFR Definition 15.10. CS0MD1: Capacitive Sense Mode 1	94
SFR Definition 15.11. CS0MD2: Capacitive Sense Mode 2	95
SFR Definition 15.12. CS0MX: Capacitive Sense Mux Channel Select	97
SFR Definition 16.1. DPL: Data Pointer Low Byte	104
SFR Definition 16.2. DPH: Data Pointer High Byte	104
SFR Definition 16.3. SP: Stack Pointer	105
SFR Definition 16.4. ACC: Accumulator	105
SFR Definition 16.5. B: B Register	106
SFR Definition 16.6. PSW: Program Status Word	107
SFR Definition 18.1. EMI0CN: External Memory Interface Control	113
SFR Definition 18.2. EMI0CF: External Memory Configuration	114
SFR Definition 18.3. EMI0TC: External Memory Timing Control	119
SFR Definition 19.1. HWID: Hardware Identification Byte	128
SFR Definition 19.2. DERIVID: Derivative Identification Byte	128
SFR Definition 19.3. REVID: Hardware Revision Identification Byte	129
SFR Definition 20.1. SFRPAGE: SFR Page	132
SFR Definition 21.1. IE: Interrupt Enable	140
SFR Definition 21.2. IP: Interrupt Priority	141
SFR Definition 21.3. EIE1: Extended Interrupt Enable 1	142
SFR Definition 21.4. EIE2: Extended Interrupt Enable 2	143

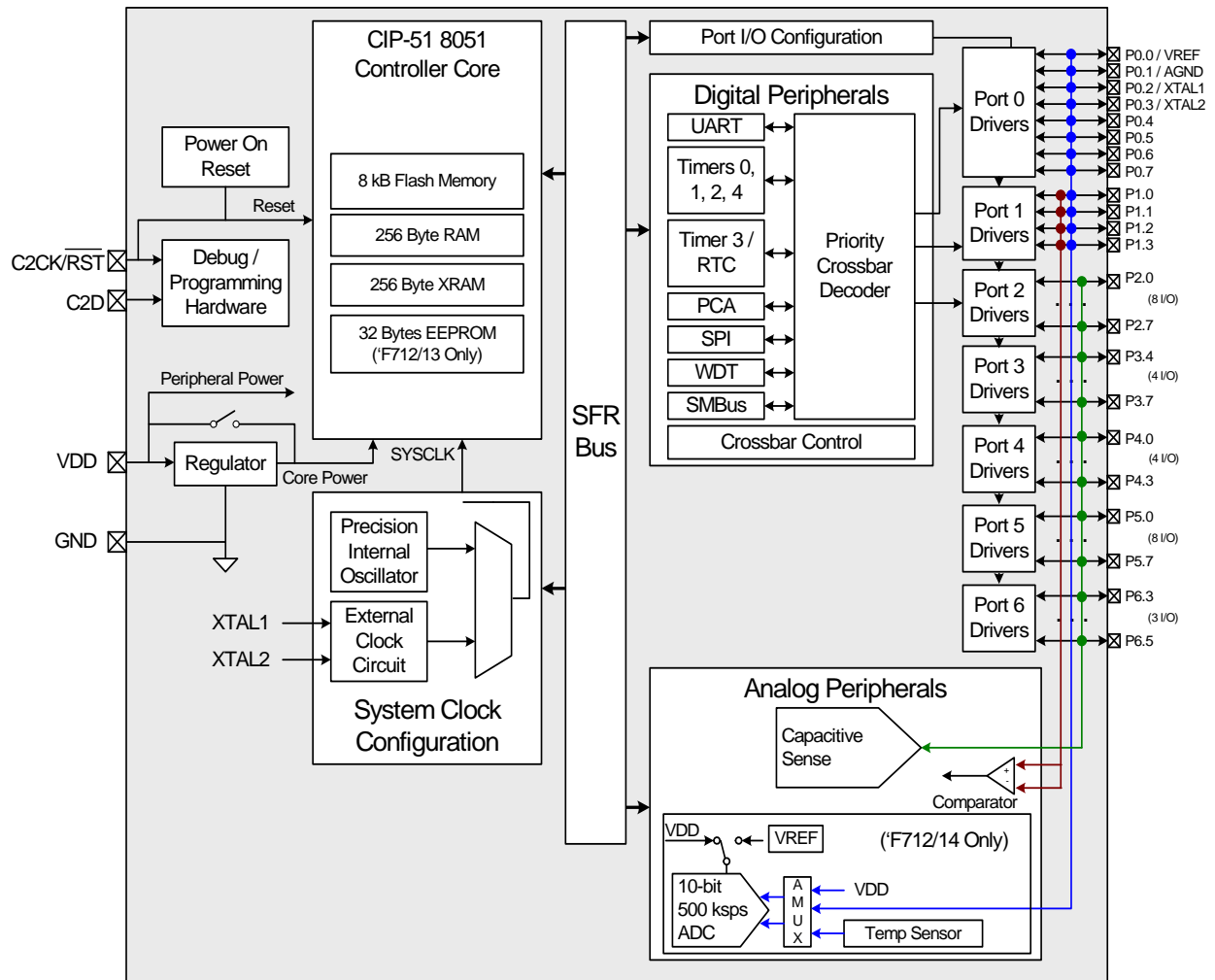


Figure 1.6. C8051F712/13/14/15 Block Diagram

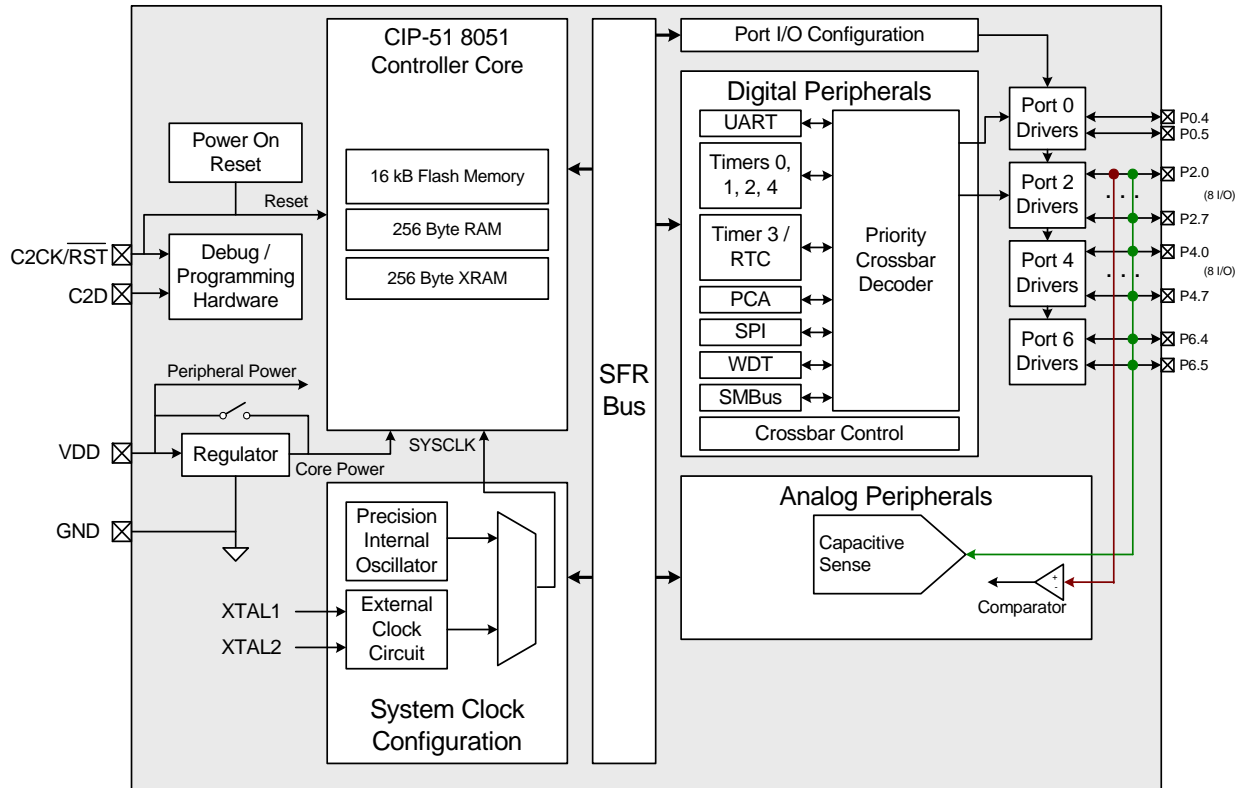


Figure 1.8. C8051F717 Block Diagram

C8051F70x/71x

SFR Definition 10.2. ADC0H: ADC0 Data Word MSB

Bit	7	6	5	4	3	2	1	0
Name	ADC0H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xBE; SFR Page = 0

Bit	Name	Function
7:0	ADC0H[7:0]	ADC0 Data Word High-Order Bits. For AD0LJST = 0: Bits 7:2 will read 000000b. Bits 1–0 are the upper 2 bits of the 10-bit ADC0 Data Word. For AD0LJST = 1: Bits 7:0 are the most-significant bits of the 10-bit ADC0 Data Word. Note: In 8-bit mode AD0LJST is ignored, and ADC0H holds the 8-bit data word.

SFR Definition 10.3. ADC0L: ADC0 Data Word LSB

Bit	7	6	5	4	3	2	1	0
Name	ADC0L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xBD; SFR Page = 0

Bit	Name	Function
7:0	ADC0L[7:0]	ADC0 Data Word Low-Order Bits. For AD0LJST = 0: Bits 7:0 are the lower 8 bits of the 10-bit Data Word. For AD0LJST = 1: Bits 7:6 are the lower 2 bits of the 10-bit Data Word. Bits 5–0 will always read 0. Note: In 8-bit mode AD0LJST is ignored, and ADC0L will read back 00000000b.

SFR Definition 12.1. REF0CN: Voltage Reference Control

Bit	7	6	5	4	3	2	1	0
Name			REFGND	REFSL		TEMPE	BIASE	
Type	R	R	R/W	R/W	R/W	R/W	R/W	R
Reset	0	0	0	1	0	0	0	0

SFR Address = 0xD2; SFR Page = F

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care.
5	REFGND	Analog Ground Reference. Selects the ADC0 ground reference. 0: The ADC0 ground reference is the GND pin. 1: The ADC0 ground reference is the P0.1/AGND pin.
4:3	REFSL	Voltage Reference Select. Selects the ADC0 voltage reference. 00: The ADC0 voltage reference is the P0.0/VREF pin. 01: The ADC0 voltage reference is the VDD pin. 10: The ADC0 voltage reference is the internal 1.8 V digital supply voltage. 11: The ADC0 voltage reference is the internal 1.6 V high-speed voltage reference.
2	TEMPE	Temperature Sensor Enable. Enables/Disables the internal temperature sensor. 0: Temperature Sensor Disabled. 1: Temperature Sensor Enabled.
1	BIASE	Internal Analog Bias Generator Enable Bit. 0: Internal Bias Generator off. 1: Internal Bias Generator on.
0	Unused	Read = 0b; Write = Don't Care.

SFR Definition 15.3. CS0DH: Capacitive Sense Data High Byte

Bit	7	6	5	4	3	2	1	0
Name	CS0DH[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xAA; SFR Page = 0

Bit	Name	Description
7:0	CS0DH	CS0 Data High Byte. Stores the high byte of the last completed 16-bit Capacitive Sense conversion.

SFR Definition 15.4. CS0DL: Capacitive Sense Data Low Byte

Bit	7	6	5	4	3	2	1	0
Name	CS0DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA9; SFR Page = 0

Bit	Name	Description
7:0	CS0DL	CS0 Data Low Byte. Stores the low byte of the last completed 16-bit Capacitive Sense conversion.

C8051F70x/71x

SFR Definition 19.3. REVID: Hardware Revision Identification Byte

Bit	7	6	5	4	3	2	1	0
Name	REVID[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SFR Address = 0xAD; SFR Page = F

Bit	Name	Description
7:0	REVID[7:0]	Hardware Revision Identification Byte. Shows the C8051F70x/71x hardware revision being used. For example, 0x00 = Revision A.

SFR Definition 21.2. IP: Interrupt Priority

Bit	7	6	5	4	3	2	1	0
Name		PSPI0	PT2	PS0	PT1	PX1	PT0	PX0
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

SFR Address = 0xB8; SFR Page = All Pages; Bit-Addressable

Bit	Name	Function
7	Unused	Read = 1b, Write = Don't Care.
6	PSPI0	Serial Peripheral Interface (SPI0) Interrupt Priority Control. This bit sets the priority of the SPI0 interrupt. 0: SPI0 interrupt set to low priority level. 1: SPI0 interrupt set to high priority level.
5	PT2	Timer 2 Interrupt Priority Control. This bit sets the priority of the Timer 2 interrupt. 0: Timer 2 interrupt set to low priority level. 1: Timer 2 interrupt set to high priority level.
4	PS0	UART0 Interrupt Priority Control. This bit sets the priority of the UART0 interrupt. 0: UART0 interrupt set to low priority level. 1: UART0 interrupt set to high priority level.
3	PT1	Timer 1 Interrupt Priority Control. This bit sets the priority of the Timer 1 interrupt. 0: Timer 1 interrupt set to low priority level. 1: Timer 1 interrupt set to high priority level.
2	PX1	External Interrupt 1 Priority Control. This bit sets the priority of the External Interrupt 1 interrupt. 0: External Interrupt 1 set to low priority level. 1: External Interrupt 1 set to high priority level.
1	PT0	Timer 0 Interrupt Priority Control. This bit sets the priority of the Timer 0 interrupt. 0: Timer 0 interrupt set to low priority level. 1: Timer 0 interrupt set to high priority level.
0	PX0	External Interrupt 0 Priority Control. This bit sets the priority of the External Interrupt 0 interrupt. 0: External Interrupt 0 set to low priority level. 1: External Interrupt 0 set to high priority level.

22.4.3. System Clock

12. If operating from an external crystal, be advised that crystal performance is susceptible to electrical interference and is sensitive to layout and to changes in temperature. If the system is operating in an electrically noisy environment, use the internal oscillator or use an external CMOS clock.
13. If operating from the external oscillator, switch to the internal oscillator during Flash write or erase operations. The external oscillator can continue to run, and the CPU can switch back to the external oscillator after the Flash operation has completed.

Additional Flash recommendations and example code can be found in “AN201: Writing to Flash from Firmware,” available from the Silicon Laboratories web site.

Port	P0								P1								P2							
Pin Number	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Special Function Signals	VREF	AGND	XTAL1	XTAL2			CNVSTR																	
TX0																								
RX0																								
SCK																								
MISO																								
MOSI																								
NSS*																								
SDA																								
SCL																								
CP0																								
CP0A																								
SYSCLK																								
CEX0																								
CEX1																								
CEX2																								
ECI																								
T0																								
T1																								
Pin Skip Settings	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	P0SKIP								P1SKIP								P2SKIP							

This example shows a crossbar configuration with XBR0 = 0x07 and XBR1 = 0x43.

■ These boxes represent Port pins which are assigned to a peripheral.

Figure 28.6. Crossbar Priority Decoder in Example Configuration—3 Pins Skipped

SFR Definition 29.4. CRC0AUTO: CRC Automatic Control

Bit	7	6	5	4	3	2	1	0
Name	AUTOEN	CRCCPT	Reserved	CRC0ST[4:0]				
Type	R/W							
Reset	0	1	0	0	0	0	0	0

SFR Address = 0x96; SFR Page = F

Bit	Name	Function
7	AUTOEN	Automatic CRC Calculation Enable. When AUTOEN is set to 1, any write to CRC0CN will initiate an automatic CRC starting at Flash sector CRC0ST and continuing for CRC0CNT sectors.
6	CRCCPT	Automatic CRC Calculation Complete. Set to 0 when a CRC calculation is in progress. Code execution is stopped during a CRC calculation, therefore reads from firmware will always return 1.
5	Reserved	Reserved. Must write 0.
4:0	CRC0ST[4:0]	Automatic CRC Calculation Starting Flash Sector. These bits specify the Flash sector to start the automatic CRC calculation. The starting address of the first Flash sector included in the automatic CRC calculation is CRC0ST x 512.

SFR Definition 29.5. CRC0CNT: CRC Automatic Flash Sector Count

Bit	7	6	5	4	3	2	1	0
Name			CRC0CNT[5:0]					
Type	R	R	R/W					
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x97; SFR Page = F

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care.
5:0	CRC0CNT[5:0]	Automatic CRC Calculation Flash Sector Count. These bits specify the number of Flash sectors to include when performing an automatic CRC calculation. The base address of the last flash sector included in the automatic CRC calculation is equal to (CRC0ST + CRC0CNT) x 512.

30.5.3. Write Sequence (Slave)

During a write sequence, an SMBus master writes data to a slave device. The slave in this transfer will be a receiver during the address byte, and a receiver during all data bytes. When slave events are enabled (INH = 0), the interface enters Slave Receiver Mode when a START followed by a slave address and direction bit (WRITE in this case) is received. If hardware ACK generation is disabled, upon entering Slave Receiver Mode, an interrupt is generated and the ACKRQ bit is set. The software must respond to the received slave address with an ACK, or ignore the received slave address with a NACK. If hardware ACK generation is enabled, the hardware will apply the ACK for a slave address which matches the criteria set up by SMB0ADR and SMB0ADM. The interrupt will occur after the ACK cycle.

If the received slave address is ignored (by software or hardware), slave interrupts will be inhibited until the next START is detected. If the received slave address is acknowledged, zero or more data bytes are received.

If hardware ACK generation is disabled, the ACKRQ is set to 1 and an interrupt is generated after each received byte. Software must write the ACK bit at that time to ACK or NACK the received byte.

With hardware ACK generation enabled, the SMBus hardware will automatically generate the ACK/NACK, and then post the interrupt. **It is important to note that the appropriate ACK or NACK value should be set up by the software prior to receiving the byte when hardware ACK generation is enabled.**

The interface exits Slave Receiver Mode after receiving a STOP. The interface will switch to Slave Transmitter Mode if SMB0DAT is written while an active Slave Receiver. Figure 30.7 shows a typical slave write sequence. Two received data bytes are shown, though any number of bytes may be received. Notice that the 'data byte transferred' interrupts occur at different places in the sequence, depending on whether hardware ACK generation is enabled. The interrupt occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled.

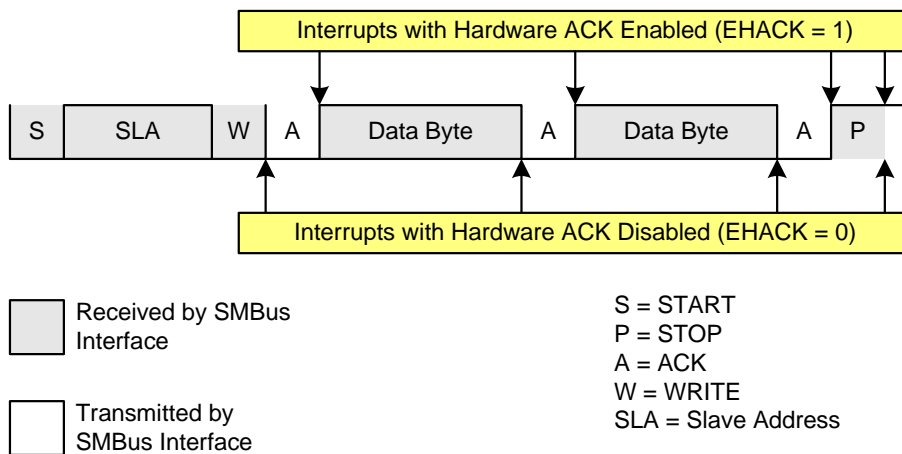


Figure 30.7. Typical Slave Write Sequence

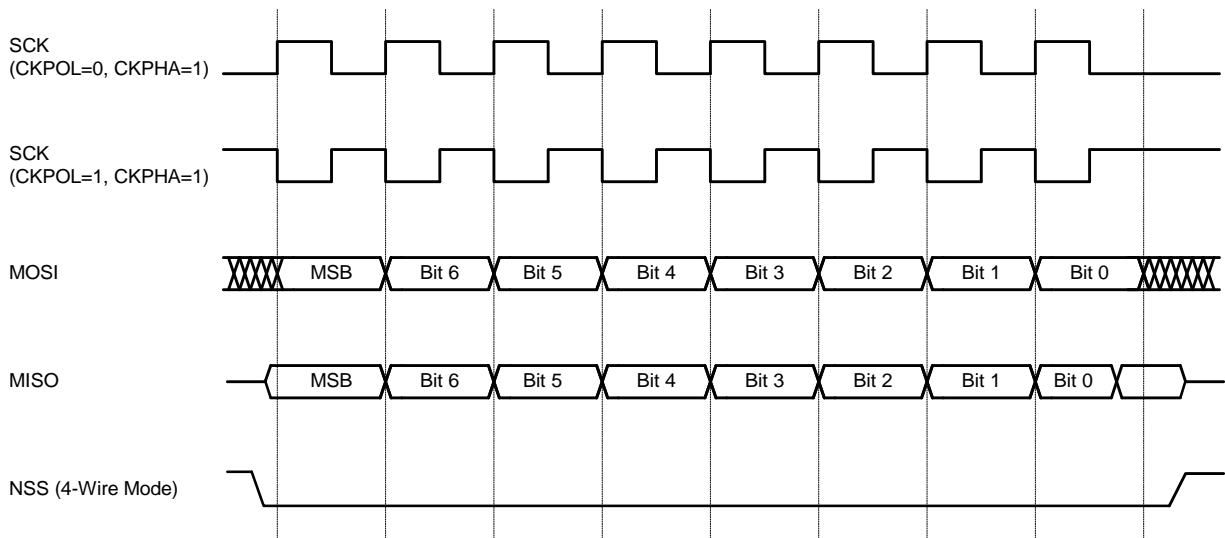
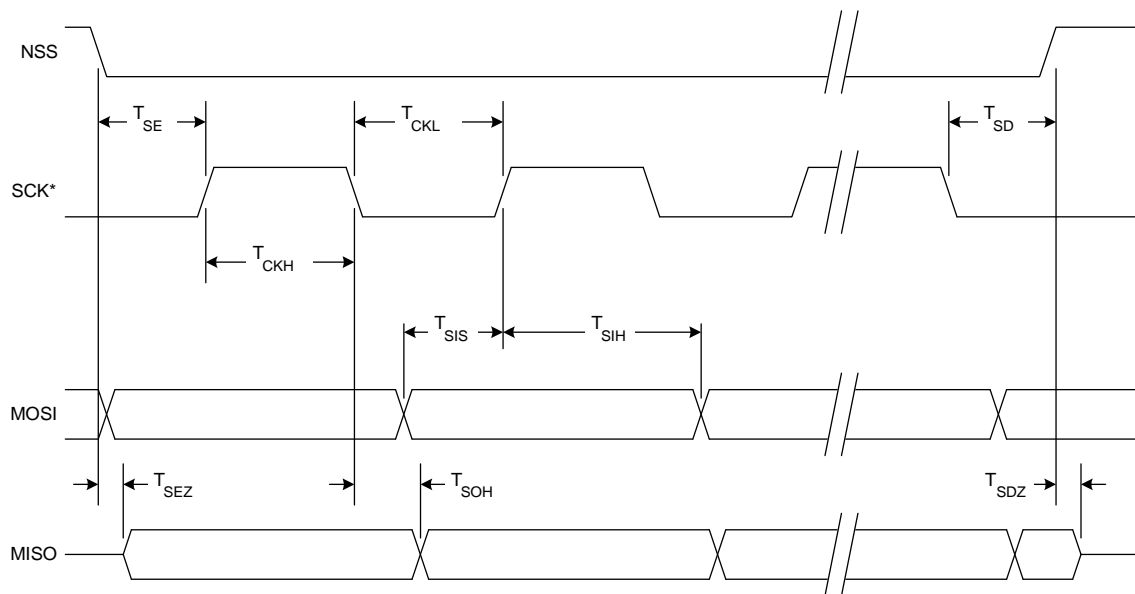


Figure 31.7. Slave Mode Data/Clock Timing (CKPHA = 1)

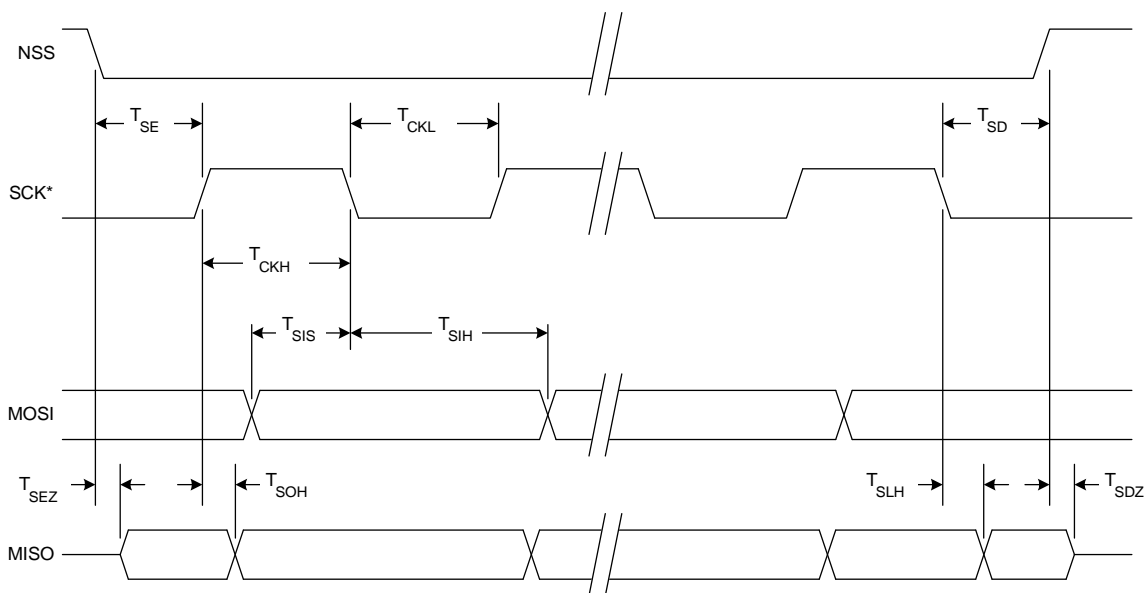
31.6. SPI Special Function Registers

SPI0 is accessed and controlled through four special function registers in the system controller: SPI0CN Control Register, SPI0DAT Data Register, SPI0CFG Configuration Register, and SPI0CKR Clock Rate Register. The four special function registers related to the operation of the SPI0 Bus are described in the following figures.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 31.10. SPI Slave Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 31.11. SPI Slave Timing (CKPHA = 1)

33. Timers

Each MCU includes four counter/timers: two are 16-bit counter/timers compatible with those found in the standard 8051, and two are 16-bit auto-reload timer for use with the ADC, SMBus, or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. Timer 2 and Timer 3 offer 16-bit and split 8-bit timer functionality with auto-reload. Additionally, Timer 3 offers the ability to be clocked from the external oscillator while the device is in Suspend mode, and can be used as a wake-up source. This allows for implementation of a very low-power system, including RTC capability.

Timer 0 and Timer 1 Modes:	Timer 2 Modes:	Timer 3 Modes:
13-bit counter/timer	16-bit timer with auto-reload	16-bit timer with auto-reload
16-bit counter/timer		
8-bit counter/timer with auto-reload	Two 8-bit timers with auto-reload	Two 8-bit timers with auto-reload
Two 8-bit counter/timers (Timer 0 only)		

Timers 0 and 1 may be clocked by one of five sources, determined by the Timer Mode Select bits (T1M–T0M) and the Clock Scale bits (SCA1–SCA0). The Clock Scale bits define a pre-scaled clock from which Timer 0 and/or Timer 1 may be clocked (See SFR Definition 33.1 for pre-scaled clock selection).

Timer 0/1 may then be configured to use this pre-scaled clock signal or the system clock. Timer 2 and Timer 3 may be clocked by the system clock, the system clock divided by 12, or the external oscillator clock source divided by 8.

Timer 0 and Timer 1 may also be operated as counters. When functioning as a counter, a counter/timer register is incremented on each high-to-low transition at the selected input pin (T0 or T1). Events with a frequency of up to one-fourth the system clock frequency can be counted. The input signal need not be periodic, but it should be held at a given level for at least two full system clock cycles to ensure the level is properly sampled.

33.1. Timer 0 and Timer 1

Each timer is implemented as a 16-bit register accessed as two separate bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The Counter/Timer Control register (TCON) is used to enable Timer 0 and Timer 1 as well as indicate status. Timer 0 interrupts can be enabled by setting the ET0 bit in the IE register (Section “21.2. Interrupt Register Descriptions” on page 140); Timer 1 interrupts can be enabled by setting the ET1 bit in the IE register (Section “21.2. Interrupt Register Descriptions” on page 140). Both counter/timers operate in one of four primary modes selected by setting the Mode Select bits T1M1–T0M0 in the Counter/Timer Mode register (TMOD). Each timer can be configured independently. Each operating mode is described below.

33.1.1. Mode 0: 13-bit Counter/Timer

Timer 0 and Timer 1 operate as 13-bit counter/timers in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically, and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSBs of the 13-bit counter/timer. TL0 holds the five LSBs in bit positions TL0.4–TL0.0. The three upper bits of TL0 (TL0.7–TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 in TCON is set and an interrupt will occur if Timer 0 interrupts are enabled.

The C/T0 bit in the TMOD register selects the counter/timer's clock source. When C/T0 is set to logic 1, high-to-low transitions at the selected Timer 0 input pin (T0) increment the timer register (Refer to Section “28.3. Priority Crossbar Decoder” on page 185 for information on selecting and configuring external I/O pins). Clearing C/T selects the clock defined by the T0M bit in register CKCON. When T0M is set, Timer 0 is clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 33.1).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 in the TMOD register is logic 0 or the input signal INT0 is active as defined by bit IN0PL in register IT01CF (see SFR Definition 21.7). Setting GATE0 to 1 allows the timer to be controlled by the external input signal INT0 (see Section “21.2. Interrupt Register Descriptions” on page 140), facilitating pulse width measurements

TR0	GATE0	INT0	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled

Note: X = Don't Care

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal INT1 is used with Timer 1; the INT1 polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 21.7).

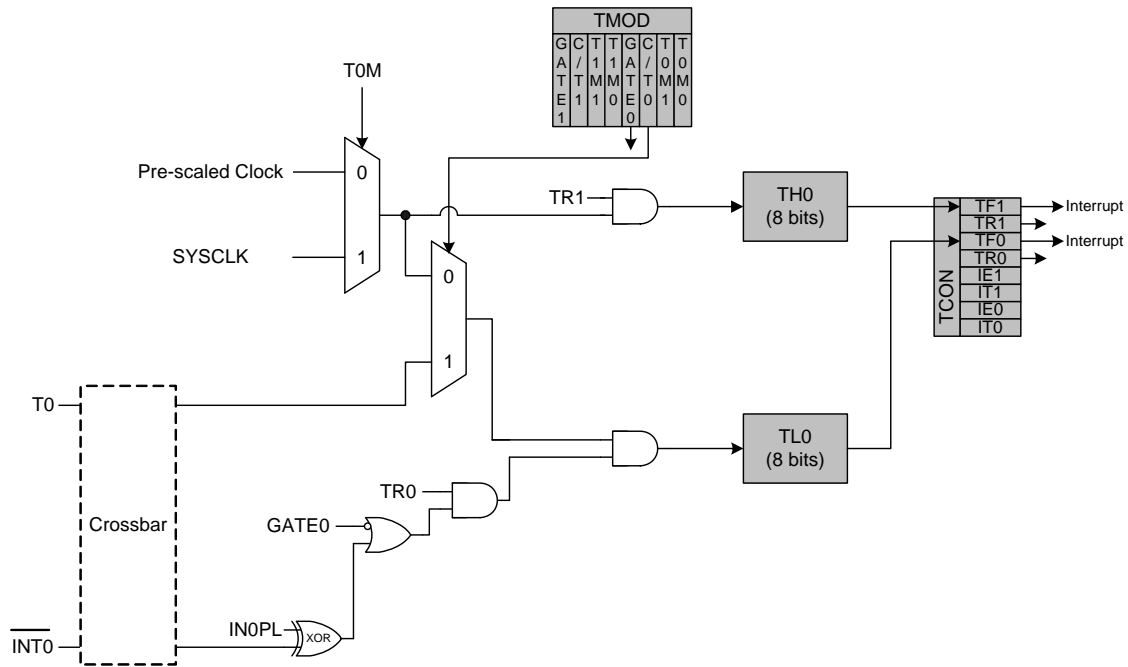


Figure 33.3. T0 Mode 3 Block Diagram

C8051F70x/71x

34.4. Register Descriptions for PCA0

Following are detailed descriptions of the special function registers related to the operation of the PCA.

SFR Definition 34.1. PCA0CN: PCA Control

Bit	7	6	5	4	3	2	1	0
Name	CF	CR				CCF2	CCF1	CCF0
Type	R/W	R/W	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD8; SFR Page = All Pages; Bit-Addressable

Bit	Name	Function
7	CF	PCA Counter/Timer Overflow Flag. Set by hardware when the PCA Counter/Timer overflows from 0xFFFF to 0x0000. When the Counter/Timer Overflow (CF) interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.
6	CR	PCA Counter/Timer Run Control. This bit enables/disables the PCA Counter/Timer. 0: PCA Counter/Timer disabled. 1: PCA Counter/Timer enabled.
5:3	Unused	Read = 000b; Write = Don't care
2:0	CCF[2:0]	PCA Module n Capture/Compare Flag. These bits are set by hardware when a match or capture occurs in the associated PCA Module n. When the CCFn interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

C8051F70x/71x

SFR Definition 34.5. PCA0L: PCA Counter/Timer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF9; SFR Page = 0

Bit	Name	Function
7:0	PCA0[7:0]	PCA Counter/Timer Low Byte. The PCA0L register holds the low byte (LSB) of the 16-bit PCA Counter/Timer.

SFR Definition 34.6. PCA0H: PCA Counter/Timer High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xFA; SFR Page = 0

Bit	Name	Function
7:0	PCA0[15:8]	PCA Counter/Timer High Byte. The PCA0H register holds the high byte (MSB) of the 16-bit PCA Counter/Timer. Reads of this register will read the contents of a “snapshot” register, whose contents are updated only when the contents of PCA0L are read (see Section 34.1).