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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	Cap Sense, POR, PWM, Temp Sensor, WDT
Number of I/O	39
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f714-gmr

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3. Pin Definitions

Table 3.1. Pin Definitions for the C8051F70x/71x

Name	TQFP64	TQFP48 QFN48	QFN32	QFN24	Type	Description
V _{DD}	8, 24, 41, 57	8, 20, 44	27	21		Power Supply Voltage.
GND	9, 25, 40, 56	9, 21, 30, 43	Center	20		Ground.
RST /	58	45	28	22	D I/O	Device Reset. Open-drain output of internal POR or V _{DD} monitor.
C2CK					D I/O	Clock signal for the C2 Debug Interface.
C2D	59	46	29	23	D I/O	Bi-directional data signal for the C2 Debug Interface.
P0.0 /	55	42	—	—	D I/O or A In	Port 0.0. ADC0 Input.
VREF					A In	External VREF input.
P0.1/	54	41	—	—	D I/O or A In	Port 0.1. ADC0 Input.
AGND						External AGND input.
P0.2 /	53	40	—	—	D I/O or A In	Port 0.2. ADC0 Input.
XTAL1					A In	External Clock Pin. This pin can be used for crystal clock mode.
P0.3 /	52	39	26	—	D I/O or A In	Port 0.3. ADC0 Input.
XTAL2					A I/O or D In	External Clock Pin. This pin can be used for RC, crystal, and CMOS clock modes.
P0.4	51	38	25	19	D I/O or A In	Port 0.4. ADC0 Input.
P0.5	50	37	24	18	D I/O or A In	Port 0.5. ADC0 Input.
P0.6	49	36	—	—	D I/O or A In	Port 0.6. ADC0 Input.

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Table 3.1. Pin Definitions for the C8051F70x/71x (Continued)

Name	TQFP64	TQFP48 QFN48	QFN32	QFN24	Type	Description
P0.7	48	35	—	—	D I/O or A In	Port 0.7. ADC0 Input.
P1.0	47	34	—	—	D I/O or A In	Port 1.0. ADC0 Input.
P1.1	46	33	—	—	D I/O or A In	Port 1.1. ADC0 Input.
P1.2	45	32	—	—	D I/O or A In	Port 1.2. ADC0 Input.
P1.3	44	31	—	—	D I/O or A In	Port 1.3. ADC0 Input.
P1.4	43	—	—	—	D I/O or A In	Port 1.4. ADC0 Input.
P1.5	42	—	—	—	D I/O or A In	Port 1.5. ADC0 Input.
P1.6	39	—	—	—	D I/O or A In	Port 1.6. ADC0 Input.
P1.7	38	—	—	—	D I/O or A In	Port 1.7. ADC0 Input.
P2.0	37	29	23	17	D I/O or A In	Port 2.0. CS0 input pin 1.
P2.1	36	28	22	16	D I/O or A In	Port 2.1. CS0 input pin 2.
P2.2	35	27	21	15	D I/O or A In	Port 2.2. CS0 input pin 3.
P2.3	34	26	20	14	D I/O or A In	Port 2.3. CS0 input pin 4.
P2.4	33	25	19	13	D I/O or A In	Port 2.4. CS0 input pin 5.
P2.5	32	24	18	12	D I/O or A In	Port 2.5. CS0 input pin 6.
P2.6	31	23	17	11	D I/O or A In	Port 2.6. CS0 input pin 7.
P2.7	30	22	16	10	D I/O or A In	Port 2.7. CS0 input pin 8.

Table 9.11. Power Management Electrical Characteristics

$V_{DD} = 1.8$ to 3.6 V; $T_A = -40$ to $+85$ °C unless otherwise specified. Use factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Idle Mode Wake-Up time		2	—	3	SYSCLKs
Suspend Mode Wake-Up Time		—	250	—	ns

Table 9.12. Temperature Sensor Electrical Characteristics

$V_{DD} = 3.0$ V, -40 to $+85$ °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Linearity		—	1	—	°C
Slope		—	3.27	—	mV/°C
Slope Error*		—	±65	—	µV/°C
Offset	Temp = 0 °C	—	868	—	mV
Offset Error*	Temp = 0 °C	—	±15.3	—	mV
*Note: Represents one standard deviation from the mean.					

Table 9.13. Voltage Reference Electrical Characteristics

$V_{DD} = 1.8$ to 3.6 V; -40 to $+85$ °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Internal High-Speed Reference (REFSL[1:0] = 11)					
Output Voltage	25 °C ambient	1.55	1.59	1.70	V
Turn-on Time		—	—	1.7	µs
Supply Current		—	200	—	µA
External Reference (REF0E = 0)					
Input Voltage Range		0	—	V_{DD}	
Input Current	Sample Rate = 500 ksp/s; $V_{REF} = 3.0$ V	—	7	—	µA

15.6. CS0 Conversion Accumulator

CS0 can be configured to accumulate multiple conversions on an input channel. The number of samples to be accumulated is configured using the CS0ACU2:0 bits (CS0CF2:0). The accumulator can accumulate 1, 4, 8, 16, 32, or 64 samples. After the defined number of samples have been accumulated, the result is divided by either 1, 4, 8, 16, 32, or 64 (depending on the CS0ACU[2:0] setting) and copied to the CS0DH:CS0DL SFRs.

Table 15.2. Operation with Auto-scan and Accumulate

Auto-Scan Enabled	Accumulator Enabled	CS0 Conversion Complete Interrupt Behavior	CS0 Greater Than Interrupt Behavior	CS0MX Behavior
N	N	CS0INT Interrupt serviced after 1 conversion completes	Interrupt serviced after 1 conversion completes if value in CS0DH:CS0DL is greater than CS0THH:CS0THL	CS0MX unchanged.
N	Y	CS0INT Interrupt serviced after <i>M</i> conversions complete	Interrupt serviced after <i>M</i> conversions complete if value in CS0DH:CS0DL (post accumulate and divide) is greater than CS0THH:CS0THL	CS0MX unchanged.
Y	N	CS0INT Interrupt serviced after 1 conversion completes	Interrupt serviced after conversion completes if value in CS0DH:CS0DL is greater than CS0THH:CS0THL; Auto-Scan stopped	If greater-than comparator detects conversion value is greater than CS0THH:CS0THL, CS0MX is left unchanged; otherwise, CS0MX updates to the next channel (CS0MX + 1) and wraps back to CS0SS after passing CS0SE
Y	Y	CS0INT Interrupt serviced after <i>M</i> conversions complete	Interrupt serviced after <i>M</i> conversions complete if value in CS0DH:CS0DL (post accumulate and divide) is greater than CS0THH:CS0THL; Auto-Scan stopped	If greater-than comparator detects conversion value is greater than CS0THH:CS0THL, CS0MX is left unchanged; otherwise, CS0MX updates to the next channel (CS0MX + 1) and wraps back to CS0SS after passing CS0SE
M = Accumulator setting (1x, 4x, 8x, 16x, 32x, 64x)				

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Table 18.2. EMIF Pinout (C8051F700/1/2/3/8/9 and C8051F710/1)

Multiplexed Mode		Non Multiplexed Mode	
Signal Name	Port Pin	Signal Name	Port Pin
$\overline{\text{RD}}$	P6.1	$\overline{\text{RD}}$	P6.1
$\overline{\text{WR}}$	P6.0	$\overline{\text{WR}}$	P6.0
ALE	P6.2	D0	P5.0
D0/A0	P5.0	D1	P5.1
D1/A1	P5.1	D2	P5.2
D2/A2	P5.2	D3	P5.3
D3/A3	P5.3	D4	P5.4
D4/A4	P5.4	D5	P5.5
D5/A5	P5.5	D6	P5.6
D6/A6	P5.6	D7	P5.7
D7/A7	P5.7	A0	P4.0
A8	P4.0	A1	P4.1
A9	P4.1	A2	P4.2
A10	P4.2	A3	P4.3
A11	P4.3	A4	P4.4
A12	P4.4	A5	P4.5
A13	P4.5	A6	P4.6
A14	P4.6	A7	P4.7
A15	P4.7	A8	P3.0
—	—	A9	P3.1
—	—	A10	P3.2
—	—	A11	P3.3
—	—	A12	P3.4
—	—	A13	P3.5
—	—	A14	P3.6
—	—	A15	P3.7

Table 20.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Page	Description	Page
CS0CN	0x9A	0	CS0 Control	88
CS0DH	0xAA	0	CS0 Data High	90
CS0DL	0xA9	0	CS0 Data Low	90
CS0CF	0x9E	0	CS0 Configuration	89
CS0MD1	0xAD	0	CS0 Mode 1	94
CS0MD2	0xBE	F	CS0 Mode 2	95
CS0MX	0x9C	0	CS0 Mux	97
CS0PM	0x9F	F	CS0 Pin Monitor	93
CS0SE	0x93	F	Auto Scan End Channel	91
CS0SS	0x92	F	Auto Scan Start Channel	91
CS0THH	0x97	0	CS0 Digital Compare Threshold High	92
CS0THL	0x96	0	CS0 Digital Compare Threshold Low	92
DERIVID	0xEC	F	Derivative Identification	128
DPH	0x83	All Pages	Data Pointer High	104
DPL	0x82	All Pages	Data Pointer Low	104
EEADDR	0xB6	All Pages	EEPROM Byte Address	156
EECNTL	0xC5	F	EEPROM Control	158
EEDATA	0xD1	All Pages	EEPROM Byte Data	157
EEKEY	0xC6	F	EEPROM Protect Key	159
EIE1	0xE6	All Pages	Extended Interrupt Enable 1	142
EIE2	0xE7	All Pages	Extended Interrupt Enable 2	143
EIP1	0xCE	F	Extended Interrupt Priority 1	144
EIP2	0xCF	F	Extended Interrupt Priority 2	145
EMI0CF	0xC7	F	EMIF Configuration	114
EMI0CN	0xAA	F	EMIF Control	113
EMI0TC	0xEE	F	EMIF Timing Control	119
FLKEY	0xB7	All Pages	Flash Lock And Key	154
HWID	0xC4	F	Hardware Identification	128
IE	0xA8	All Pages	Interrupt Enable	140
IP	0xB8	All Pages	Interrupt Priority	141
IT01CF	0xE4	F	INT0/INT1 Configuration	147
OSCICL	0xBF	F	Internal Oscillator Calibration	173
OSICN	0xA9	F	Internal Oscillator Control	174
OSXCXN	0xB5	F	External Oscillator Control	176
P0	0x80	All Pages	Port 0 Latch	195
P0DRV	0xF9	F	Port 0 Drive Strength	197
P0MASK	0xF4	0	Port 0 Mask	192
P0MAT	0xF3	0	Port 0 Match	193

21.1. MCU Interrupt Sources and Vectors

The C8051F70x/71x MCUs support 16 interrupt sources. Software can simulate an interrupt by setting an interrupt-pending flag to logic 1. If interrupts are enabled for the flag, an interrupt request will be generated and the CPU will vector to the ISR address associated with the interrupt-pending flag. MCU interrupt sources, associated vector addresses, priority order and control bits are summarized in Table 21.1. Refer to the datasheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

21.1.1. Interrupt Priorities

Each interrupt source can be individually programmed to one of two priority levels: low or high. A low priority interrupt service routine can be preempted by a high priority interrupt. A high priority interrupt cannot be preempted. Each interrupt has an associated interrupt priority bit in an SFR (IP or EIP1) used to configure its priority level. Low priority is the default. If two interrupts are recognized simultaneously, the interrupt with the higher priority is serviced first. If both interrupts have the same priority level, a fixed priority order is used to arbitrate, given in Table 21.1.

21.1.2. Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 5 system clock cycles: 1 clock cycle to detect the interrupt and 4 clock cycles to complete the LCALL to the ISR. If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. Therefore, the maximum response time for an interrupt (when no other interrupt is currently being serviced or the new interrupt is of greater priority) occurs when the CPU is performing an RETI instruction followed by a DIV as the next instruction. In this case, the response time is 18 system clock cycles: 1 clock cycle to detect the interrupt, 5 clock cycles to execute the RETI, 8 clock cycles to complete the DIV instruction and 4 clock cycles to execute the LCALL to the ISR. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction.

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6. Using the MOVX instruction, write a data byte to any location within the 512-byte page to be erased.
7. Clear the PSWE and PSEE bits.
8. Restore previous interrupt state.

Steps 4–6 must be repeated for each 512-byte page to be erased.

Note: Flash security settings may prevent erasure of some Flash pages, such as the reserved area and the page containing the lock bytes. For a summary of Flash security settings and restrictions affecting Flash erase operations, please see Section “22.3. Security Options” on page 149.

22.1.3. Flash Write Procedure

A write to Flash memory can clear bits to logic 0 but cannot set them; only an erase operation can set bits to logic 1 in Flash. **A byte location to be programmed should be erased before a new value is written.**

The recommended procedure for writing a single byte in Flash is as follows:

1. Save current interrupt state and disable interrupts.
2. Ensure that the Flash byte has been erased (has a value of 0xFF).
3. Set the PSWE bit (register PSCTL).
4. Clear the PSEE bit (register PSCTL).
5. Write the first key code to FLKEY: 0xA5.
6. Write the second key code to FLKEY: 0xF1.
7. Using the MOVX instruction, write a single data byte to the desired location within the 512-byte sector.
8. Clear the PSWE bit.
9. Restore previous interrupt state.

Steps 5–7 must be repeated for each byte to be written.

Note: Flash security settings may prevent writes to some areas of Flash, such as the reserved area. For a summary of Flash security settings and restrictions affecting Flash write operations, please see Section “22.3. Security Options” on page 149.

22.2. Non-volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX write instruction and read using the MOVC instruction.

Note: MOVX read instructions always target XRAM.

22.3. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the Flash memory from accidental modification by software. PSWE must be explicitly set to 1 before software can modify the Flash memory; both PSWE and PSEE must be set to 1 before software can erase Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A Security Lock Byte located at the last byte of Flash user space offers protection of the Flash program memory from access (reads, writes, and erases) by unprotected code or the C2 interface. The Flash security mechanism allows the user to lock all Flash pages, starting at page 0, by writing a non-0xFF value to the lock byte. **Note that writing a non-0xFF value to the lock byte will lock all pages of FLASH from reads, writes, and erases, including the page containing the lock byte.**

The level of Flash security depends on the Flash access method. The three Flash access methods that can be restricted are reads, writes, and erases from the C2 debug interface, user firmware executing on

SFR Definition 22.2. FLKEY: Flash Lock and Key

Bit	7	6	5	4	3	2	1	0
Name	FLKEY[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB7; SFR Page = All Pages

Bit	Name	Function
7:0	FLKEY[7:0]	<p>Flash Lock and Key Register.</p> <p>Write: This register provides a lock and key function for Flash erasures and writes. Flash writes and erases are enabled by writing 0xA5 followed by 0xF1 to the FLKEY register. Flash writes and erases are automatically disabled after the next write or erase is complete. If any writes to FLKEY are performed incorrectly, or if a Flash write or erase operation is attempted while these operations are disabled, the Flash will be permanently locked from writes or erasures until the next device reset. If an application never writes to Flash, it can intentionally lock the Flash by writing a non-0xA5 value to FLKEY from software.</p> <p>Read: When read, bits 1–0 indicate the current Flash lock state. 00: Flash is write/erase locked. 01: The first key code has been written (0xA5). 10: Flash is unlocked (writes/erases allowed). 11: Flash writes/erases disabled until the next reset.</p>

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SFR Definition 23.3. EECNTL: EEPROM Control

Bit	7	6	5	4	3	2	1	0
Name	EEEN					EEREAD	EEWRT	AUTOINC
Type	R/W	R				R/W		
Reset	0	0	0	0	0	0	0	1

SFR Address = 0xC5; SFR Page = F

Bit	Name	Description
7	EEEN	EEPROM Enable. 0: EEPROM control logic disabled. 1: EEPROM control logic enabled. EEPROM reads and writes can be performed.
6:4	Reserved	Reserved. Read = variable; Write = Don't Care
3	Reserved	Reserved. Read = 0b, Write = 0
2	EEREAD	EEPROM 32-Byte Read. 0: Does nothing. 1: 32 bytes of EEPROM Data will be read from Flash to internal RAM.
1	EEWRITE	EEPROM 32-Byte Write. 0: Does nothing. 1: 32 bytes of EEPROM Data will be written from internal RAM to Flash.
0	AUTOINC	Auto Increment. 0: Disable auto-increment. 1: Enable auto-increment.

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SFR Definition 28.2. XBR1: Port I/O Crossbar Register 1

Bit	7	6	5	4	3	2	1	0
Name	WEAKPUD	XBARE	T1E	T0E	ECIE		PCA0ME[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE2; SFR Page = F

Bit	Name	Function
7	WEAKPUD	Port I/O Weak Pullup Disable. 0: Weak Pullups enabled (except for Ports whose I/O are configured for analog mode). 1: Weak Pullups disabled.
6	XBARE	Crossbar Enable. 0: Crossbar disabled. 1: Crossbar enabled.
5	T1E	T1 Enable. 0: T1 unavailable at Port pin. 1: T1 routed to Port pin.
4	T0E	T0 Enable. 0: T0 unavailable at Port pin. 1: T0 routed to Port pin.
3	ECIE	PCA0 External Counter Input Enable. 0: ECI unavailable at Port pin. 1: ECI routed to Port pin.
2	Unused	Read = 0b; Write = Don't Care.
1:0	PCA0ME[1:0]	PCA Module I/O Enable Bits. 00: All PCA I/O unavailable at Port pins. 01: CEX0 routed to Port pin. 10: CEX0, CEX1 routed to Port pins. 11: CEX0, CEX1, CEX2 routed to Port pins.

SFR Definition 28.13. P1MDIN: Port 1 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDIN[7:0]							
Type	R/W							
Reset	1*	1	1	1	1	1	1	1

SFR Address = 0xF2; SFR Page = F

Bit	Name	Function
7:0	P1MDIN[7:0]	Analog Configuration Bits for P1.7–P1.0 (respectively). Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled. 0: Corresponding P1.n pin is configured for analog mode. 1: Corresponding P1.n pin is not configured for analog mode.
Note: On C8051F716 and C8051F717 devices, P1.7 will default to analog mode. If the P1MDIN register is written on the C8051F716 and C8051F717 devices, P1.7 should always be configured as analog.		

SFR Definition 28.14. P1MDOUT: Port 1 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA5; SFR Page = F

Bit	Name	Function
7:0	P1MDOUT[7:0]	Output Configuration Bits for P1.7–P1.0 (respectively). These bits are ignored if the corresponding bit in register P1MDIN is logic 0. 0: Corresponding P1.n Output is open-drain. 1: Corresponding P1.n Output is push-pull.

SFR Definition 28.37. P6DRV: Port 6 Drive Strength

Bit	7	6	5	4	3	2	1	0
Name			P6DRV[5:0]					
Type	R	R	R/W					
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC1; SFR Page = F

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care
5:0	P6DRV[5:0]	Drive Strength Configuration Bits for P6.5–P6.0 (respectively). Configures digital I/O Port cells to high or low output drive strength. 0: Corresponding P6.n Output has low output drive strength. 1: Corresponding P6.n Output has high output drive strength.

30.4.4. Data Register

The SMBus Data register SMB0DAT holds a byte of serial data to be transmitted or one that has just been received. Software may safely read or write to the data register when the SI flag is set. Software should not attempt to access the SMB0DAT register when the SMBus is enabled and the SI flag is cleared to logic 0, as the interface may be in the process of shifting a byte of data into or out of the register.

Data in SMB0DAT is always shifted out MSB first. After a byte has been received, the first bit of received data is located at the MSB of SMB0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in. SMB0DAT always contains the last data byte present on the bus. In the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data or address in SMB0DAT.

SFR Definition 30.5. SMB0DAT: SMBus Data

Bit	7	6	5	4	3	2	1	0
Name	SMB0DAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC2; SFR Page = 0

Bit	Name	Function
7:0	SMB0DAT[7:0]	SMBus Data. The SMB0DAT register contains a byte of data to be transmitted on the SMBus serial interface or a byte that has just been received on the SMBus serial interface. The CPU can read from or write to this register whenever the SI serial interrupt flag (SMB0CN.0) is set to logic 1. The serial data in the register remains stable as long as the SI flag is set. When the SI flag is not set, the system may be in the process of shifting data in/out and the CPU should not attempt to access this register.

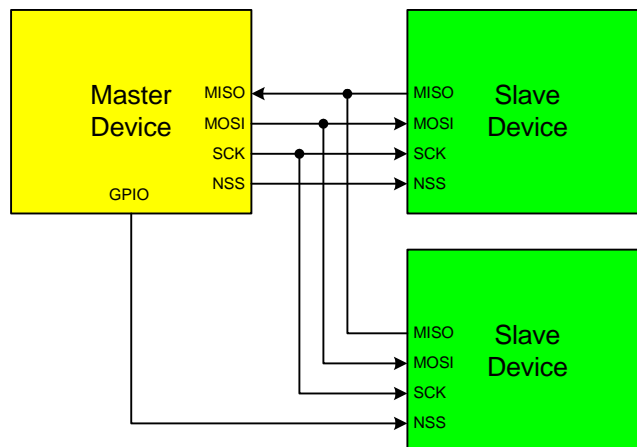


Figure 31.4. 4-Wire Single Master Mode and Slave Mode Connection Diagram

31.3. SPI0 Slave Mode Operation

When SPI0 is enabled and not configured as a master, it will operate as a SPI slave. As a slave, bytes are shifted in through the MOSI pin and out through the MISO pin by a master device controlling the SCK signal. A bit counter in the SPI0 logic counts SCK edges. When 8 bits have been shifted through the shift register, the SPIF flag is set to logic 1, and the byte is copied into the receive buffer. Data is read from the receive buffer by reading SPI0DAT. A slave device cannot initiate transfers. Data to be transferred to the master device is pre-loaded into the shift register by writing to SPI0DAT. Writes to SPI0DAT are double-buffered, and are placed in the transmit buffer first. If the shift register is empty, the contents of the transmit buffer will immediately be transferred into the shift register. When the shift register already contains data, the SPI will load the shift register with the transmit buffer's contents after the last SCK edge of the next (or current) SPI transfer.

When configured as a slave, SPI0 can be configured for 4-wire or 3-wire operation. The default, 4-wire slave mode, is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In 4-wire mode, the NSS signal is routed to a port pin and configured as a digital input. SPI0 is enabled when NSS is logic 0, and disabled when NSS is logic 1. The bit counter is reset on a falling edge of NSS. The NSS signal must be driven low at least 2 system clocks before the first active edge of SCK for each byte transfer. Figure 31.4 shows a connection diagram between two slave devices in 4-wire slave mode and a master device.

3-wire slave mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. NSS is not used in this mode, and is not mapped to an external port pin through the crossbar. Since there is no way of uniquely addressing the device in 3-wire slave mode, SPI0 must be the only slave device present on the bus. It is important to note that in 3-wire slave mode there is no external means of resetting the bit counter that determines when a full byte has been received. The bit counter can only be reset by disabling and re-enabling SPI0 with the SPIEN bit. Figure 31.3 shows a connection diagram between a slave device in 3-wire slave mode and a master device.

33. Timers

Each MCU includes four counter/timers: two are 16-bit counter/timers compatible with those found in the standard 8051, and two are 16-bit auto-reload timer for use with the ADC, SMBus, or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. Timer 2 and Timer 3 offer 16-bit and split 8-bit timer functionality with auto-reload. Additionally, Timer 3 offers the ability to be clocked from the external oscillator while the device is in Suspend mode, and can be used as a wake-up source. This allows for implementation of a very low-power system, including RTC capability.

Timer 0 and Timer 1 Modes:	Timer 2 Modes:	Timer 3 Modes:
13-bit counter/timer	16-bit timer with auto-reload	16-bit timer with auto-reload
16-bit counter/timer		
8-bit counter/timer with auto-reload	Two 8-bit timers with auto-reload	Two 8-bit timers with auto-reload
Two 8-bit counter/timers (Timer 0 only)		

Timers 0 and 1 may be clocked by one of five sources, determined by the Timer Mode Select bits (T1M–T0M) and the Clock Scale bits (SCA1–SCA0). The Clock Scale bits define a pre-scaled clock from which Timer 0 and/or Timer 1 may be clocked (See SFR Definition 33.1 for pre-scaled clock selection).

Timer 0/1 may then be configured to use this pre-scaled clock signal or the system clock. Timer 2 and Timer 3 may be clocked by the system clock, the system clock divided by 12, or the external oscillator clock source divided by 8.

Timer 0 and Timer 1 may also be operated as counters. When functioning as a counter, a counter/timer register is incremented on each high-to-low transition at the selected input pin (T0 or T1). Events with a frequency of up to one-fourth the system clock frequency can be counted. The input signal need not be periodic, but it should be held at a given level for at least two full system clock cycles to ensure the level is properly sampled.

33.1. Timer 0 and Timer 1

Each timer is implemented as a 16-bit register accessed as two separate bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The Counter/Timer Control register (TCON) is used to enable Timer 0 and Timer 1 as well as indicate status. Timer 0 interrupts can be enabled by setting the ET0 bit in the IE register (Section “21.2. Interrupt Register Descriptions” on page 140); Timer 1 interrupts can be enabled by setting the ET1 bit in the IE register (Section “21.2. Interrupt Register Descriptions” on page 140). Both counter/timers operate in one of four primary modes selected by setting the Mode Select bits T1M1–T0M0 in the Counter/Timer Mode register (TMOD). Each timer can be configured independently. Each operating mode is described below.

33.1.1. Mode 0: 13-bit Counter/Timer

Timer 0 and Timer 1 operate as 13-bit counter/timers in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically, and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSBs of the 13-bit counter/timer. TL0 holds the five LSBs in bit positions TL0.4–TL0.0. The three upper bits of TL0 (TL0.7–TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 in TCON is set and an interrupt will occur if Timer 0 interrupts are enabled.

The C/T0 bit in the TMOD register selects the counter/timer's clock source. When C/T0 is set to logic 1, high-to-low transitions at the selected Timer 0 input pin (T0) increment the timer register (Refer to Section “28.3. Priority Crossbar Decoder” on page 185 for information on selecting and configuring external I/O pins). Clearing C/T selects the clock defined by the T0M bit in register CKCON. When T0M is set, Timer 0 is clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 33.1).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 in the TMOD register is logic 0 or the input signal INT0 is active as defined by bit IN0PL in register IT01CF (see SFR Definition 21.7). Setting GATE0 to 1 allows the timer to be controlled by the external input signal INT0 (see Section “21.2. Interrupt Register Descriptions” on page 140), facilitating pulse width measurements

TR0	GATE0	INT0	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled

Note: X = Don't Care

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal INT1 is used with Timer 1; the INT1 polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 21.7).

35.2. C2CK Pin Sharing

The C2CK pin is shared with the $\overline{\text{RST}}$ signal on this device family. If the $\overline{\text{RST}}$ pin is used by other parts of the system, debugging and programming the device can still be accomplished without disrupting the rest of the system. If this is desired, it is normally necessary to add a resistor to isolate the system's reset line from the C2CK signal. This external resistors would not be necessary for production boards, where debugging capabilities are not needed. A typical isolation configuration is shown in Figure 35.1.

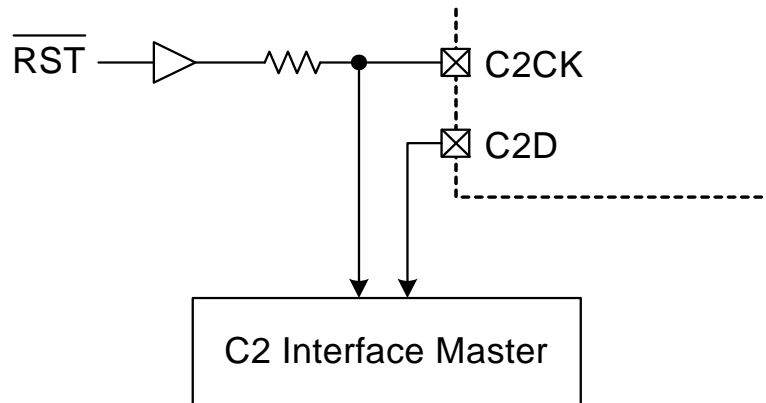


Figure 35.1. Typical C2CK Pin Sharing

The configuration in Figure 35.1 assumes the $\overline{\text{RST}}$ pin on the target device is used as an input only. Additional resistors may be necessary depending on the specific application.



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