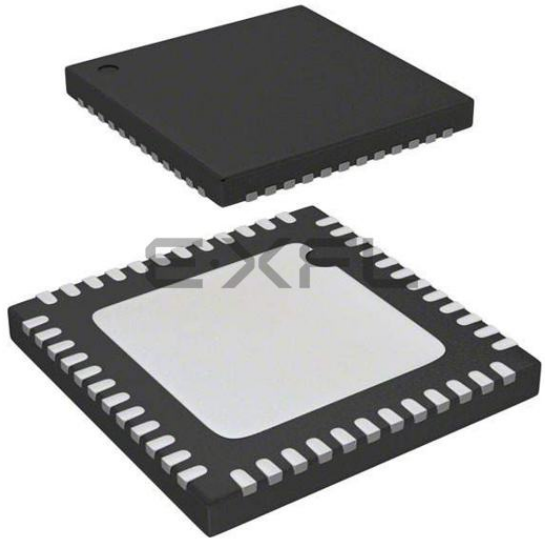

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Cap Sense, POR, PWM, WDT
Number of I/O	39
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f715-gmr

Table 3.1. Pin Definitions for the C8051F70x/71x (Continued)

Name	TQFP64	TQFP48 QFN48	QFN32	QFN24	Type	Description
P5.1	10	10	7	—	D I/O or A In	Port 5.0. CS0 input pin 26.
P5.2	7	7	6	—	D I/O or A In	Port 5.2. CS0 input pin 27
P5.3	6	6	5	—	D I/O or A In	Port 5.3. CS0 input pin 28.
P5.4	5	5	4	—	D I/O or A In	Port 5.4. CS0 input pin 29.
P5.5	4	4	3	—	D I/O or A In	Port 5.5. CS0 input pin 30.
P5.6	3	3	2	—	D I/O or A In	Port 5.6. CS0 input pin 31.
P5.7	2	2	1	—	D I/O or A In	Port 5.7. CS0 input pin 32.
P6.0	1	—	—	—	D I/O	Port 6.0. CS0 input pin 33.
P6.1	64	—	—	—	D I/O	Port 6.1. CS0 input pin 34.
P6.2	63	—	—	—	D I/O	Port 6.2. CS0 input pin 35.
P6.3	62	1	32	—	D I/O	Port 6.3. CS0 input pin 36.
P6.4	61	48	31	1	D I/O	Port 6.4. CS0 input pin 37.
P6.5	60	47	30	24	D I/O	Port 6.5. CS0 input pin 38.

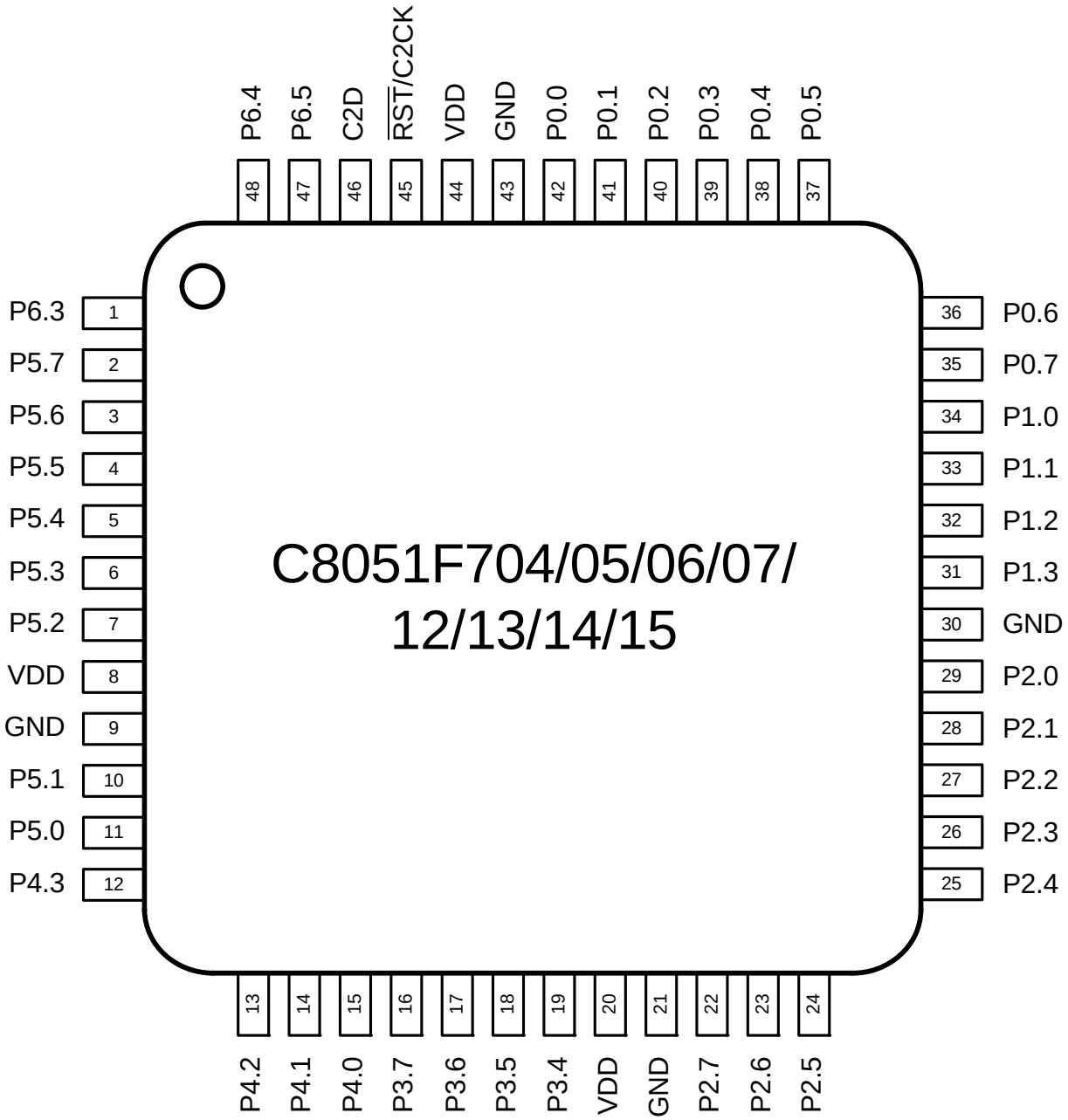

Figure 3.2. C8051F7xx-GQ QFP48 Pinout Diagram (Top View)

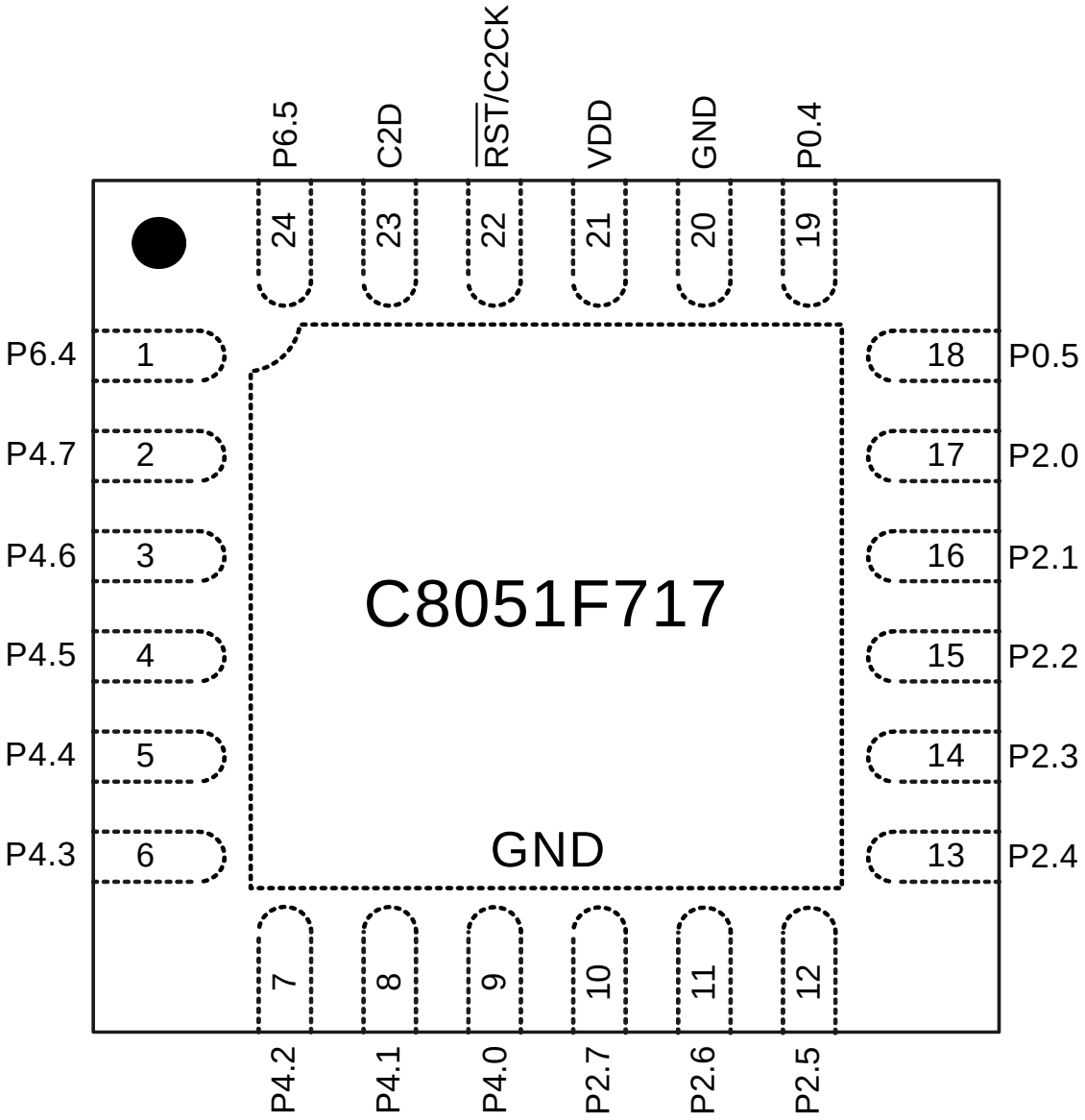

Figure 3.5. C8051F717-GM QFN24 Pinout Diagram (Top View)

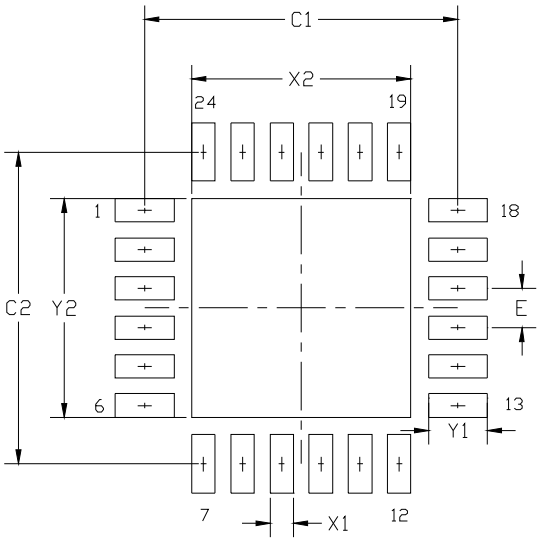

Figure 8.2. QFN-24 Recommended PCB Land Pattern

Table 8.2. QFN-24 PCB Land Pattern Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	3.90	4.00	X2	2.70	2.80
C2	3.90	4.00	Y1	0.65	0.75
E	0.50 BSC		Y2	2.70	2.80
X1	0.20	0.30			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 mm x 1.10 mm openings on a 1.30 mm pitch should be used for the center pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

SFR Definition 15.11. CS0MD2: Capacitive Sense Mode 2

Bit	7	6	5	4	3	2	1	0
Name	CS0CR[1:0]		CS0DT[2:0]			CS0IA[2:0]		
Type	R/W		R/W			R/W		
Reset	0	1	0	0	0	0	0	0

SFR Address = 0xBE; SFR Page = F

Bit	Name	Description
7:6	CS0CR[1:0]	**CS0 Conversion Rate.** These bits control the conversion rate of the CS0 module. See the electrical specifications table for specific timing. 00: Conversions last 12 internal CS0 clocks and are 12 bits in length. 01: Conversions last 13 internal CS0 clocks and are 13 bits in length. 10: Conversions last 14 internal CS0 clocks and are 14 bits in length. 11: Conversions last 16 internal CS0 clocks.and are 16 bits in length.
5:3	CS0DT[2:0]	**CS0 Discharge Time.** These bits adjust the primary CS0 reset time. For most touch-sensitive switches, the default (fastest) value is sufficient, and these bits should not be modified. 000: Discharge time is 0.75 µs (recommended for most switches) 001: Discharge time is 1.0 µs 010: Discharge time is 1.2 µs 011: Discharge time is 1.5 µs 100: Discharge time is 2 µs 101: Discharge time is 3 µs 110: Discharge time is 6 µs 111: Discharge time is 12 µs
2:0	CS0IA[2:0]	**CS0 Output Current Adjustment.** These bits allow the user to adjust the output current used to charge up the capacitive sensor element. For most touch-sensitive switches, the default (highest) current is sufficient, and these bits should not be modified. 000: Full Current (recommended for most switches) 001: 1/8 Current 010: 1/4 Current 011: 3/8 Current 100: 1/2 Current 101: 5/8 Current 110: 3/4 Current 111: 7/8 Current

18.6.1.2. 8-bit MOVX without Bank Select: EMI0CF[4:2] = 101 or 111

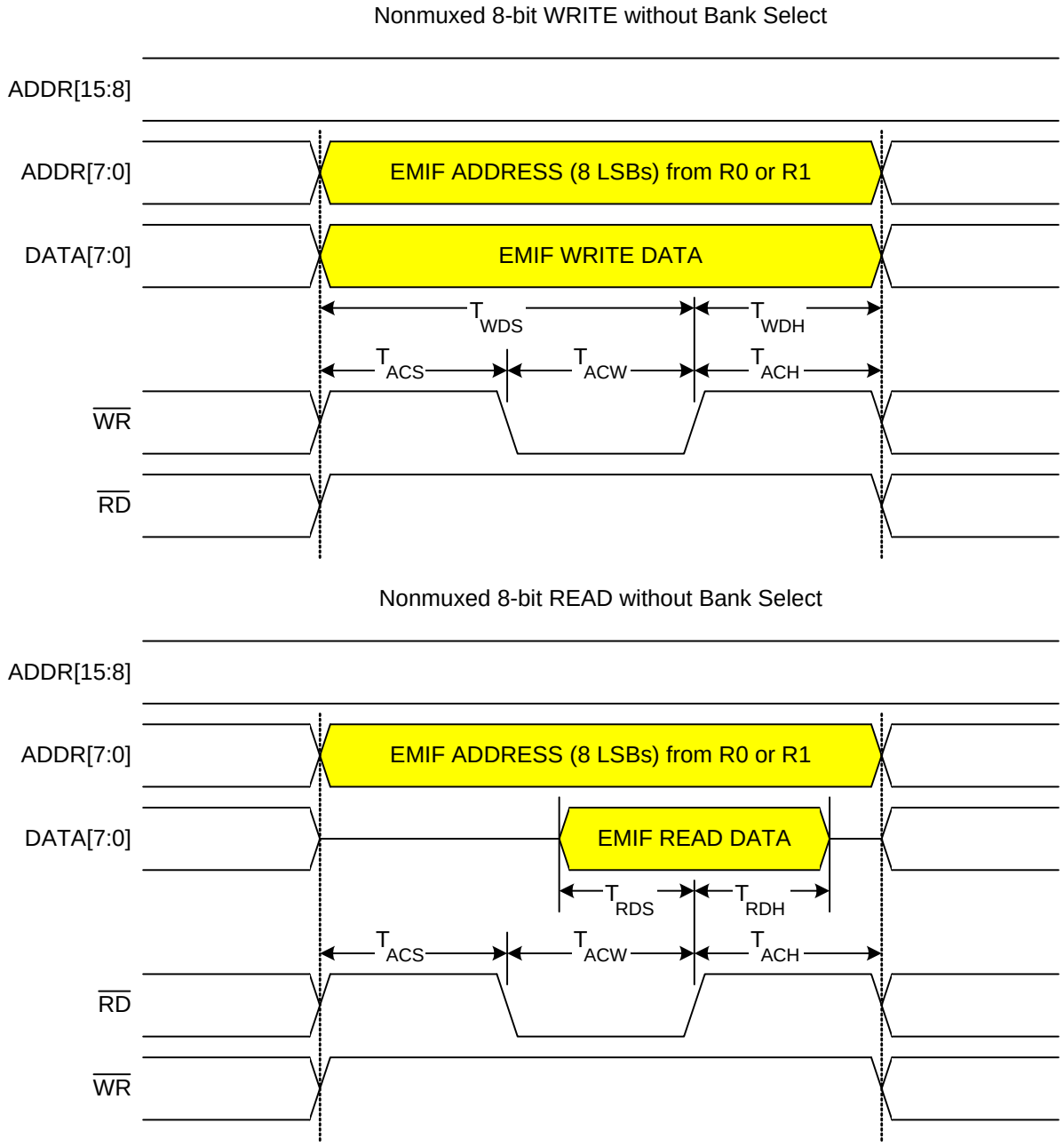

Figure 18.5. Non-multiplexed 8-bit MOVX without Bank Select Timing

18.6.1.3. 8-bit MOVX with Bank Select: EMI0CF[4:2] = 110

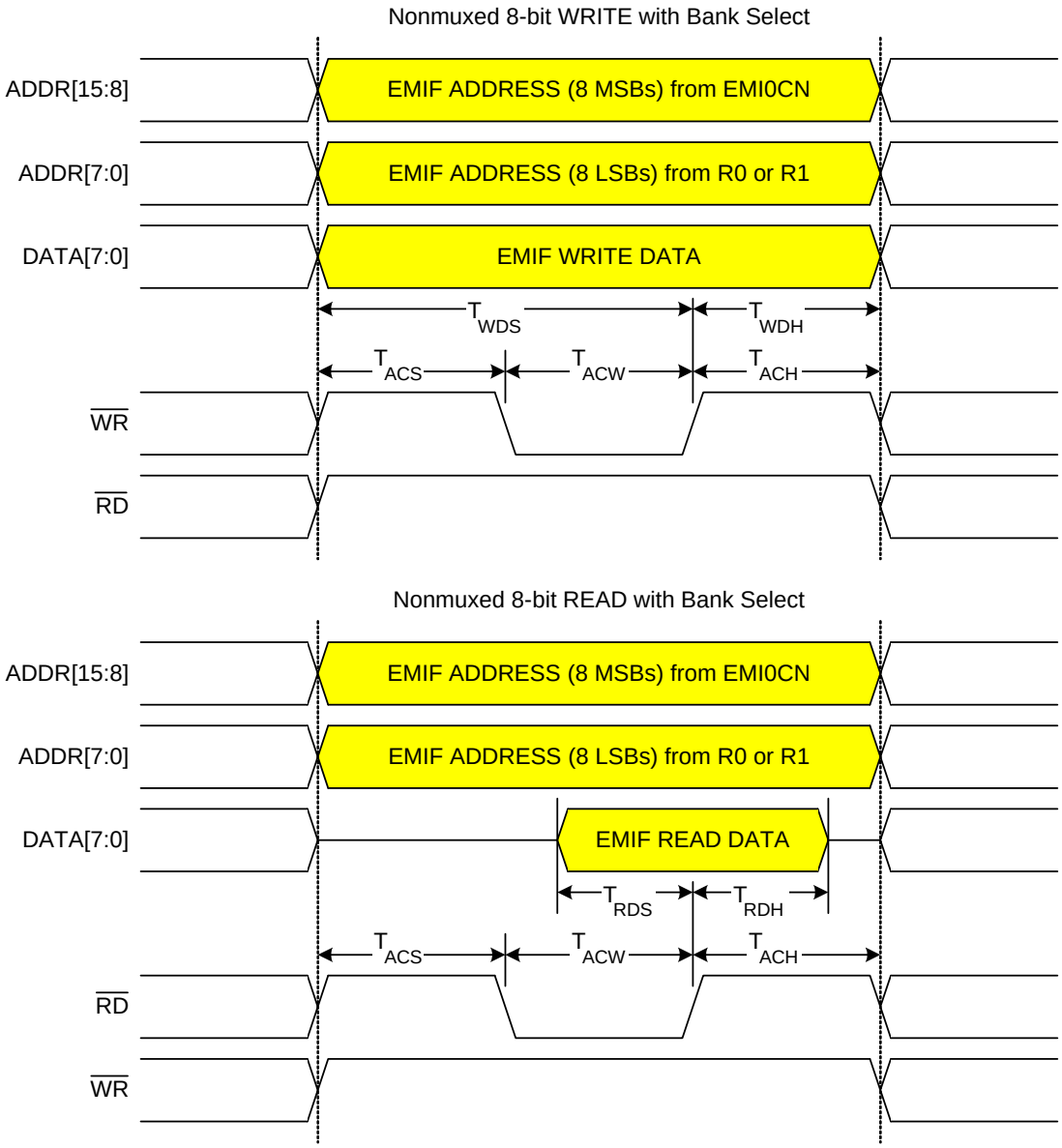

Figure 18.6. Non-Multiplexed 8-Bit MOVX with Bank Select Timing

Table 20.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Page	Description	Page
P0MDIN	0xF1	F	Port 0 Input Mode Configuration	195
P0MDOUT	0xA4	F	Port 0 Output Mode Configuration	196
P0SKIP	0xD4	F	Port 0 Skip	196
P1	0x90	All Pages	Port 1 Latch	197
P1DRV	0xFA	F	Port 1 Drive Strength	199
P1MASK	0xE2	0	P0 Mask	193
P1MAT	0xE1	0	P1 Match	194
P1MDIN	0xF2	F	Port 1 Input Mode Configuration	198
P1MDOUT	0xA5	F	Port 1 Output Mode Configuration	198
P1SKIP	0xD5	F	Port 1 Skip	199
P2	0xA0	All Pages	Port 2 Latch	200
P2DRV	0xFB	F	Port 2 Drive Strength	202
P2MDIN	0xF3	F	Port 2 Input Mode Configuration	200
P2MDOUT	0xA6	F	Port 2 Output Mode Configuration	201
P2SKIP	0xD6	F	Port 2 Skip	201
P3	0xB0	All Pages	Port 3 Latch	202
P3DRV	0xFC	F	Port 3 Drive Strength	204
P3MDIN	0xF4	F	Port 3 Input Mode Configuration	203
P3MDOUT	0xAF	F	Port 3 Output Mode Configuration	203
P4	0xAC	All Pages	Port 4 Latch	204
P4DRV	0xFD	F	Port 4 Drive Strength	206
P4MDIN	0xF5	F	Port 4 Input Mode Configuration	205
P4MDOUT	0x9A	F	Port 4 Output Mode Configuration	205
P5	0xB3	All Pages	Port 5 Latch	206
P5DRV	0xFE	F	Port 5 Drive Strength	208
P5MDIN	0xF6	F	Port 5 Input Mode Configuration	207
P5MDOUT	0x9B	F	Port 5 Output Mode Configuration	207
P6	0xB2	All Pages	Port 6 Latch	208
P6DRV	0xC1	F	Port 6 Drive Strength	210
P6MDIN	0xF7	F	Port 6 Input Mode Configuration	209
P6MDOUT	0x9C	F	Port 6 Output Mode Configuration	209
PCA0CN	0xD8	All Pages	PCA Control	295
PCA0CPH0	0xFC	0	PCA Capture 0 High	300
PCA0CPH1	0xEA	0	PCA Capture 1 High	300
PCA0CPH2	0xEC	0	PCA Capture 2 High	300
PCA0CPL0	0xFB	0	PCA Capture 0 Low	300
PCA0CPL1	0xE9	0	PCA Capture 1 Low	300
PCA0CPL2	0xEB	0	PCA Capture 2 Low	300

Table 20.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Page	Description	Page
TMR3CN	0x91	0	Timer/Counter 3 Control	281
TMR3H	0x95	0	Timer/Counter 3 High	283
TMR3L	0x94	0	Timer/Counter 3 Low	283
TMR3RLH	0x93	0	Timer/Counter 3 Reload High	282
TMR3RLL	0x92	0	Timer/Counter 3 Reload Low	282
VDM0CN	0xFF	All Pages	VDD Monitor Control	166
WDTCN	0xE3	All Pages	Watchdog Timer Control	170
XBR0	0xE1	F	Port I/O Crossbar Control 0	190
XBR1	0xE2	F	Port I/O Crossbar Control 1	191
All other SFR Locations			Reserved	

23. EEPROM

C8051F700/1/4/5/8/9 and C8051F712/3 devices have hardware which emulates 32 bytes of non-volatile, byte-programmable EEPROM data space. The module mirrors each non-volatile byte through 32 bytes of volatile data space. This data space can be accessed indirectly through EEADDR and EEDATA. Users can copy the complete 32-byte image between EEPROM space and volatile space using controls in the EECNTL SFR.

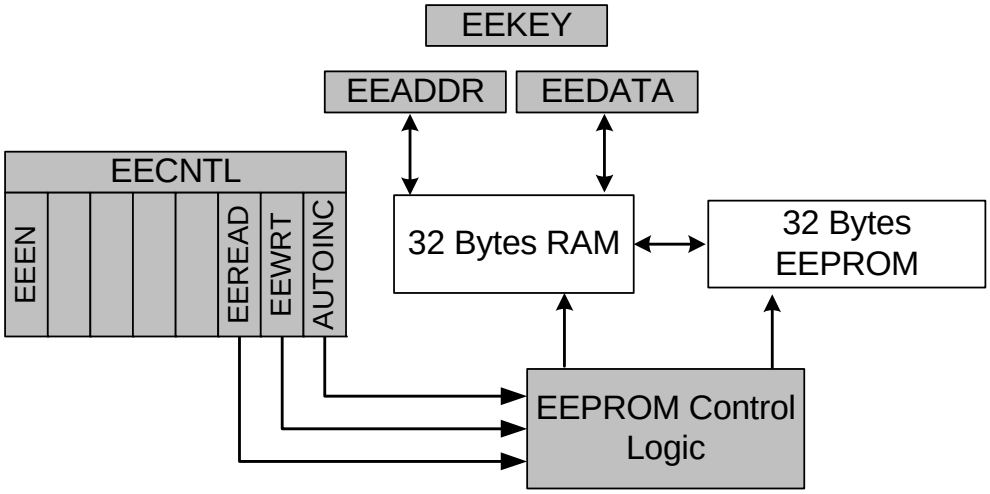

Figure 23.1. EEPROM Block Diagram

23.1. RAM Reads and Writes

In order to perform EEPROM reads and writes, the EEPROM control logic must be enabled by setting EEEN (EECNTL.7).

32 bytes of RAM can be accessed indirectly through EEADDR and EEDATA. To write to a byte of RAM, write address of byte to EEADDR and then write the value to be written to EEDATA. To read a byte from RAM, write address of byte to be read to EEADDR. The value stored at that address can then be read from EEDATA.

23.2. Auto Increment

When AUTOINC (EECNTL.0) is set, EEADDR will increment by one after each write to EEDATA and each read from EEDATA. When Auto Increment is enabled and EEADDR reaches the top address of dedicated RAM space, the next write to or read from EEDATA will cause EEADDR to wrap along the address boundary, which will set the address to 0.

23.3. Interfacing with the EEPROM

The EEPROM is accessed through the dedicated 32 bytes of RAM. Writes to EEPROM are allowed only after writes have been enabled (see “23.4. EEPROM Security”). The contents of the EEPROM can be uploaded to the RAM by setting EEREAD (EECNTL.2). Contents of RAM can be downloaded to EEPROM by setting EEWRT (EENTL.1).

Note: A minimum SYSCLK frequency is required for writing EEPROM memory, as detailed in Section “Table 9.9. EEPROM Electrical Characteristics” on page 52.

SFR Definition 26.1. WDTCN: Watchdog Timer Control

Bit	7	6	5	4	3	2	1	0
Name	WDT[7:0]							
Type	R/W							
Reset	0	0	0	1	0	1	1	1

SFR Address = 0xE3; SFR Page = All Pages

Bit	Name	Description	Write	Read
7:0	WDT[7:0]	**WDT Control.**	Writing 0xA5 both enables and reloads the WDT. Writing 0xDE followed within 4 system clocks by 0xAD disables the WDT. Writing 0xFF locks out the disable feature.	
4	WDTSTATUS	**Watchdog Status Bit.**		0: WDT is inactive 1: WDT is active
2:0	WDTTIMEOUT	**Watchdog Timeout Interval Bits.**	WDTCN[2:0] bits set the Watchdog Timeout Interval. When writing these bits, WDTCN[7] must be set to 0.	

27.3.1. External Crystal Example

If a crystal or ceramic resonator is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 27.1, Option 1. The External Oscillator Frequency Control value (XFCN) should be chosen from the Crystal column of the table in SFR Definition 27.4 (OSCXCN register). For example, an 11.0592 MHz crystal requires an XFCN setting of 111b and a 32.768 kHz Watch Crystal requires an XFCN setting of 001b. After an external 32.768 kHz oscillator is stabilized, the XFCN setting can be switched to 000 to save power. It is recommended to enable the missing clock detector before switching the system clock to any external oscillator source.

When the crystal oscillator is first enabled, the oscillator amplitude detection circuit requires a settling time to achieve proper bias. Introducing a delay of 1 ms between enabling the oscillator and checking the XTLVLD bit will prevent a premature switch to the external oscillator as the system clock. Switching to the external oscillator before the crystal oscillator has stabilized can result in unpredictable behavior. The recommended procedure is:

1. Force XTAL1 and XTAL2 to a low state. This involves enabling the Crossbar and writing 0 to the port pins associated with XTAL1 and XTAL2.
2. Configure XTAL1 and XTAL2 as analog inputs.
3. Enable the external oscillator.
4. Wait at least 1 ms.
5. Poll for XTLVLD = 1.
6. If desired, enable the Missing Clock Detector.
7. Switch the system clock to the external oscillator.

Important Note on External Crystals: Crystal oscillator circuits are quite sensitive to PCB layout. The crystal should be placed as close as possible to the XTAL pins on the device. The traces should be as short as possible and shielded with ground plane from any other traces which could introduce noise or interference.

The capacitors shown in the external crystal configuration provide the load capacitance required by the crystal for correct oscillation. These capacitors are "in series" as seen by the crystal and "in parallel" with the stray capacitance of the XTAL1 and XTAL2 pins.

Note: The desired load capacitance depends upon the crystal and the manufacturer. Please refer to the crystal data sheet when completing these calculations.

For example, a tuning-fork crystal of 32.768 kHz with a recommended load capacitance of 12.5 pF should use the configuration shown in Figure 27.1, Option 1. The total value of the capacitors and the stray capacitance of the XTAL pins should equal 25 pF. With a stray capacitance of 3 pF per pin, the 22 pF capacitors yield an equivalent capacitance of 12.5 pF across the crystal, as shown in Figure 27.2.

28.2.2. Assigning Port I/O Pins to Digital Functions

Any Port pins not assigned to analog functions may be assigned to digital functions or used as GPIO. Most digital functions rely on the Crossbar for pin assignment; however, some digital functions bypass the Crossbar in a manner similar to the analog functions listed above. **Port pins used by these digital functions and any Port pins selected for use as GPIO should have their corresponding bit in PnSKIP set to 1.** Table 28.2 shows all available digital functions and the potential mapping of Port I/O to each digital function.

Table 28.2. Port I/O Assignment for Digital Functions

Digital Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
UART0, SPI0, SMBus, CP0, CP0A, SYSCLK, PCA0 (CEX0-2 and ECI), T0 or T1.	Any Port pin available for assignment by the Crossbar. This includes P0.0–P2.7 pins which have their PnSKIP bit set to 0. **Note:** The Crossbar will always assign UART0 pins to P0.4 and P0.5.	XBR0, XBR1
Any pin used for GPIO	P0.0–P6.5	P0SKIP, P1SKIP, P2SKIP
External Memory Interface	P3.0–P6.2	EMI0CF

28.2.3. Assigning Port I/O Pins to External Event Trigger Functions

External event trigger functions can be used to trigger an interrupt or wake the device from a low power mode when a transition occurs on a digital I/O pin. The event trigger functions do not require dedicated pins and will function on both GPIO pins (PnSKIP = 1) and pins in use by the Crossbar (PnSKIP = 0). External event trigger functions cannot be used on pins configured for analog I/O. Table 28.3 shows all available external event trigger functions.

Table 28.3. Port I/O Assignment for External Event Trigger Functions

Event Trigger Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
External Interrupt 0	P0.0–P0.7	IT01CF
External Interrupt 1	P0.0–P0.7	IT01CF
Port Match	P0.0–P1.7	P0MASK, P0MAT P1MASK, P1MAT

SFR Definition 29.1. CRC0CN: CRC0 Control

Bit	7	6	5	4	3	2	1	0
Name				CRC0SEL	CRC0INIT	CRC0VAL	CRC0PNT[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x91; SFR Page = F

Bit	Name	Function
7:5	Unused	Read = 000b; Write = Don't Care.
4	CRC0SEL	**CRC0 Polynomial Select Bit.** This bit selects the CRC0 polynomial and result length (32-bit or 16-bit). 0: CRC0 uses the 32-bit polynomial 0x04C11DB7 for calculating the CRC result. 1: CRC0 uses the 16-bit polynomial 0x1021 for calculating the CRC result.
3	CRC0INIT	**CRC0 Result Initialization Bit.** Writing a 1 to this bit initializes the entire CRC result based on CRC0VAL.
2	CRC0VAL	**CRC0 Set Value Initialization Bit.** This bit selects the set value of the CRC result. 0: CRC result is set to 0x00000000 on write of 1 to CRC0INIT. 1: CRC result is set to 0xFFFFFFFF on write of 1 to CRC0INIT.
1:0	CRC0PNT[1:0]	**CRC0 Result Pointer.** Specifies the byte of the CRC result to be read/written on the next access to CRC0DAT. The value of these bits will auto-increment upon each read or write. For CRC0SEL = 0: 00: CRC0DAT accesses bits 7–0 of the 32-bit CRC result. 01: CRC0DAT accesses bits 15–8 of the 32-bit CRC result. 10: CRC0DAT accesses bits 23–16 of the 32-bit CRC result. 11: CRC0DAT accesses bits 31–24 of the 32-bit CRC result. For CRC0SEL = 1: 00: CRC0DAT accesses bits 7–0 of the 16-bit CRC result. 01: CRC0DAT accesses bits 15–8 of the 16-bit CRC result. 10: CRC0DAT accesses bits 7–0 of the 16-bit CRC result. 11: CRC0DAT accesses bits 15–8 of the 16-bit CRC result.

Table 30.3. Sources for Hardware Changes to SMB0CN

Bit	Set by Hardware When:	Cleared by Hardware When:
MASTER	■ A START is generated.	■ A STOP is generated. ■ Arbitration is lost.
TXMODE	■ START is generated. ■ SMB0DAT is written before the start of an SMBus frame.	■ A START is detected. ■ Arbitration is lost. ■ SMB0DAT is not written before the start of an SMBus frame.
STA	■ A START followed by an address byte is received.	■ Must be cleared by software.
STO	■ A STOP is detected while addressed as a slave. ■ Arbitration is lost due to a detected STOP.	■ A pending STOP is generated.
ACKRQ	■ A byte has been received and an ACK response value is needed (only when hardware ACK is not enabled).	■ After each ACK cycle.
ARBLOST	■ A repeated START is detected as a MASTER when STA is low (unwanted repeated START). ■ SCL is sensed low while attempting to generate a STOP or repeated START condition. ■ SDA is sensed low while transmitting a 1 (excluding ACK bits).	■ Each time SI is cleared.
ACK	■ The incoming ACK value is low (ACKNOWLEDGE).	■ The incoming ACK value is high (NOT ACKNOWLEDGE).
SI	■ A START has been generated. ■ Lost arbitration. ■ A byte has been transmitted and an ACK/NACK received. ■ A byte has been received. ■ A START or repeated START followed by a slave address + R/W has been received. ■ A STOP has been received.	■ Must be cleared by software.

30.4.3. Hardware Slave Address Recognition

The SMBus hardware has the capability to automatically recognize incoming slave addresses and send an ACK without software intervention. Automatic slave address recognition is enabled by setting the EHACK bit in register SMB0ADM to 1. This will enable both automatic slave address recognition and automatic hardware ACK generation for received bytes (as a master or slave). More detail on automatic hardware ACK generation can be found in Section 30.4.2.2.

The registers used to define which address(es) are recognized by the hardware are the SMBus Slave Address register (SFR Definition 30.3) and the SMBus Slave Address Mask register (SFR Definition 30.4). A single address or range of addresses (including the General Call Address 0x00) can be specified using these two registers. The most-significant seven bits of the two registers are used to define which addresses will be ACKed. A 1 in bit positions of the slave address mask SLVM[6:0] enable a comparison between the received slave address and the hardware's slave address SLV[6:0] for those bits. A 0 in a bit of the slave address mask means that bit will be treated as a "don't care" for comparison purposes. In this

Table 30.5. SMBus Status Decoding: Hardware ACK Disabled (EHACK = 0) (Continued)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Slave Transmitter	0100	0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	X	0001
		0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	X	0100
		0	1	X	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	X	0001
	0101	0	X	X	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	X	—
Slave Receiver	0010	1	0	X	A slave address + R/W was received; ACK requested.	If Write, Acknowledge received address	0	0	1	0000
						If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
						NACK received address.	0	0	0	—
		1	1	X	Lost arbitration as master; slave address + R/W received; ACK requested.	If Write, Acknowledge received address	0	0	1	0000
						If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
						NACK received address.	0	0	0	—
						Reschedule failed transfer; NACK received address.	1	0	0	1110
	0001	0	0	X	A STOP was detected while addressed as a Slave Transmitter or Slave Receiver.	Clear STO.	0	0	X	—
		1	1	X	Lost arbitration while attempting a STOP.	No action required (transfer complete/aborted).	0	0	0	—
	0000	1	0	X	A slave byte was received; ACK requested.	Acknowledge received byte; Read SMB0DAT.	0	0	1	0000
						NACK received byte.	0	0	0	—

31. Enhanced Serial Peripheral Interface (SPI0)

The Enhanced Serial Peripheral Interface (SPI0) provides access to a flexible, full-duplex synchronous serial bus. SPI0 can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI0 in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

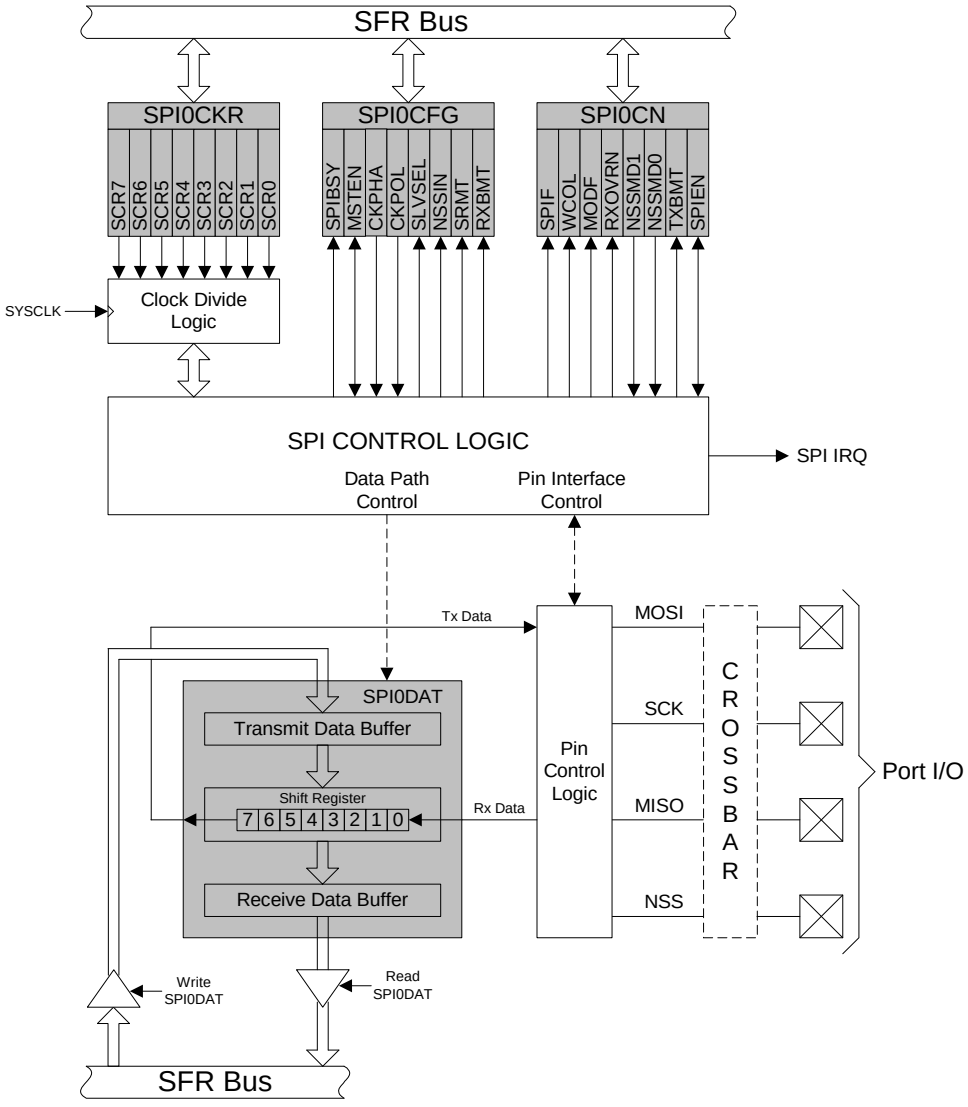

Figure 31.1. SPI Block Diagram

33.3. Timer 3

Timer 3 is a 16-bit timer formed by two 8-bit SFRs: TMR3L (low byte) and TMR3H (high byte). Timer 3 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T3SPLIT bit (TMR3CN.3) defines the Timer 3 operation mode.

Timer 3 may be clocked by the system clock, the system clock divided by 12, or the external oscillator source divided by 8. The external clock mode is ideal for real-time clock (RTC) functionality, where the internal high-frequency oscillator drives the system clock while Timer 3 is clocked by an external oscillator source. The external oscillator source divided by 8 is synchronized with the system clock when in all operating modes except suspend. When the internal oscillator is placed in suspend mode, The external clock/8 signal can directly drive the timer. This allows the use of an external clock to wake up the device from suspend mode. The timer will continue to run in suspend mode and count up. When the timer overflow occurs, the device will wake from suspend mode, and begin executing code again. The timer value may be set prior to entering suspend, to overflow in the desired amount of time (number of clocks) to wake the device. If a wake-up source other than the timer wakes the device from suspend mode, it may take up to three timer clocks before the timer registers can be read or written. During this time, the STSYNC bit in register OSCICN will be set to 1, to indicate that it is not safe to read or write the timer registers.

33.3.1. 16-bit Timer with Auto-Reload

When T3SPLIT (TMR3CN.3) is zero, Timer 3 operates as a 16-bit timer with auto-reload. Timer 3 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 3 reload registers (TMR3RLH and TMR3RLL) is loaded into the Timer 3 register as shown in Figure 33.7, and the Timer 3 High Byte Overflow Flag (TMR3CN.7) is set. If Timer 3 interrupts are enabled (if EIE1.7 is set), an interrupt will be generated on each Timer 3 overflow. Additionally, if Timer 3 interrupts are enabled and the TF3LEN bit is set (TMR3CN.5), an interrupt will be generated each time the lower 8 bits (TMR3L) overflow from 0xFF to 0x00.

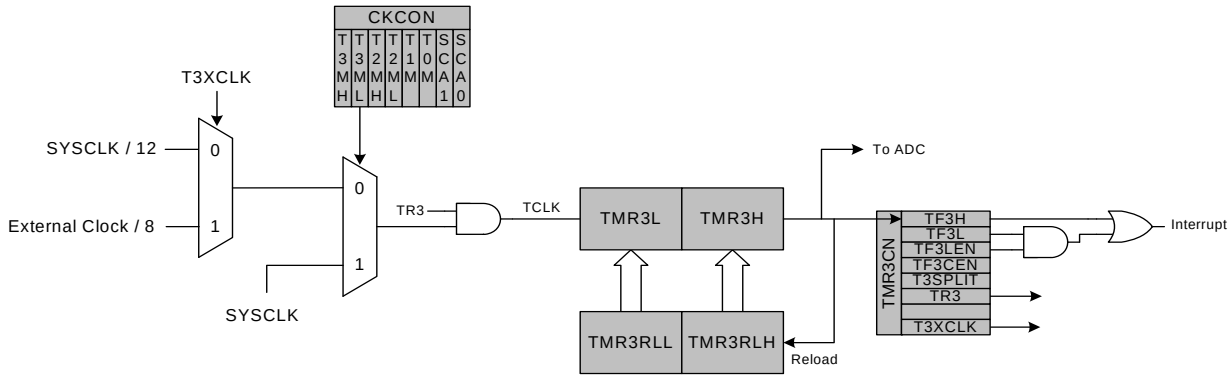

Figure 33.7. Timer 3 16-Bit Mode Block Diagram

C2 Register Definition 35.4. FPCTL: C2 Flash Programming Control

Bit	7	6	5	4	3	2	1	0
Name	FPCTL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0x02

Bit	Name	Function
7:0	FPCTL[7:0]	**C2 Flash Programming Control Register.** This register is used to enable Flash programming via the C2 interface. To enable C2 Flash programming, the following codes must be written in order: 0x02, 0x01. Once C2 Flash programming is enabled, a system reset must be issued to resume normal operation.

C2 Register Definition 35.5. FPDAT: C2 Flash Programming Data

Bit	7	6	5	4	3	2	1	0
Name	FPDAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xBF

Bit	Name	Function	
7:0	FPDAT[7:0]	**C2 Flash Programming Data Register.** This register is used to pass Flash commands, addresses, and data during C2 Flash accesses. Valid commands are listed below.	
		Code	**Command**
		0x06	Flash Block Read
		0x07	Flash Block Write
		0x08	Flash Page Erase
		0x03	Device Erase

35.2. C2CK Pin Sharing

The C2CK pin is shared with the $\overline{\text{RST}}$ signal on this device family. If the $\overline{\text{RST}}$ pin is used by other parts of the system, debugging and programming the device can still be accomplished without disrupting the rest of the system. If this is desired, it is normally necessary to add a resistor to isolate the system's reset line from the C2CK signal. This external resistors would not be necessary for production boards, where debugging capabilities are not needed. A typical isolation configuration is shown in Figure 35.1.

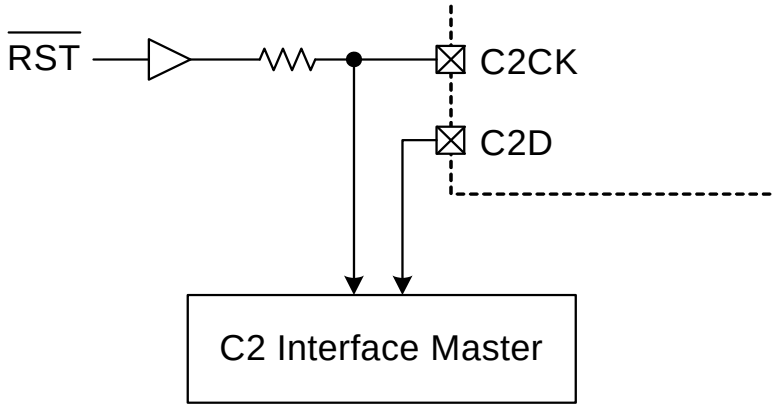

Figure 35.1. Typical C2CK Pin Sharing

The configuration in Figure 35.1 assumes the $\overline{\text{RST}}$ pin on the target device is used as an input only. Additional resistors may be necessary depending on the specific application.