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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Cap Sense, POR, PWM, Temp Sensor, WDT
Number of I/O	29
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f716-gmr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Figure 1.1. C8051F700/1 Block Diagram



SFR Definition 10.2. ADC0H: ADC0 Data Word MSB

Bit	7	6	5	4	3	2	1	0
Name	ADC0H[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xBE; SFR Page = 0

Bit	Name	Function
7:0	ADC0H[7:0]	ADC0 Data Word High-Order Bits.
		For AD0LJST = 0: Bits 7:2 will read 000000b. Bits 1–0 are the upper 2 bits of the 10- bit ADC0 Data Word.
		For AD0LJST = 1: Bits 7:0 are the most-significant bits of the 10-bit ADC0 Data Word. Note: In 8-bit mode AD0LJST is ignored, and ADC0H holds the 8-bit data word.

SFR Definition 10.3. ADC0L: ADC0 Data Word LSB

Bit	7	6	5	4	3	2	1	0	
Name	ADC0L[7:0]								
Туре	R/W								
Reset	0	0	0	0	0	0	0	0	

SFR Address = 0xBD; SFR Page = 0

Bit	Name	Function
7:0	ADC0L[7:0]	ADC0 Data Word Low-Order Bits.
		For AD0LJST = 0: Bits 7:0 are the lower 8 bits of the 10-bit Data Word.
		For AD0LJST = 1: Bits 7:6 are the lower 2 bits of the 10-bit Data Word. Bits 5–0 will always read 0.
		Note: In 8-bit mode AD0LJST is ignored, and ADC0L will read back 00000000b.



SFR Definition 12.1. REF0CN: Voltage Reference Control

Bit	7	6	5	4	3	2	1	0
Name			REFGND	REFSL		TEMPE	BIASE	
Туре	R	R	R/W	R/W	R/W	R/W	R/W	R
Reset	0	0	0	1	0	0	0	0

SFR Address = 0xD2; SFR Page = F

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care.
5	REFGND	Analog Ground Reference.
		Selects the ADC0 ground reference.
		0: The ADC0 ground reference is the GND pin.
		1: The ADC0 ground reference is the P0.1/AGND pin.
4:3	REFSL	Voltage Reference Select.
		Selects the ADC0 voltage reference.
		00: The ADC0 voltage reference is the P0.0/VREF pin.
		01: The ADC0 voltage reference is the VDD pin.
		10: The ADC0 voltage reference is the internal 1.8 V digital supply voltage.
		11: The ADC0 voltage reference is the internal 1.6 V high-speed voltage reference.
2	TEMPE	Temperature Sensor Enable.
		Enables/Disables the internal temperature sensor.
		0: Temperature Sensor Disabled.
		1: Temperature Sensor Enabled.
1	BIASE	Internal Analog Bias Generator Enable Bit.
		0: Internal Bias Generator off.
		1: Internal Bias Generator on.
0	Unused	Read = 0b; Write = Don't Care.



14.1. Comparator Multiplexer

C8051F70x/71x devices include an analog input multiplexer to connect Port I/O pins to the comparator inputs. The Comparator0 inputs are selected in the CPT0MX register (SFR Definition 14.3). The CMX0P2–CMX0P0 bits select the Comparator0 positive input; the CMX0N2–CMX0N0 bits select the Comparator0 negative input.

Important Note About Comparator Inputs: The Port pins selected as comparator inputs should be configured as analog inputs in their associated Port configuration register, and configured to be skipped by the Crossbar (for details on Port configuration, see Section "28.6. Special Function Registers for Accessing and Configuring Port I/O" on page 194).



*P1.7 on 64 and 48-pin devices, P2.0 on 32 and 24-pin devices





SFR Definition 14.3. CPT0MX: Comparator0 MUX Selection

Bit	7	6	5	4	3	2		1	0
Nam	e		CMX0N[2:0]				CMX0P[2:0]		
Туре	, R		R/W		R		R	/W	
Rese	et 0	0	0	0	0	0		0	0
SFR A	ddress = 0x9	F; SFR Pa	ge = 0				•		
Bit	Name				Function				
7	Unused	Read = 0b	o; Write = don't c	are.					
6:4	CMX0N[2:0]	Compara	tor0 Negative Ir	nput MUX	Selection.				
			64-Pin Devices	s 48-Piı	n Devices	32-Pin Dev	ices	24-Pir	1 Devices
		000	P1.1		P1.1	—			—
		001	P1.3		P1.3	—		—	
		010 P1.5			_			—	
		011	P1.7		—	P2.0 (see note)		P2.0 (see note)	
		100-111	No input	No	o input	No input		No input	
			selected.	se	selected.		selected.		ected.
3	Unused	Read = $0t$; vvrite = don't c	are.					
2:0	CMX0P[2:0]	Compara	tor0 Positive In	put MUX	Selection.	•			
			64-Pin Devices	s 48-Pir	n Devices	32-Pin Devi	ices	24-Pir	1 Devices
		000	P1.0		P1.0	—			—
		001	P1.2		P1.2	—			—
		010	P1.4			—			—
		011	P1.6			(P1.6—see r	note)	(P1.6–	-see note)
		100-111	No input	No	o input	No inpu	t	No	o input
			selected.	se	lected.	selected		se	ected.
Note:	Note: On 32 and 24-pin devices, P2.0 can be used as the negative comparator input, for detecting low-level signals near the GND or VDD supply rails. The P1.6 setting for the positive input should be used in conjunction with the selection of P2.0 as the negative input. P1.6 should be configured for push-pull mode and driven to the desired supply rail. Although P1.6 is not connected to a device pin in these packages, it is still a valid signal internally.								



SFR Definition 15.2. CS0CF: Capacitive Sense Configuration

Bit	7	6	5	4	3	2	1	0
Name			CS0CM[2:0]			(CS0ACU[2:0]
Туре	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9E; SFR Page = 0

Bit	Name	Description
7	Unused	Read = 0b; Write = Don't care
6:4	CS0CM[2:0]	CS0 Start of Conversion Mode Select.
		000: Conversion initiated on every write of 1 to CS0BUSY.
		001: Conversion initiated on overflow of Timer 0.
		010: Conversion initiated on overflow of Timer 2.
		011: Conversion initiated on overflow of Timer 1.
		100: Conversion initiated on overflow of Timer 3.
		101: Reserved.
		110: Conversion initiated continuously after writing 1 to CS0BUSY.
		111: Auto-scan enabled, conversions initiated continuously after writing 1 to CS0BUSY.
3	Unused	Read = 0b; Write = Don't care
2:0	CS0ACU[2:0]	CS0 Accumulator Mode Select.
		000: Accumulate 1 sample.
		001: Accumulate 4 samples.
		010: Accumulate 8 samples.
		011: Accumulate 16 samples
		100: Accumulate 32 samples.
		101: Accumulate 64 samples.
		11x: Reserved.



18.2. Configuring the External Memory Interface

Configuring the External Memory Interface consists of five steps:

- 1. Configure the Output Modes of the associated port pins as either push-pull or open-drain (push-pull is most common).
- 2. Configure Port latches to "park" the EMIF pins in a dormant state (usually by setting them to logic 1).
- 3. Select Multiplexed mode or Non-multiplexed mode.
- 4. Select the memory mode (on-chip only, split mode without bank select, split mode with bank select, or off-chip only).
- 5. Set up timing to interface with off-chip memory or peripherals.

Each of these five steps is explained in detail in the following sections. The Port selection, Multiplexed mode selection, and Mode bits are located in the EMI0CF register shown in SFR Definition .

18.3. Port Configuration

The EMIF pinout is shown in Figure 18.2 on Page 127

The External Memory Interface claims the associated Port pins for memory operations ONLY during the execution of an off-chip MOVX instruction. Once the MOVX instruction has completed, control of the Port pins reverts to the Port latches for those pins. See Section "28. Port Input/Output" on page 180 for more information about Port operation and configuration. The Port latches should be explicitly configured to "park" the External Memory Interface pins in a dormant state, most commonly by setting them to a logic 1.

During the execution of the MOVX instruction, the External Memory Interface will explicitly disable the drivers on all Port pins that are acting as Inputs (Data[7:0] during a READ operation, for example). The Output mode of the Port pins (whether the pin is configured as Open-Drain or Push-Pull) is unaffected by the External Memory Interface operation, and remains controlled by the PnMDOUT registers. In most cases, the output modes of all EMIF pins should be configured for push-pull mode.



18.5.3. Split Mode with Bank Select

When EMI0CF[3:2] are set to 10, the XRAM memory map is split into two areas, on-chip space and offchip space.

- Effective addresses below the internal XRAM size boundary will access on-chip XRAM space.
- Effective addresses above the internal XRAM size boundary will access off-chip space.
- 8-bit MOVX operations use the contents of EMI0CN to determine whether the memory access is onchip or off-chip. The upper 8-bits of the Address Bus A[15:8] are determined by EMI0CN, and the lower 8-bits of the Address Bus A[7:0] are determined by R0 or R1. All 16-bits of the Address Bus A[15:0] are driven in "Bank Select" mode.
- 16-bit MOVX operations use the contents of DPTR to determine whether the memory access is on-chip or off-chip, and the full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

18.5.4. External Only

When EMI0CF[3:2] are set to 11, all MOVX operations are directed to off-chip space. On-chip XRAM is not visible to the CPU. This mode is useful for accessing off-chip memory located between 0x0000 and the internal XRAM size boundary.

- 8-bit MOVX operations ignore the contents of EMI0CN. The upper Address bits A[15:8] are not driven (identical behavior to an off-chip access in "Split Mode without Bank Select" described above). This allows the user to manipulate the upper address bits at will by setting the Port state directly. The lower 8-bits of the effective address A[7:0] are determined by the contents of R0 or R1.
- 16-bit MOVX operations use the contents of DPTR to determine the effective address A[15:0]. The full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

18.6. Timing

The timing parameters of the External Memory Interface can be configured to enable connection to devices having different setup and hold time requirements. The Address Setup time, Address Hold time, RD and WR strobe widths, and in multiplexed mode, the width of the ALE pulse are all programmable in units of SYSCLK periods through EMI0TC, shown in SFR Definition 18.3, and EMI0CF[1:0].

The timing for an off-chip MOVX instruction can be calculated by adding 4 SYSCLK cycles to the timing parameters defined by the EMI0TC register. Assuming non-multiplexed operation, the minimum execution time for an off-chip XRAM operation is 5 SYSCLK cycles (1 SYSCLK for RD or WR pulse + 4 SYSCLKs). For multiplexed operations, the Address Latch Enable signal will require a minimum of 2 additional SYSCLK cycles. Therefore, the minimum execution time for an off-chip XRAM operation in multiplexed mode is 7 SYSCLK cycles (2 for /ALE + 1 for RD or WR + 4). The programmable setup and hold times default to the maximum delay settings after a reset. Table 18.1 lists the ac parameters for the External Memory Interface, and Figure 18.4 through Figure 18.9 show the timing diagrams for the different External Memory Interface modes and MOVX operations.



21.3. INTO and INT1 External Interrupts

The INTO and INT1 external interrupt sources are configurable as active high or low, edge or level sensitive. The INOPL (INTO Polarity) and IN1PL (INT1 Polarity) bits in the IT01CF register select active high or active low; the IT0 and IT1 bits in TCON (Section "33.1. Timer 0 and Timer 1" on page 264) select level or edge sensitive. The table below lists the possible configurations.

IT0	IN0PL	INT0 Interrupt
1	0	Active low, edge sensitive
1	1	Active high, edge sensitive
0	0	Active low, level sensitive
0	1	Active high, level sensitive

IT1	IN1PL	INT1 Interrupt
1	0	Active low, edge sensitive
1	1	Active high, edge sensitive
0	0	Active low, level sensitive
0	1	Active high, level sensitive

INT0 and INT1 are assigned to Port pins as defined in the IT01CF register (see SFR Definition 21.7). Note that INT0 and INT0 Port pin assignments are independent of any Crossbar assignments. INT0 and INT1 will monitor their assigned Port pins without disturbing the peripheral that was assigned the Port pin via the Crossbar. To assign a Port pin only to INT0 and/or INT1, configure the Crossbar to skip the selected pin(s). This is accomplished by setting the associated bit in register XBR0 (see Section "28.3. Priority Crossbar Decoder" on page 185 for complete details on configuring the Crossbar).

IE0 (TCON.1) and IE1 (TCON.3) serve as the interrupt-pending flags for the INT0 and INT1 external interrupts, respectively. If an INT0 or INT1 external interrupt is configured as edge-sensitive, the corresponding interrupt-pending flag is automatically cleared by the hardware when the CPU vectors to the ISR. When configured as level sensitive, the interrupt-pending flag remains logic 1 while the input is active as defined by the corresponding polarity bit (IN0PL or IN1PL); the flag remains logic 0 while the input is inactive. The external interrupt source must hold the input active until the interrupt request is recognized. It must then deactivate the interrupt request before execution of the ISR completes or another interrupt request will be generated.



Rev. 1.0

SFR Definition 25.2. RSTSRC: Reset Source

Bit	7	6	5	4	3	2	1	0
Name		FERROR	CORSEF	SWRSF	WDTRSF	MCDRSF	PORSF	PINRSF
Туре	R	R	R/W	R/W	R	R/W	R/W	R
Reset	0	Varies						

SFR Address = 0xEF; SFR Page = All Pages

Bit	Name	Description	Write	Read
7	Unused	Unused.	Don't care.	0
6	FERROR	Flash Error Reset Flag.	N/A	Set to 1 if Flash read/write/erase error caused the last reset.
5	CORSEF	Comparator0 Reset Enable and Flag.	Writing a 1 enables Comparator0 as a reset source (active-low).	Set to 1 if Comparator0 caused the last reset.
4	SWRSF	Software Reset Force and Flag.	Writing a 1 forces a sys- tem reset.	Set to 1 if last reset was caused by a write to SWRSF.
3	WDTRSF	Watchdog Timer Reset Flag.	N/A	Set to 1 if Watchdog Timer overflow caused the last reset.
2	MCDRSF	Missing Clock Detector Enable and Flag.	Writing a 1 enables the Missing Clock Detector. The MCD triggers a reset if a missing clock condition is detected.	Set to 1 if Missing Clock Detector timeout caused the last reset.
1	PORSF	Power-On / V _{DD} Monitor Reset Flag, and V _{DD} monitor Reset Enable.	Writing a 1 enables the V_{DD} monitor as a reset source. Writing 1 to this bit before the V_{DD} monitor is enabled and stabilized may cause a system reset.	Set to 1 anytime a power- on or V _{DD} monitor reset occurs. When set to 1 all other RSTSRC flags are inde- terminate.
0	PINRSF	HW Pin Reset Flag.	N/A	Set to 1 if \overrightarrow{RST} pin caused the last reset.
Note:	Do not use	read-modify-write operations on this	s register	1



27.3.1. External Crystal Example

If a crystal or ceramic resonator is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 27.1, Option 1. The External Oscillator Frequency Control value (XFCN) should be chosen from the Crystal column of the table in SFR Definition 27.4 (OSCXCN register). For example, an 11.0592 MHz crystal requires an XFCN setting of 111b and a 32.768 kHz Watch Crystal requires an XFCN setting of 001b. After an external 32.768 kHz oscillator is stabilized, the XFCN setting can be switched to 000 to save power. It is recommended to enable the missing clock detector before switching the system clock to any external oscillator source.

When the crystal oscillator is first enabled, the oscillator amplitude detection circuit requires a settling time to achieve proper bias. Introducing a delay of 1 ms between enabling the oscillator and checking the XTLVLD bit will prevent a premature switch to the external oscillator as the system clock. Switching to the external oscillator before the crystal oscillator has stabilized can result in unpredictable behavior. The recommended procedure is:

- 1. Force XTAL1 and XTAL2 to a low state. This involves enabling the Crossbar and writing 0 to the port pins associated with XTAL1 and XTAL2.
- 2. Configure XTAL1 and XTAL2 as analog inputs.
- 3. Enable the external oscillator.
- 4. Wait at least 1 ms.
- 5. Poll for XTLVLD = 1.
- 6. If desired, enable the Missing Clock Detector.
- 7. Switch the system clock to the external oscillator.

Important Note on External Crystals: Crystal oscillator circuits are quite sensitive to PCB layout. The crystal should be placed as close as possible to the XTAL pins on the device. The traces should be as short as possible and shielded with ground plane from any other traces which could introduce noise or interference.

The capacitors shown in the external crystal configuration provide the load capacitance required by the crystal for correct oscillation. These capacitors are "in series" as seen by the crystal and "in parallel" with the stray capacitance of the XTAL1 and XTAL2 pins.

Note: The desired load capacitance depends upon the crystal and the manufacturer. Please refer to the crystal data sheet when completing these calculations.

For example, a tuning-fork crystal of 32.768 kHz with a recommended load capacitance of 12.5 pF should use the configuration shown in Figure 27.1, Option 1. The total value of the capacitors and the stray capacitance of the XTAL pins should equal 25 pF. With a stray capacitance of 3 pF per pin, the 22 pF capacitors yield an equivalent capacitance of 12.5 pF across the crystal, as shown in Figure 27.2.



SFR Definition 28.13. P1MDIN: Port 1 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDIN[7:0]							
Туре	R/W							
Reset	1*	1	1	1	1	1	1	1

SFR Address = 0xF2; SFR Page = F

Bit	Name	Function
7:0	P1MDIN[7:0]	Analog Configuration Bits for P1.7–P1.0 (respectively).
		Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled.
		0: Corresponding P1.n pin is configured for analog mode.
		1: Corresponding P1.n pin is not configured for analog mode.
Note:	On C8051F716 a on the C8051F71	nd C8051F717 devices, P1.7 will default to analog mode. If the P1MDIN register is written 6 and C8051F717 devices, P1.7 should always be configured as analog.

SFR Definition 28.14. P1MDOUT: Port 1 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDOUT[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA5; SFR Page = F

Bit	Name	Function
7:0	P1MDOUT[7:0]	Output Configuration Bits for P1.7–P1.0 (respectively).
		These bits are ignored if the corresponding bit in register P1MDIN is logic 0.
		0: Corresponding P1.n Output is open-drain.
		1: Corresponding P1.n Output is push-pull.



SFR Definition 28.35. P6MDIN: Port 6 Input Mode

Bit	7	6	5	4	3	2	1	0
Name				P6MDIN[5:0]				
Туре	R	R		R/W				
Reset	0	0	1	1	1	1	1	1

SFR Address = 0xF7; SFR Page = F

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care
5:0	P6MDIN[5:0]	Analog Configuration Bits for P6.5–P6.0 (respectively).
		Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled. 0: Corresponding P6.n pin is configured for analog mode. 1: Corresponding P6.n pin is not configured for analog mode.

SFR Definition 28.36. P6MDOUT: Port 6 Output Mode

Bit	7	6	5	4	3	2	1	0
Name			P6MDOUT[5:0]					
Туре	R	R		R/W				
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9C; SFR Page = F

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care
5:0	P6MDOUT[5:0]	Output Configuration Bits for P6.5–P6.0 (respectively).
		These bits are ignored if the corresponding bit in register P6MDIN is logic 0.
		0: Corresponding P6.n Output is open-drain.
		1: Corresponding P6.n Output is push-pull.



Bit	Set by Hardware When:	Cleared by Hardware When:
MASTED	 A START is generated. 	 A STOP is generated.
WASTER		 Arbitration is lost.
	 START is generated. 	A START is detected.
	 SMB0DAT is written before the start of an 	 Arbitration is lost.
TAMODE	SMBus frame.	 SMB0DAT is not written before the start of an SMBus frame.
STA	 A START followed by an address byte is received. 	Must be cleared by software.
	 A STOP is detected while addressed as a 	A pending STOP is generated.
STO	slave.	
	 Arbitration is lost due to a detected STOP. 	
	A byte has been received and an ACK	After each ACK cycle.
ACKRQ	response value is needed (only when	
	A repeated STAPT is detected as a	 Each time SLis cleared
	MASTER when STA is low (unwanted repeated START).	
ARBLOST	 SCL is sensed low while attempting to generate a STOP or repeated START condition. 	
	 SDA is sensed low while transmitting a 1 (excluding ACK bits). 	
ACK	 The incoming ACK value is low (ACKNOWLEDGE). 	 The incoming ACK value is high (NOT ACKNOWLEDGE).
	 A START has been generated. 	 Must be cleared by software.
	 Lost arbitration. 	·····
	A byte has been transmitted and an	
	ACK/NACK received.	
51	A byte has been received.	
	A START or repeated START followed by a	
	slave address + R/W has been received.	
	 A STOP has been received. 	

Table 30.3. Sources for Hardware Changes to SMB0CN

30.4.3. Hardware Slave Address Recognition

The SMBus hardware has the capability to automatically recognize incoming slave addresses and send an ACK without software intervention. Automatic slave address recognition is enabled by setting the EHACK bit in register SMB0ADM to 1. This will enable both automatic slave address recognition and automatic hardware ACK generation for received bytes (as a master or slave). More detail on automatic hardware ACK generation can be found in Section 30.4.2.2.

The registers used to define which address(es) are recognized by the hardware are the SMBus Slave Address register (SFR Definition 30.3) and the SMBus Slave Address Mask register (SFR Definition 30.4). A single address or range of addresses (including the General Call Address 0x00) can be specified using these two registers. The most-significant seven bits of the two registers are used to define which addresses will be ACKed. A 1 in bit positions of the slave address mask SLVM[6:0] enable a comparison between the received slave address and the hardware's slave address SLV[6:0] for those bits. A 0 in a bit of the slave address mask means that bit will be treated as a "don't care" for comparison purposes. In this



32. UART0

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates (details in Section "32.1. Enhanced Baud Rate Generation" on page 255). Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

UART0 has two associated SFRs: Serial Control Register 0 (SCON0) and Serial Data Buffer 0 (SBUF0). The single SBUF0 location provides access to both transmit and receive registers. Writes to SBUF0 always access the Transmit register. Reads of SBUF0 always access the buffered Receive register; it is not possible to read data from the Transmit register.

With UART0 interrupts enabled, an interrupt is generated each time a transmit is completed (TI0 is set in SCON0), or a data byte has been received (RI0 is set in SCON0). The UART0 interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine. They must be cleared manually by software, allowing software to determine the cause of the UART0 interrupt (transmit complete or receive complete).



Figure 32.1. UART0 Block Diagram



33.3. Timer 3

Timer 3 is a 16-bit timer formed by two 8-bit SFRs: TMR3L (low byte) and TMR3H (high byte). Timer 3 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T3SPLIT bit (TMR3CN.3) defines the Timer 3 operation mode.

Timer 3 may be clocked by the system clock, the system clock divided by 12, or the external oscillator source divided by 8. The external clock mode is ideal for real-time clock (RTC) functionality, where the internal high-frequency oscillator drives the system clock while Timer 3 is clocked by an external oscillator source. The external oscillator source divided by 8 is synchronized with the system clock when in all operating modes except suspend. When the internal oscillator is placed in suspend mode, The external clock/8 signal can directly drive the timer. This allows the use of an external clock to wake up the device from suspend mode. The timer will continue to run in suspend mode and count up. When the timer overflow occurs, the device will wake from suspend mode, and begin executing code again. The timer value may be set prior to entering suspend, to overflow in the desired amount of time (number of clocks) to wake the device. If a wake-up source other than the timer wakes the device from suspend mode, it may take up to three timer clocks before the timer registers can be read or written. During this time, the STSYNC bit in register OSCICN will be set to 1, to indicate that it is not safe to read or write the timer registers.

33.3.1. 16-bit Timer with Auto-Reload

When T3SPLIT (TMR3CN.3) is zero, Timer 3 operates as a 16-bit timer with auto-reload. Timer 3 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 3 reload registers (TMR3RLH and TMR3RLL) is loaded into the Timer 3 register as shown in Figure 33.7, and the Timer 3 High Byte Overflow Flag (TMR3CN.7) is set. If Timer 3 interrupts are enabled (if EIE1.7 is set), an interrupt will be generated on each Timer 3 overflow. Additionally, if Timer 3 interrupts are enabled and the TF3LEN bit is set (TMR3CN.5), an interrupt will be generated each time the lower 8 bits (TMR3L) overflow from 0xFF to 0x00.



Figure 33.7. Timer 3 16-Bit Mode Block Diagram



SFR Definition 33.13. TMR3CN: Timer 3 Control

Bit	7	6	5	4	3	2	1	0
Name	TF3H	TF3L	TF3LEN	TF3CEN	T3SPLIT	TR3		T3XCLK
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x91; SFR Page = 0

Bit	Name	Function
7	TF3H	Timer 3 High Byte Overflow Flag. Set by hardware when the Timer 3 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF3L	Timer 3 Low Byte Overflow Flag. Set by hardware when the Timer 3 low byte overflows from 0xFF to 0x00. TF3L will be set when the low byte overflows regardless of the Timer 3 mode. This bit is not automatically cleared by hardware.
5	TF3LEN	Timer 3 Low Byte Interrupt Enable. When set to 1, this bit enables Timer 3 Low Byte interrupts. If Timer 3 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 3 overflows.
4	TF3CEN	Timer 3 Comparator Capture Enable.
		When set to 1, this bit enables Timer 3 Comparator Capture Mode. If TF3CEN is set, on a rising edge of the Comparator0 output the current 16-bit timer value in TMR3H:TMR3L will be copied to TMR3RLH:TMR3RLL. If Timer 3 interrupts are also enabled, an interrupt will be generated on this event.
3	T3SPLIT	Timer 3 Split Mode Enable.When this bit is set, Timer 3 operates as two 8-bit timers with auto-reload.0: Timer 3 operates in 16-bit auto-reload mode.1: Timer 3 operates as two 8-bit auto-reload timers.
2	TR3	Timer 3 Run Control. Timer 3 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR3H only; TMR3L is always enabled in split mode.
1	Unused	Read = 0b; Write = Don't Care.
0	T3XCLK	 Timer 3 External Clock Select. This bit selects the external clock source for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 0: System clock divided by 12. 1: External clock divided by 8 (synchronized with SYSCLK when not in suspend).



34.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or fall-ing-edge caused the capture.



Figure 34.4. PCA Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.



34.3.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.



Figure 34.5. PCA Software Timer Mode Diagram

