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Application specific microcontrollers are engineered to

Details

Product Status	Obsolete
Applications	Trusted Platform Module (TPM)
Core Processor	AVR
Program Memory Type	EEPROM
Controller Series	-
RAM Size	-
Interface	I ² C
Number of I/O	4
Voltage - Supply	3.3V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at97sc3205t-g3m4620b

SUMMARY DATASHEET**Features**

- Compliant to the Trusted Computing Group (TCG) Trusted Platform Module (TPM) Version 1.2 Specification
- Single-chip Turnkey Solution
- Hardware Asymmetric Crypto Engine
- Atmel AVR[®] RISC Microprocessor
- Internal EEPROM Storage for RSA Keys
- 400kHz Fast Mode/100kHz Standard Mode I²C Operation
- Secure Hardware and Firmware Design and Device Layout
- FIPS-140-2 Module Certified Including the High-quality Random Number Generator (RNG), HMAC, AES, SHA, and RSA Engines
- NV Storage Space for 2066 bytes of User Defined Data
- 3.3V Supply Voltage
- 28-lead Thin TSSOP or 32-pad QFN Packages
- Offered in Commercial (0°C to 70°C) and Industrial (-40 to +85°C) Temperature Range

Description

Atmel AT97SC3205T is a fully integrated security module designed to be integrated into embedded systems. It implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM).

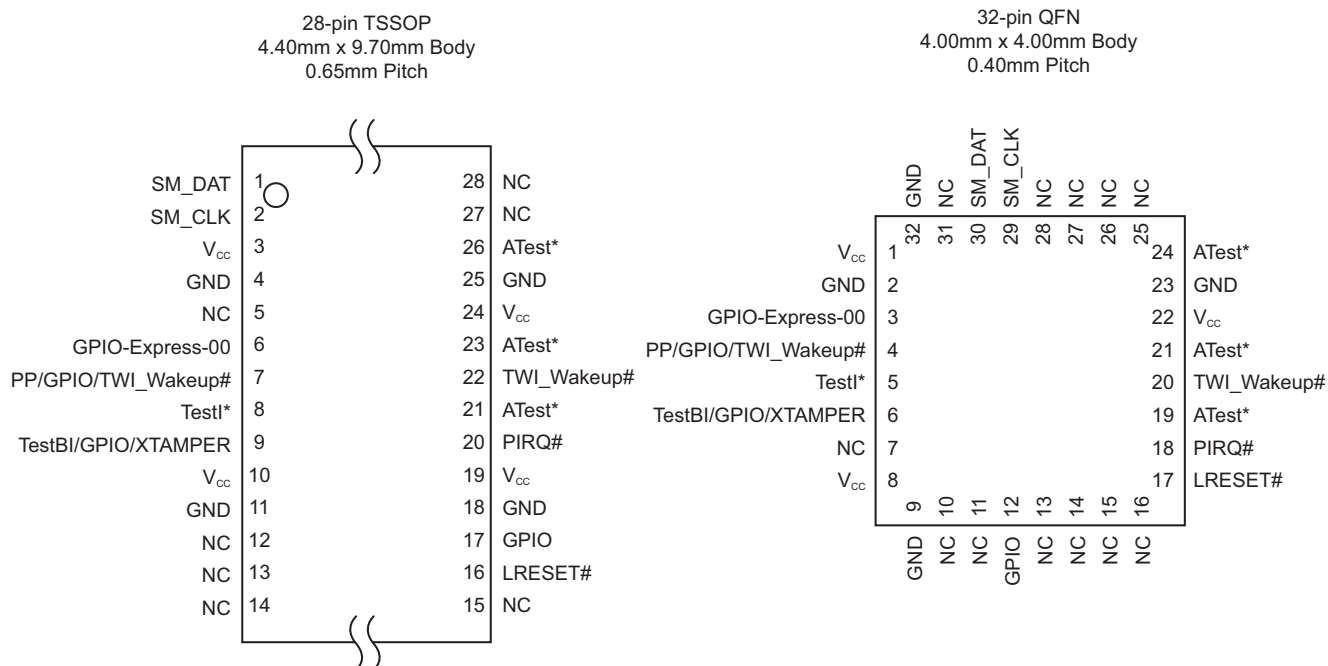
This is a summary document.
The complete document is
available under NDA. For more
information, please contact
your local Atmel sales office.

1. Pin Configuration and Pinouts

Table 1-1. Pin Configurations

Pin Name	Description
V _{CC}	3.3V Supply Voltage
GND	Ground
LRESET#	Reset Input Active Low
SM_DAT	Serial Data Input/Output
SM_CLK	Serial Clock Input
GPIO	General Purpose Input/Output
GPIO-Express-00	GPIO Assigned to TPM_NV_INDEX_GPIO_00
PP/GPIO	Hardware Physical Presence or GPIO Pin
TestI	Test Input (Disabled)
TestBI/GPIO/XTAMPER	Test Input (Disabled) / XTAMPER / GPIO Pin
TWI_Wakeup#	Low-Power Sleep Recovery (Active Low)
PIRQ#	SPI Interrupt Requests
ATest	Atmel Test Pin
NC	No Connect

Figure 1-1. Pinout Diagrams



Note: * Used for Atmel internal testing only. Tie to V_{CC} or GND directly or through a 4.7KΩ resistor.

Table 1-2. Pin Descriptions

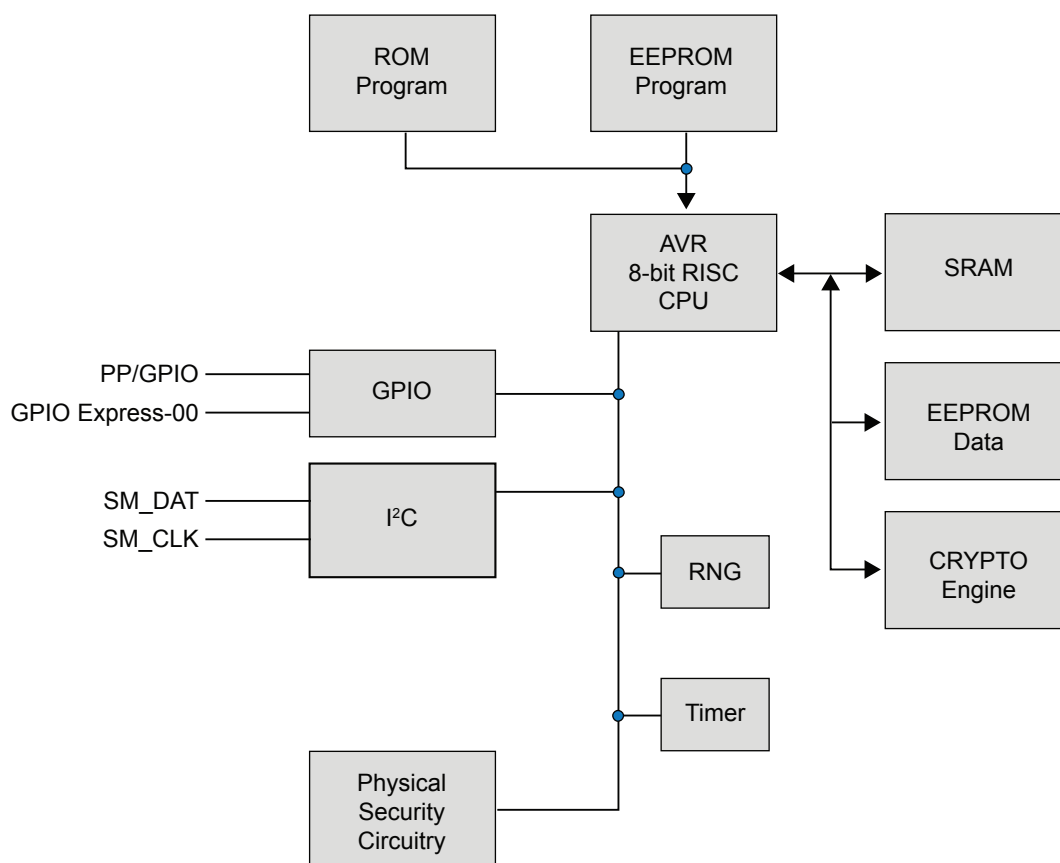
Pin	Description
V _{CC}	Power Supply, 3.3V. Care should be taken to prevent excessive noise. Effective decoupling of the V _{CC} inputs to the Atmel TPM is critical to assure consistently reliable operation over the lifetime of the system. The Atmel recommendation is for a decoupling bypass capacitor within the range of 2200pF to 4700pF to be placed as close as possible <5mm to each of the V _{CC} pins; located between each V _{CC} pin and the immediately adjacent GND pin. A 0.1μF decoupling bypass capacitor should be placed at the node in which these V _{CC} traces join as close as possible; <10mm to the TPM. In all cases, this bypass capacitor should be closer than the next closest component. All capacitors should be of high quality with dielectric ratings of X5R or X7R. A low-power state is automatically entered when the device is idle. No further action is required by the system to enter low-power mode.
GND	System Ground.
LRESET#	Reset Active-Low. Pulsing this signal low resets the internal state of the TPM and is equivalent to removal/restoration of power to the device. The required minimum reset pulse width is 2μs. On power-up, it is critical that Reset be kept active low until V _{CC} stabilizes.
SM_DAT	I²C Data Input/Output. This pin serves as the Data Input/Output for the TPM. If one attempts to communicate over the interface at close to the rated speed of 400kHz, the size of the pull-ups on SM_DAT can be critical. A known value that functions properly at 400kHz is 800Ω on the SM_DAT line. One may experiment with different pull-up values and/or reduce the clock rate if desired.
SM_CLK	I²C Clock Input. This pin serves as the Serial Clock Input to the TPM. If one attempts to communicate over the interface at close to the rated speed of 400kHz, the size of the pull-ups on SM_CLK can be critical. A known value that functions properly at 400kHz is 1.5KΩ on the SM_CLK line. One may experiment with different pull-up values and/or reduce the clock rate if desired. The TPM communication stability is increased the closer to a 50% duty cycle on the SM_CLK signal that can be provided. Although this becomes more critical at the rated speed of 400kHz, improvements from a 50% duty cycle can result at lower speeds as well.
GPIO	General Purpose Input/Output. If not used, tie high or low.
GPIO-Express-00	General Purpose Input/Output. Internal pull-up resistor. This pin is mapped to NV Index TPM_NV_INDEX_GPIO_00 and serves as the GPIO-Express-00. Default TPM configuration: GPIO Input. GPIO-Express-00 also serves as the XOR chain Output during I/O test mode. Since GPIO-Express-00 has an internal pull-up it should be left floating if unused.
PP/GPIO	General Purpose Input/Output. Internal pull-down resistor. This pin is an indicator for hardware physical presence; active high. Default TPM configuration: GPIO input. Since PP/GPIO has an internal pull-down, it should be left floating if unused.
TestI	Test Input. TestI manufacturing test input disabled after manufacturing. Tie TestI to ground directly or through a 4.7KΩ resistor.
TestBI/GPIO/XTAMPER	Test Input. The Atmel TPM does not support legacy addressing via the optional BADD implementation of this pin. The TestBI pin serves as the XTAMPER pin or an additional GPIO pin, active high. (See the application note, "Atmel Specific TPM Commands Reference Guide," for details on XTAMPER implementation). If unused, this pin should be tied to ground directly or through a 4.7KΩ resistor.
TWI_Wakeup#	Low-Power Sleep Recovery. These two pins serve as the mechanism to allow the TPM to recover from its low-power sleep state after receiving the Atmel Specific command TPM_DeepSleep (See Atmel TPM Specific Commands document for further details). These pins must both be pulsed active low in order to recover from the low-power sleep state. If unused, pin 7 can be left floating or tied to GND either directly or through a 4.7KΩ resistor. Pin 22 should be tied to GND or V _{CC} either directly or through a 4.7KΩ resistor.

Table 1-2. Pin Descriptions (Continued)

Pin	Description
PIRQ#	SPI Interrupt Requests. If unused, this pin should be tied to ground directly or through a 4.7K Ω resistor.
ATest	<p>Atmel Test Pins.</p> <p>Only utilized during manufacturing test.</p> <p>To optimize power savings and improve noise immunity, these ATest pins should be biased to V_{CC} or GND as follows:</p> <p>TSSOP Pin 21 / QFN Pin 19</p> <p>TSSOP Pin 23 / QFN Pin 21</p> <p>TSSOP Pin 26 / QFN Pin 24</p>
NC	<p>No Connect Pins.</p> <p>The AT97SC3205T TSSOP package has additional pins which are no connects and can be tied to GND, V_{CC}, or left floating at the customers discretion:</p> <p>NC – TSSOP Pin 5</p> <p>NC – TSSOP Pin 12</p> <p>NC – TSSOP Pin 13</p> <p>NC – TSSOP Pin 14</p> <p>NC – TSSOP Pin 15</p> <p>NC – TSSOP Pin 27</p> <p>NC – TSSOP Pin 28</p> <p>The AT97SC3205T QFN package has additional pins which are no connects and can be tied to GND, V_{CC}, or left floating at the customers discretion:</p> <p>NC – QFN Pin 7</p> <p>NC – QFN Pin 10</p> <p>NC – QFN Pin 11</p> <p>NC – QFN Pin 13</p> <p>NC – QFN Pin 14</p> <p>NC – QFN Pin 15</p> <p>NC – QFN Pin 16</p> <p>NC – QFN Pin 25</p> <p>NC – QFN Pin 26</p> <p>NC – QFN Pin 27</p> <p>NC – QFN Pin 28</p> <p>NC – QFN Pin 31</p>

Note: 1. The substrate center pad for the 32-pin QFN is directly tied to GND internally; therefore, this pad can either be left floating or tied to GND.

2. Block Diagram



Communication to and from the TPM occurs through a 400kHz Fast mode/100kHz Standard mode. The TPM includes a hardware random number generator, including a FIPS certified Pseudo Random Number Generator which is used for key generation and TCG protocol functions. The RNG is also available to the system to generate random numbers which may be needed during normal operation.

The device uses a dynamic internal memory management scheme to store multiple RSA keys. Other than the standard TCG commands (TPM_FlushSpecific, TPM_Loadkey2), no system intervention is required to manage this internal key cache.

Full documentation for TCG primitives can be found in the TCG TPM Main Specification, Parts 1 – 3, on the TCG Web site located at www.trustedcomputinggroup.org. This specification includes only mechanical, electrical and I²C protocol information.

3. Ordering Information

Ordering Code	Package		Operational Range
AT97SC3205T ⁽¹⁾	28X1 (28-pin Thin TSSOP)	Lead-free, RoHS	Commercial (0°C to 70°C)
AT97SC3205T ⁽¹⁾	32M3 (32-pin Very Thin QFN)		Industrial (-40°C to 85°C)

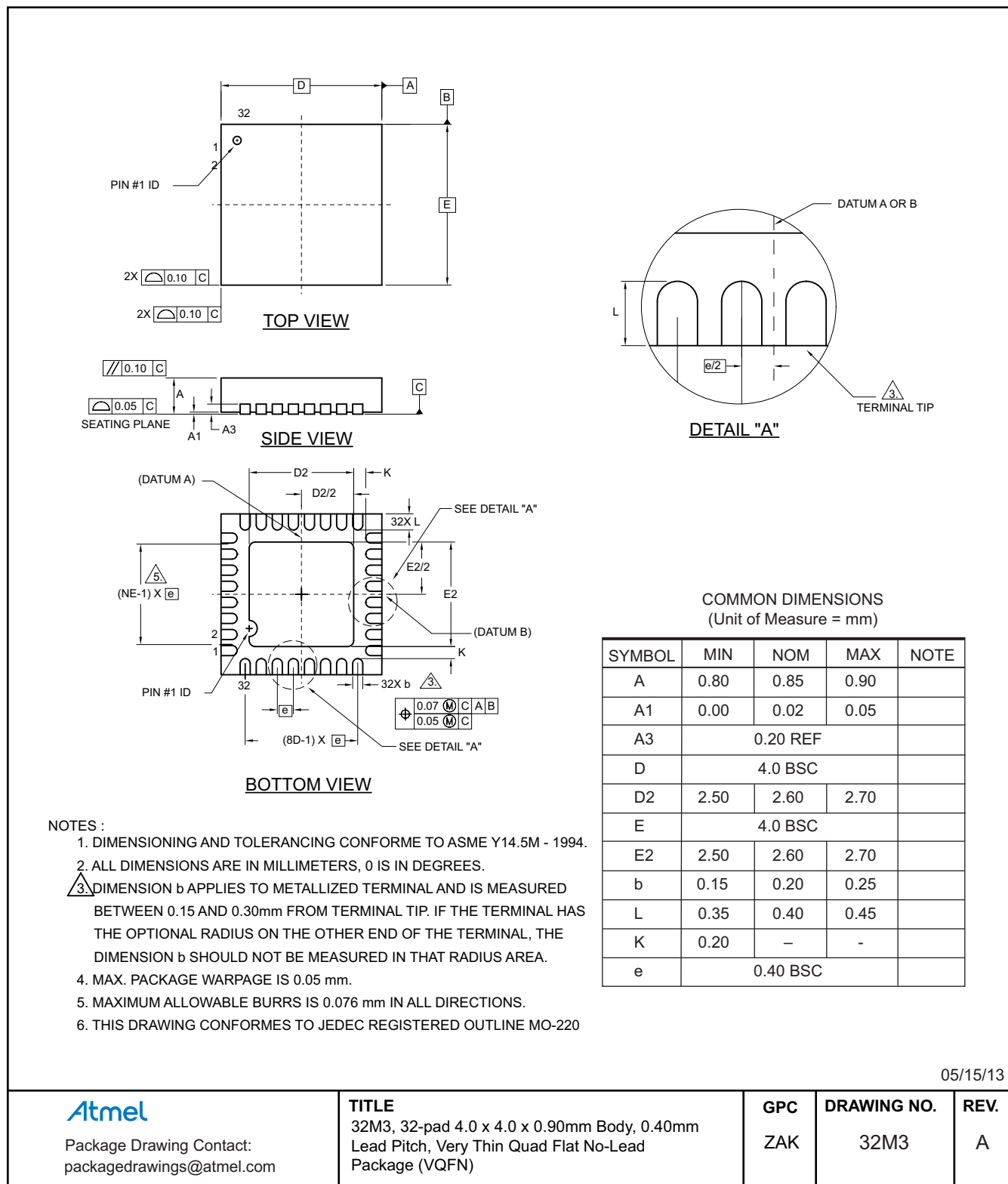
Note: 1. Please see the AT97SC3205T datasheet addendum for the complete catalog number ordering code.

4. Package Drawings

4.1 28X1 — 28-lead Thin TSSOP



4.2 32M3 — 32-pad QFN



5. Revision History

Doc. Rev.	Date	Comments
8883AS	02/2014	Initial summary document release.

