Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	49
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atxmega256a3b-au

1. Ordering Information

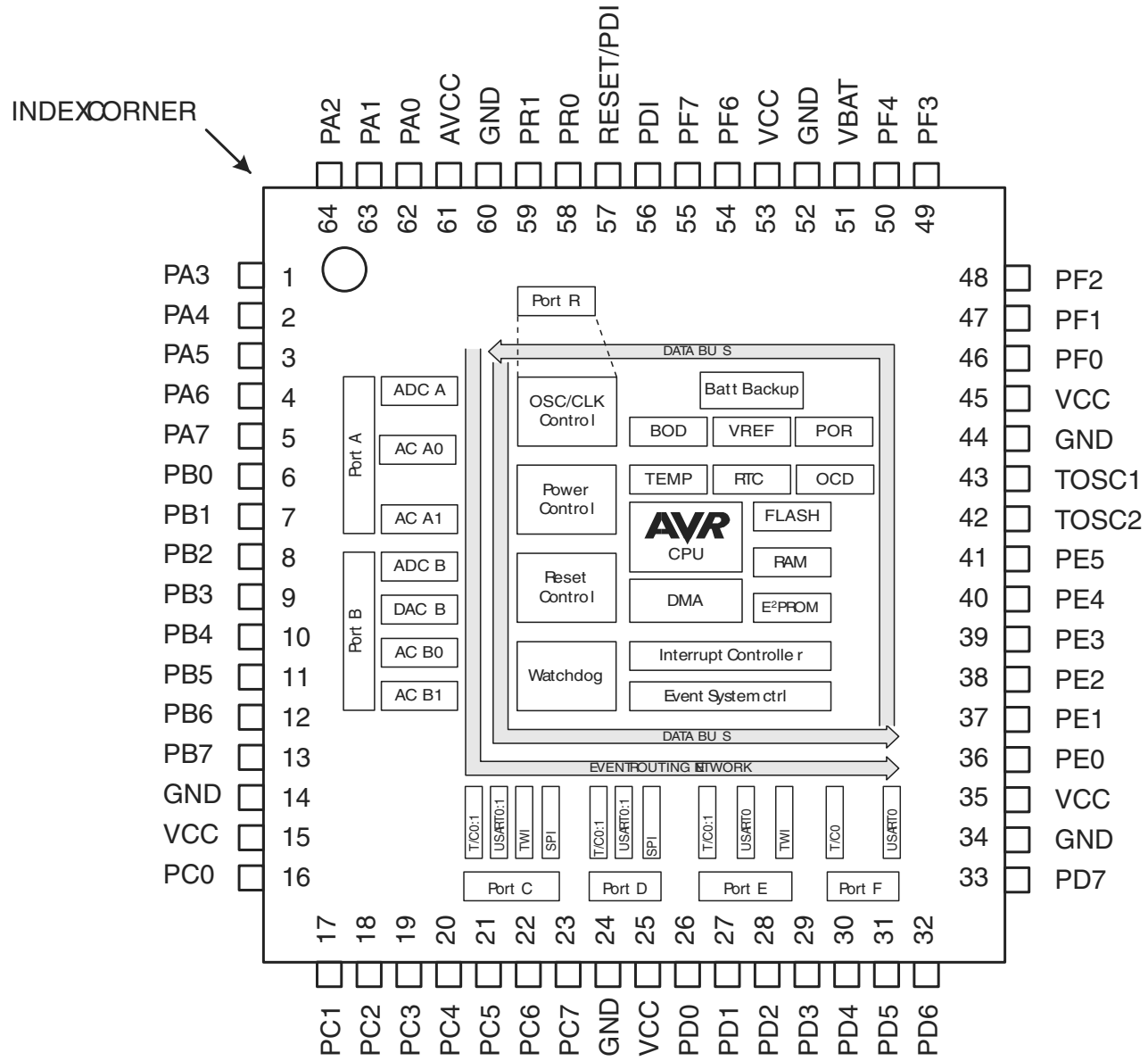
Ordering Code	Flash	E^2	SRAM	Speed (MHz)	Power Supply	Package[1][2][3]	Temp
ATxmega256A3B-AU	256 KB + 8 KB	4 KB	16 KB	32	1.6 - 3.6V	64A	-40°C - 85°C
ATxmega256A3B-MH	256 KB + 8 KB	4 KB	16 KB	32	1.6 - 3.6V	64M2	

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see ”Electrical Characteristics” on page 64.

Package Type	
64A	64-Lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)
64M2	64-Pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 7.65 mm Exposed Pad, Micro Lead Frame Package (MLF)

2. Pinout/Block Diagram

Figure 2-1. Block diagram and pinout.



Notes: 1. For full details on pinout and pin functions refer to ”Pinout and Pin Functions” on page 50.
2. The large center pad underneath the QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

6. AVR CPU

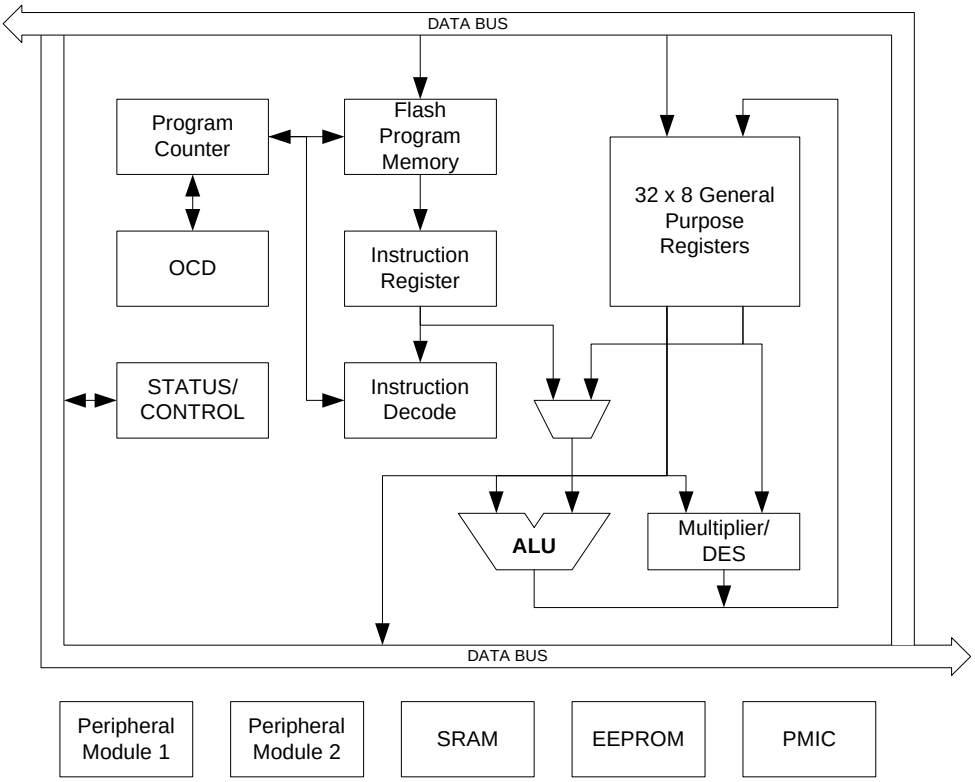
6.1 Features

- **8/16-bit high performance AVR RISC Architecture**
  - **138 instructions**
  - **Hardware multiplier**
- **32x8-bit registers directly connected to the ALU**
- **Stack in SRAM**
- **Stack Pointer accessible in I/O memory space**
- **Direct addressing of up to 16M Bytes of program and data memory**
- **True 16/24-bit access to 16/24-bit I/O registers**
- **Support for 8-, 16- and 32-bit Arithmetic**
- **Configuration Change Protection of system critical features**

6.2 Overview

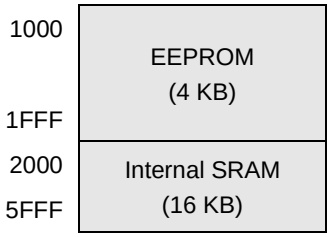
The XMEGA A3B uses the 8/16-bit AVR CPU. The main function of the CPU is program execution. The CPU must therefore be able to access memories, perform calculations and control peripherals. Interrupt handling is described in a separate section. Figure 6-1 on page 7 shows the CPU block diagram.

Figure 6-1. CPU block diagram



The AVR uses a Harvard architecture - with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This

Figure 7-2. Data Memory Map (Hexadecimal address)



7.4.1 I/O Memory

All peripherals and modules are addressable through I/O memory locations in the data memory space. All I/O memory locations can be accessed by the Load (LD/LDS/LDD) and Store (ST/STS/STD) instructions, transferring data between the 32 general purpose registers in the CPU and the I/O Memory.

The IN and OUT instructions can address I/O memory locations in the range 0x00 - 0x3F directly.

I/O registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. The value of single bits can be checked by using the SBIS and SBIC instructions on these registers.

The I/O memory address for all peripherals and modules in XMEGA A3B is shown in the ”Peripheral Module Address Map” on page 57.

7.4.2 SRAM Data Memory

The XMEGA A3B devices have internal SRAM memory for data storage.

7.4.3 EEPROM Data Memory

The XMEGA A3B devices have internal EEPROM memory for non-volatile data storage. It is addressable either in a separate data space or it can be memory mapped into the normal data memory space. The EEPROM memory supports both byte and page access.

8. DMAC - Direct Memory Access Controller

8.1 Features

- **Allows High-speed data transfer**
  - **From memory to peripheral**
  - **From memory to memory**
  - **From peripheral to memory**
  - **From peripheral to peripheral**
- **4 Channels**
- **From 1 byte and up to 16M bytes transfers in a single transaction**
- **Multiple addressing modes for source and destination address**
  - **Increment**
  - **Decrement**
  - **Static**
- **1, 2, 4, or 8 byte Burst Transfers**
- **Programmable priority between channels**

8.2 Overview

The XMEGA A3B has a Direct Memory Access (DMA) Controller to move data between memories and peripherals in the data space. The DMA controller uses the same data bus as the CPU to transfer data.

It has 4 channels that can be configured independently. Each DMA channel can perform data transfers in blocks of configurable size from 1 to 64K bytes. A repeat counter can be used to repeat each block transfer for single transactions up to 16M bytes. Each DMA channel can be configured to access the source and destination memory address with incrementing, decrementing or static addressing. The addressing is independent for source and destination address. When the transaction is complete the original source and destination address can automatically be reloaded to be ready for the next transaction.

The DMAC can access all the peripherals through their I/O memory registers, and the DMA may be used for automatic transfer of data to/from communication modules, as well as automatic data retrieval from ADC conversions, data transfer to DAC conversions, or data transfer to or from port pins. A wide range of transfer triggers are available from the peripherals, Event System and software. Each DMA channel has different transfer triggers.

To allow for continuous transfers, two channels can be interlinked so that the second takes over the transfer when the first is finished and vice versa.

The DMA controller can read from memory mapped EEPROM, but it cannot write to the EEPROM or access the Flash.

12. System Control and Reset

12.1 Features

- **Multiple reset sources for safe operation and device reset**
  - **Power-On Reset**
  - **External Reset**
  - **Watchdog Reset**
    The Watchdog Timer runs from separate, dedicated oscillator
  - **Brown-Out Reset**
    Accurate, programmable Brown-Out levels
  - **JTAG Reset**
  - **PDI reset**
  - **Software reset**
- **Asynchronous reset**
  - **No running clock in the device is required for reset**
- **Reset status register**

12.2 Resetting the AVR

During reset, all I/O registers are set to their initial values. The SRAM content is not reset. Application execution starts from the Reset Vector. The instruction placed at the Reset Vector should be an Absolute Jump (JMP) instruction to the reset handling routine. By default the Reset Vector address is the lowest Flash program memory address, ‘0’, but it is possible to move the Reset Vector to the first address in the Boot Section.

The I/O ports of the AVR are immediately tri-stated when a reset source goes active.

The reset functionality is asynchronous, so no running clock is required to reset the device.

After the device is reset, the reset source can be determined by the application by reading the Reset Status Register.

12.3 Reset Sources

12.3.1 Power-On Reset

The MCU is reset when the supply voltage VCC is below the Power-on Reset threshold voltage.

12.3.2 External Reset

The MCU is reset when a low level is present on the RESET pin.

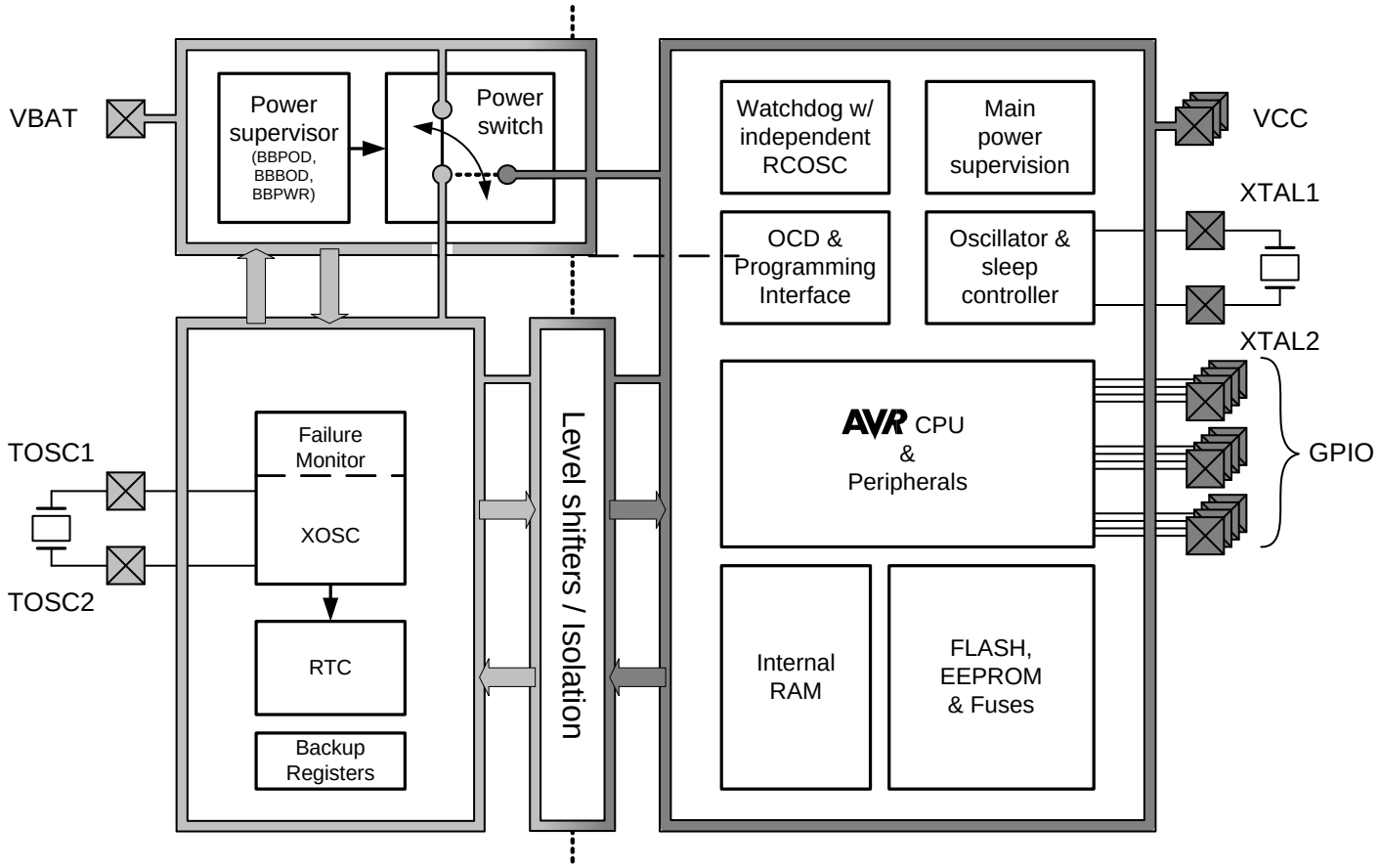
12.3.3 Watchdog Reset

The MCU is reset when the Watchdog Timer period expires and the Watchdog Reset is enabled. The Watchdog Timer runs from a dedicated oscillator independent of the System Clock. For more details see ”WDT - Watchdog Timer” on page 23.

12.3.4 Brown-Out Reset

The MCU is reset when the supply voltage VCC is below the Brown-Out Reset threshold voltage and the Brown-out Detector is enabled. The Brown-out threshold voltage is programmable.

Figure 13-1. Battery Backup Module and its power domain implementation



14. PMIC - Programmable Multi-level Interrupt Controller

14.1 Features

- **Separate interrupt vector for each interrupt**
- **Short, predictable interrupt response time**
- **Programmable Multi-level Interrupt Controller**
  - **3 programmable interrupt levels**
  - **Selectable priority scheme within low level interrupts (round-robin or fixed)**
  - **Non-Maskable Interrupts (NMI)**
- **Interrupt vectors can be moved to the start of the Boot Section**

14.2 Overview

XMEGA A3B has a Programmable Multi-level Interrupt Controller (PMIC). All peripherals can define three different priority levels for interrupts; high, medium or low. Medium level interrupts may interrupt low level interrupt service routines. High level interrupts may interrupt both low- and medium level interrupt service routines. Low level interrupts have an optional round robin scheme to make sure all interrupts are serviced within a certain amount of time.

The built in oscillator failure detection mechanism can issue a Non-Maskable Interrupt (NMI).

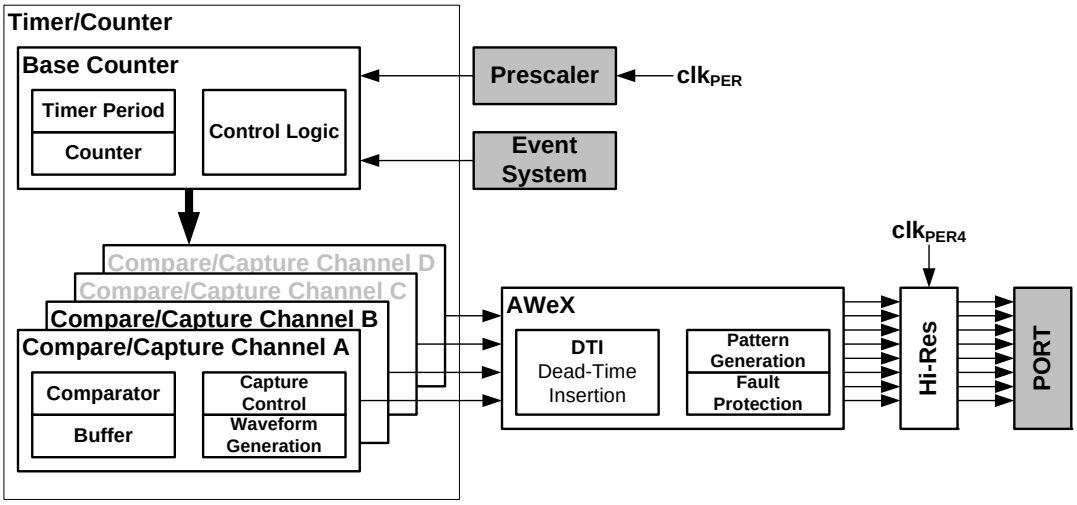
14.3 Interrupt vectors

When an interrupt is serviced, the program counter will jump to the interrupt vector address. The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the XMEGA A3B devices are shown in Table 14-1. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA A manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 14-1. The program address is the word address.

Table 14-1. Reset and Interrupt Vectors

Program Address (Base Address)	Source	Interrupt Description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal Oscillator Failure Interrupt vector (NMI)
0x004	PORTC_INT_base	Port C Interrupt base
0x008	PORTR_INT_base	Port R Interrupt base
0x00C	DMA_INT_base	DMA Controller Interrupt base
0x014	RTC32_INT_base	32-bit Real Time Counter Interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C Interrupt base
0x01C	TCC0_INT_base	Timer/Counter 0 on port C Interrupt base
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x038	USARTC1_INT_base	USART 1 on port C Interrupt base
0x03E	AES_INT_vect	AES Interrupt vector

Figure 16-1. Overview of a Timer/Counter and closely related peripherals



The Hi-Resolution Extension can be enabled to increase the waveform generation resolution by 2 bits (4x). This is available for all Timer/Counters. See ”Hi-Res - High Resolution Extension” on page 35 for more details.

The Advanced Waveform Extension can be enabled to provide extra and more advanced features for the Timer/Counter. This are only available for Timer/Counter 0. See ”AWEX - Advanced Waveform Extension” on page 34 for more details.

27. AC - Analog Comparator

27.1 Features

- **Four Analog Comparators**
- **Selectable Power vs. Speed**
- **Selectable hysteresis**
  - **0, 20 mV, 50 mV**
- **Analog Comparator output available on pin**
- **Flexible Input Selection**
  - **All pins on the port**
  - **Output from the DAC**
  - **Bandgap reference voltage.**
  - **Voltage scaler that can perform a 64-level scaling of the internal VCC voltage.**
- **Interrupt and event generation on**
  - **Rising edge**
  - **Falling edge**
  - **Toggle**
- **Window function interrupt and event generation on**
  - **Signal above window**
  - **Signal inside window**
  - **Signal below window**

27.2 Overview

XMEGA A3B features four Analog Comparators (AC). An Analog Comparator compares two voltages, and the output indicates which input is largest. The Analog Comparator may be configured to give interrupt requests and/or events upon several different combinations of input change.

Both hysteresis and propagation delays may be adjusted in order to find the optimal operation for each application.

A wide range of input selection is available, both external pins and several internal signals can be used.

The Analog Comparators are always grouped in pairs (AC0 and AC1) on each analog port. They have identical behavior but separate control registers.

Optionally, the state of the comparator is directly available on a pin.

PORTA and PORTB each have one AC pair. Notations are ACA and ACB, respectively.

29. Program and Debug Interfaces

29.1 Features

- **PDI - Program and Debug Interface (Atmel proprietary 2-pin interface)**
- **JTAG Interface (IEEE std. 1149.1 compliant)**
- **Boundary-scan capabilities according to the IEEE Std. 1149.1 (JTAG)**
- **Access to the OCD system**
- **Programming of Flash, EEPROM, Fuses and Lock Bits**

29.2 Overview

The programming and debug facilities are accessed through the JTAG and PDI physical interfaces. The PDI physical uses one dedicated pin together with the Reset pin, and no general purpose pins are used. JTAG uses four general purpose pins on PORTB.

29.3 JTAG interface

The JTAG physical layer handles the basic low-level serial communication over four I/O lines named TMS, TCK, TDI, and TDO. It complies to the IEEE Std. 1149.1 for test access port and boundary scan.

29.4 PDI - Program and Debug Interface

The PDI is an Atmel proprietary protocol for communication between the microcontroller and Atmel's development tools.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CALL	k	call Subroutine	PC ← k	None	3 / 4[1]
RET		Subroutine Return	PC ← STACK	None	4 / 5[1]
RETI		Interrupt Return	PC ← STACK	I	4 / 5[1]
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data Transfer Instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2[1][2]
LD	Rd, X	Load Indirect	Rd ← (X)	None	1[1][2]
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1[1][2]
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2[1][2]
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1[1][2]
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1[1][2]

Mnemonics	Operands	Description	Operation	Flags	#Clocks
LD	Rd, -Y	Load Indirect and Pre-Decrement	Y ← Y - 1 Rd ← (Y)	None	2[1][2]
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2[1][2]
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	1[1][2]
LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	1[1][2]
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z - 1, Rd ← (Z)	None	2[1][2]
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2[1][2]
STS	k, Rr	Store Direct to Data Space	(k) ← Rd	None	2[1]
ST	X, Rr	Store Indirect	(X) ← Rr	None	1[1]
ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	1[1]
ST	-X, Rr	Store Indirect and Pre-Decrement	X ← X - 1, (X) ← Rr	None	2[1]
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	1[1]
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	1[1]
ST	-Y, Rr	Store Indirect and Pre-Decrement	Y ← Y - 1, (Y) ← Rr	None	2[1]
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2[1]
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	1[1]
ST	Z+, Rr	Store Indirect and Post-Increment	(Z) ← Rr Z ← Z + 1	None	1[1]
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z - 1	None	2[1]
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2[1]
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	Rd ← (Z), Z ← Z + 1	None	3
ELPM		Extended Load Program Memory	R0 ← (RAMPZ:Z)	None	3
ELPM	Rd, Z	Extended Load Program Memory	Rd ← (RAMPZ:Z)	None	3
ELPM	Rd, Z+	Extended Load Program Memory and Post-Increment	Rd ← (RAMPZ:Z), Z ← Z + 1	None	3
SPM		Store Program Memory	(RAMPZ:Z) ← R1:R0	None	-
SPM	Z+	Store Program Memory and Post-Increment by 2	(RAMPZ:Z) ← R1:R0, Z ← Z + 2	None	-
IN	Rd, A	In From I/O Location	Rd ← I/O(A)	None	1
OUT	A, Rr	Out To I/O Location	I/O(A) ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	1[1]
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2[1]
Bit and Bit-test Instructions					
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0, C ← Rd(7)	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0, C ← Rd(0)	Z,C,N,V	1

Table 34-1. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Units
Module current consumption(2)						
I_{CC}	RC32M			460		µA
	RC32M w/DFLL	Internal 32.768 kHz oscillator as DFLL source		594		
	RC2M			101		
	RC2M w/DFLL	Internal 32.768 kHz oscillator as DFLL source		134		
	RC32K			27		
	PLL	Multiplication factor = 10x		202		
	Watchdog normal mode			1		
	BOD Continuous mode			128		
	BOD Sampled mode			1		
	Internal 1.00 V ref			80		
	Temperature reference			74		
	RTC with int. 32 kHz RC as source	No prescaling		27		
	RTC with ULP as source	No prescaling		1		
	ADC	250 kS/s - Int. 1V Ref		2.9		mA
	DAC Normal Mode	1000 kS/s, Single channel, Int. 1V Ref		1.8		
	DAC Low-Power Mode	1000 KS/s, Single channel, Int. 1V Ref		0.95		
	DAC S/H Normal Mode	Int.1.1V Ref, Refresh 16CLK		2.9		
	DAC Low-Power Mode S/H	Int.1.1V Ref, Refresh 16CLK		1.1		
	AC High-speed			195		µA
	AC Low-power			103		
	USART	Rx and Tx enabled, 9600 BAUD		5.4		
	DMA			128		
	Timer/Counter	Prescaler DIV1		20		
	AES			223		
	Flash/EEPROM Programming	Vcc = 2V		25		mA
		Vcc = 3V		33		

Note: 1. All Power Reduction Registers set. Typical numbers measured at T = 25°C if nothing else is specified.

2. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1 MHz External clock with no prescaling, T = 25°C.

34.11 POR Characteristics

Table 34-12. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{POT-}	POR threshold voltage falling Vcc			1		V
V_{POT+}	POR threshold voltage rising Vcc			1.45		

34.12 Reset Characteristics

Table 34-13. Reset Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Minimum reset pulse width			90		ns
	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.42*V_{CC}		

34.13 Oscillator Characteristics

Table 34-14. Internal 32.768 kHz Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Accuracy	T = 85°C, V_{CC} = 3V, After production calibration	-0.5		0.5	%

Table 34-15. Internal 2 MHz Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Accuracy	T = 85°C, V_{CC} = 3V, After production calibration	-1.5		1.5	%
	DFLL Calibration step size	T = 25°C, V_{CC} = 3V		0.15		

Table 34-16. Internal 32 MHz Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Accuracy	T = 85°C, V_{CC} = 3V, After production calibration	-1.5		1.5	%
	DFLL Calibration stepsize	T = 25°C, V_{CC} = 3V		0.2		

Table 34-17. Internal 32 kHz, ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Output frequency 32 kHz ULP OSC	T = 85°C, V_{CC} = 3.0V		26		kHz

35.3 Power-down Supply Current

Figure 35-15. Power-down Supply Current vs. Temperature

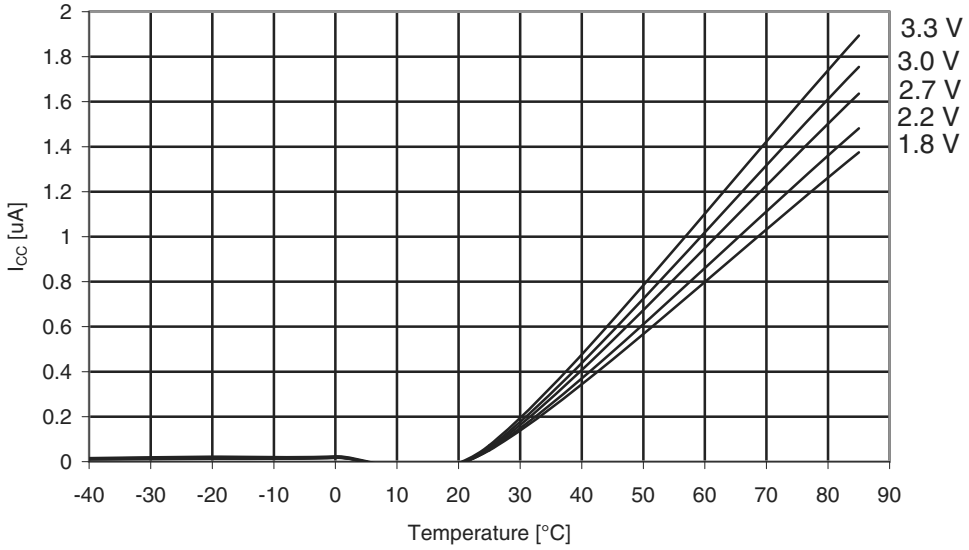
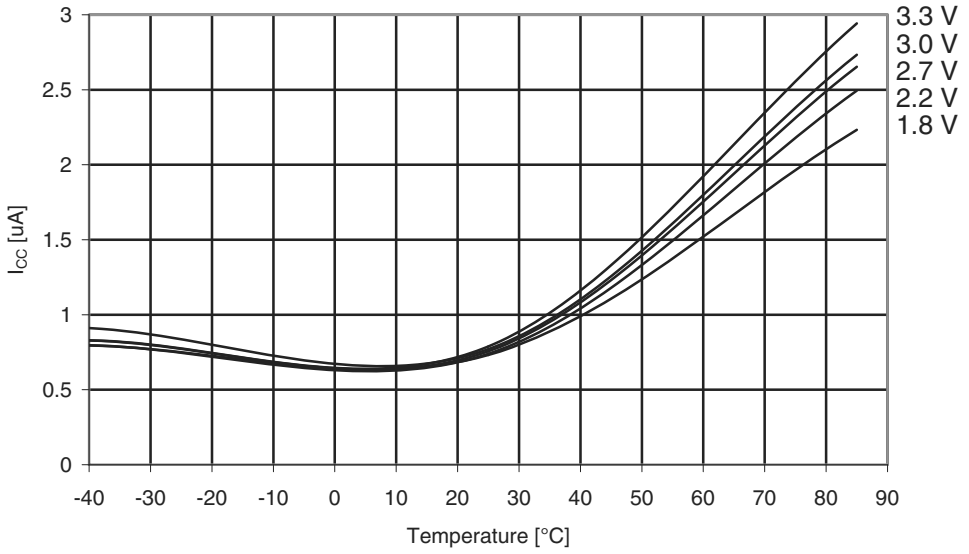


Figure 35-16. Power-down Supply Current vs. Temperature

With WDT and sampled BOD enabled.



35.7 Pin Thresholds and Hysteresis

Figure 35-27. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - I/O Pin Read as "1"

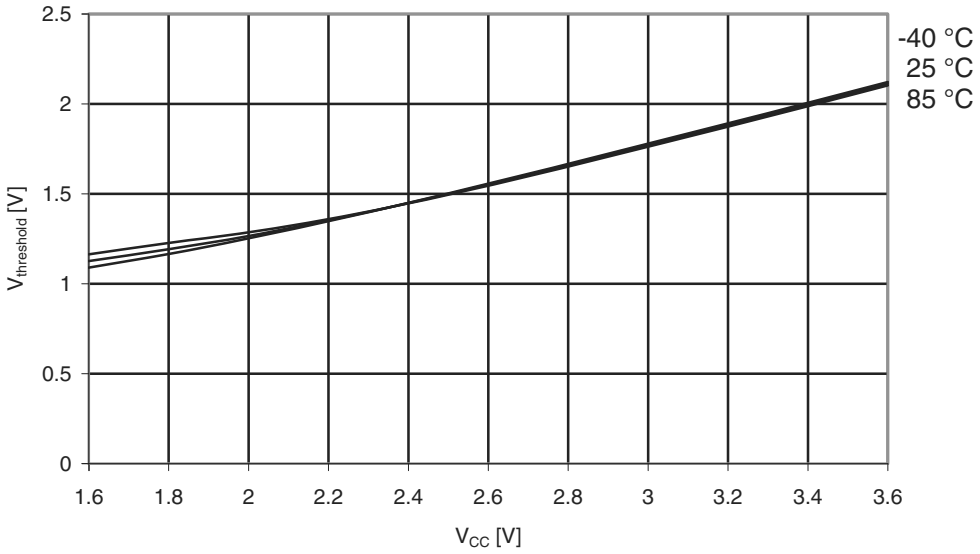


Figure 35-28. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} - I/O Pin Read as "0"

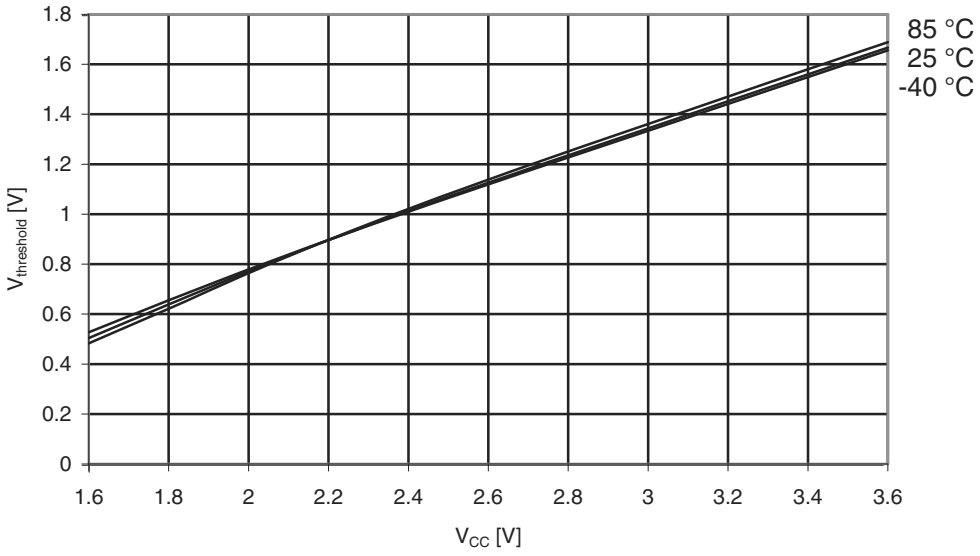
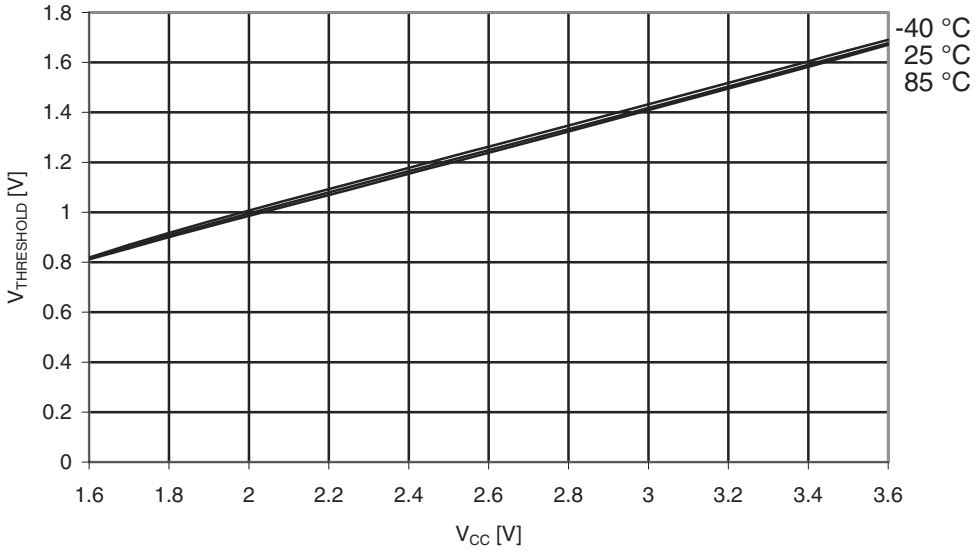


Figure 35-31. Reset Input Threshold Voltage vs. V_{CC}

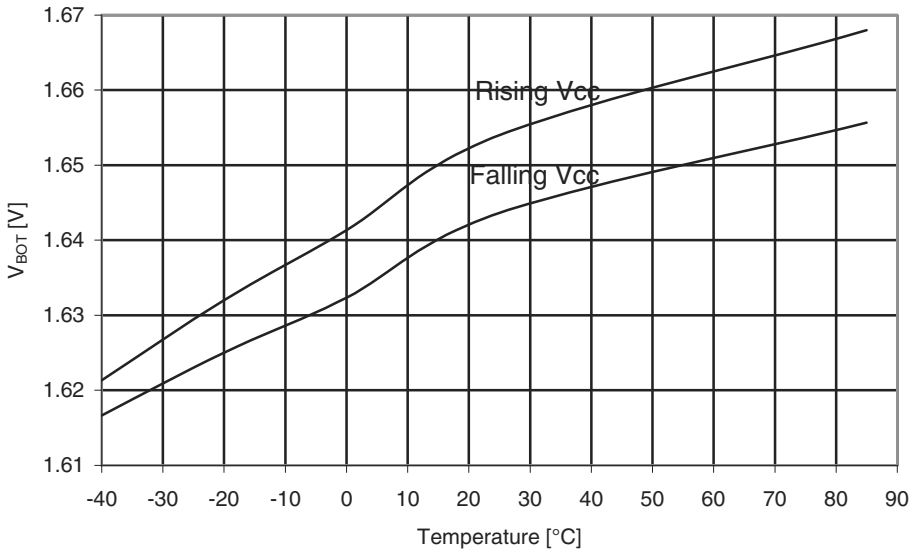
V_{IL} - I/O Pin Read as "0"



35.8 Bod Thresholds

Figure 35-32. BOD Thresholds vs. Temperature

BOD Level = 1.6V



12. DAC refresh may be blocked in S/H mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workaround

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

13. Conversion lost on DAC channel B in event triggered mode

If during dual channel operation channel 1 is set in auto trigged conversion mode, channel 1 conversions are occasionally lost. This means that not all data-values written to the Channel 1 data register are converted.

Problem fix/Workaround

Keep the DAC conversion interval in the range 000-001 (1 and 3 CLK), and limit the Peripheral clock frequency so the conversion internal never is shorter than 1.5 µs.

14. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

15. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

16. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

17. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

6. Updated ”Alternate Pin Functions” on page 52.
7. Updated ”Operating voltage and frequency” on page 66 by replacing SYS to CPU.
8. Replaced Table 34-3 on page 67.
9. Updated Table 34-3 on page 67, Endurance and Data Retention.
11. Updated ”PAD Characteristics” on page 70. Input hysteresis is in V and not in mV.
12. Added new table ”Maximum load capacitance (CL) and ESR recommendation for 32.768 kHz Crystal” on page 72.
13. Added new table ”Device wake-up time from sleep” on page 72.
14. Updated Table 34-20 on page 73.
15. Changed Internal Oscillator Speed to ”Oscillators and Wake-up Time” on page 90.
16. Added characterization for PDI speed in Figure 35-42 on page 94.
17. Updated ”Errata” on page 95.

37.5 8116F - 09/09

1. Updated ”DC Characteristics” on page 64.
2. Added ”Flash and EEPROM Memory Characteristics” on page 67.
3. Added ”” on page 72.
4. Upddated ”Errata” on page 95.

37.6 8116E - 06/09

1. Updated ”Electrical Characteristics” on page 64.
2. Added ”Typical Characteristics” on page 74.
3. Updated ”Errata” on page 95.

37.7 8116D - 04/09

1. Updated ”Ordering Information” on page 2.
2. Editorial updates.

37.8 8116C - 02/09

1. Added ”Errata” on page 95 for ATxmega256A3B rev B.