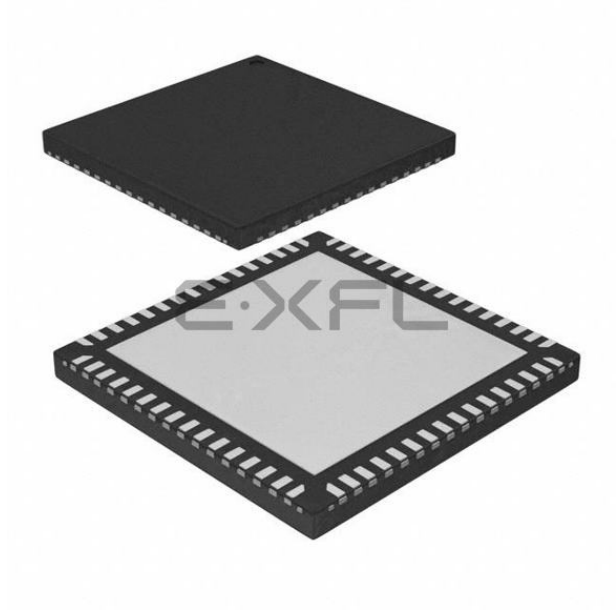

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	49
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3b-mh

1. Ordering Information

Ordering Code	Flash	E^2	SRAM	Speed (MHz)	Power Supply	Package[1][2][3]	Temp
ATxmega256A3B-AU	256 KB + 8 KB	4 KB	16 KB	32	1.6 - 3.6V	64A	-40°C - 85°C
ATxmega256A3B-MH	256 KB + 8 KB	4 KB	16 KB	32	1.6 - 3.6V	64M2	

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see ”Electrical Characteristics” on page 64.

Package Type	
64A	64-Lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)
64M2	64-Pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 7.65 mm Exposed Pad, Micro Lead Frame Package (MLF)

4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4.1 Recommended reading

- XMEGA A Manual
- XMEGA Application Notes

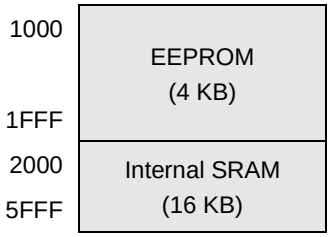
This device data sheet only contains part specific information and a short description of each peripheral and module. The XMEGA A Manual describes the modules and peripherals in depth. The XMEGA application notes contain example code and show applied use of the modules and peripherals.

The XMEGA A Manual and Application Notes are available from http://www.atmel.com/avr.

5. Disclaimer

For devices that are not available yet, typical values contained in this datasheet are based on simulations and characterization of other AVR XMEGA microcontrollers manufactured on the same process technology. Min. and Max values will be available after the device is characterized.

Figure 7-2. Data Memory Map (Hexadecimal address)



7.4.1 I/O Memory

All peripherals and modules are addressable through I/O memory locations in the data memory space. All I/O memory locations can be accessed by the Load (LD/LDS/LDD) and Store (ST/STS/STD) instructions, transferring data between the 32 general purpose registers in the CPU and the I/O Memory.

The IN and OUT instructions can address I/O memory locations in the range 0x00 - 0x3F directly.

I/O registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. The value of single bits can be checked by using the SBIS and SBIC instructions on these registers.

The I/O memory address for all peripherals and modules in XMEGA A3B is shown in the ”Peripheral Module Address Map” on page 57.

7.4.2 SRAM Data Memory

The XMEGA A3B devices have internal SRAM memory for data storage.

7.4.3 EEPROM Data Memory

The XMEGA A3B devices have internal EEPROM memory for non-volatile data storage. It is addressable either in a separate data space or it can be memory mapped into the normal data memory space. The EEPROM memory supports both byte and page access.

9. Event System

9.1 Features

- **Inter-peripheral communication and signalling with minimum latency**
- **CPU and DMA independent operation**
- **8 Event Channels allows for up to 8 signals to be routed at the same time**
- **Events can be generated by**
  - **Timer/Counters (TCxn)**
  - **Real Time Counter (RTC)**
  - **Analog to Digital Converters (ADCx)**
  - **Analog Comparators (ACx)**
  - **Ports (PORTx)**
  - **System Clock (Clk_{SYS})**
  - **Software (CPU)**
- **Events can be used by**
  - **Timer/Counters (TCxn)**
  - **Analog to Digital Converters (ADCx)**
  - **Digital to Analog Converters (DACx)**
  - **Ports (PORTx)**
  - **DMA Controller (DMAC)**
  - **IR Communication Module (IRCOM)**
- **The same event can be used by multiple peripherals for synchronized timing**
- **Advanced Features**
  - **Manual Event Generation from software (CPU)**
  - **Quadrature Decoding**
  - **Digital Filtering**
- **Functions in Active and Idle mode**

9.2 Overview

The Event System is a set of features for inter-peripheral communication. It enables the possibility for a change of state in one peripheral to automatically trigger actions in one or more peripherals. What changes in a peripheral that will trigger actions in other peripherals are configurable by software. It is a simple, but powerful system as it allows for autonomous control of peripherals without any use of interrupts, CPU or DMA resources.

The indication of a change in a peripheral is referred to as an event, and is usually the same as the interrupt conditions for that peripheral. Events are passed between peripherals using a dedicated routing network called the Event Routing Network. Figure 9-1 on page 16 shows a basic block diagram of the Event System with the Event Routing Network and the peripherals to which it is connected. This highly flexible system can be used for simple routing of signals, pin functions or for sequencing of events.

The maximum latency is two CPU clock cycles from when an event is generated in one peripheral, until the actions are triggered in one or more other peripherals.

The Event System is functional in both Active and Idle modes.

10. System Clock and Clock options

10.1 Features

- **Fast start-up time**
- **Safe run-time clock switching**
- **Internal Oscillators:**
  - **32 MHz run-time calibrated RC oscillator**
  - **2 MHz run-time calibrated RC oscillator**
  - **32.768 kHz calibrated RC oscillator**
  - **32 kHz Ultra Low Power (ULP) oscillator**
- **External clock options**
  - **0.4 - 16 MHz Crystal Oscillator**
  - **32.768 kHz Crystal Oscillator**
  - **External clock**
- **PLL with internal and external clock options with 2 to 31x multiplication**
- **Clock Prescalers with 2 to 2048x division**
- **Fast peripheral clock running at 2 and 4 times the CPU clock speed**
- **Automatic Run-Time Calibration of internal oscillators**
- **Crystal Oscillator failure detection**

10.2 Overview

XMEGA A3B has an advanced clock system, supporting a large number of clock sources. It incorporates both integrated oscillators, external crystal oscillators and resonators. A high frequency Phase Locked Loop (PLL) and clock prescalers can be controlled from software to generate a wide range of clock frequencies from the clock source input.

It is possible to switch between clock sources from software during run-time. After reset the device will always start up running from the 2 Mhz internal oscillator.

A calibration feature is available, and can be used for automatic run-time calibration of the internal 2 MHz and 32 MHz oscillators. This reduce frequency drift over voltage and temperature.

A Crystal Oscillator Failure Monitor can be enabled to issue a Non-Maskable Interrupt and switch to internal oscillator if the external oscillator fails. Figure 10-1 on page 18 shows the principal clock system in XMEGA A3B.

13. Battery Backup System

13.1 Features

- **Battery Backup voltage supply from dedicated V_{BAT} power pin for:**
  - **One Ultra Low-power 32-bit Real Time Counter**
  - **One 32.768 kHz crystal oscillator with failure detection monitor**
  - **Two Backup Registers**
- **Typical power consumption of 500nA with Real Time Counter (RTC) running**
- **Automatic switching from main power to battery backup power at:**
  - **Brown-Out Detection (BOD) reset**
- **Automatic switching from battery backup power to main power:**
  - **Device reset after Brown-Out Reset (BOR) is released**
  - **Device reset after Power-On Reset (POR) and BOR is released**

13.2 Overview

The AVR XMEGA family is already running in an ultra low leakage process with power-save current consumption below 2 µA with RTC, BOD and watchdog enabled. Still, for some applications where time keeping is important, the system would have one main battery or power source used for day to day tasks, and one backup battery power for the time keeping functionality. The Battery Backup System includes functionality that enable automatic power switching between main power and a battery backup power. Figure 13-1 on page 25 shows an overview of the system.

The Battery Backup Module support connection of a backup battery to the dedicated V_{BAT} power pin. This will ensure power to the 32-bit Real Time Counter, a 32.768 kHz crystal oscillator with failure detection monitor and two backup registers, when the main battery or power source is unavailable.

Upon main power loss the device will automatically detect this and the Battery Backup Module will switch to be powered from the V_{BAT} pin. After main power has been restored and both main POR and BOR are released, the Battery Backup Module will automatically switch back to be powered from main power again.

The 32-bit Real Time Counter (RTC) must be clocked from the 1 Hz output of a 32.768 kHz crystal oscillator connected between the TOSC1 and TOSC2 pins when running from V_{BAT}. For more details on the 32-bit RTC refer to the “RTC32 - 32-bit Real Time Counter” section in the XMEGA A Manual.

16. T/C - 16-bit Timer/Counter with PWM

16.1 Features

- **Seven 16-bit Timer/Counters**
  - **Four Timer/Counters of type 0**
  - **Three Timer/Counters of type 1**
- **Four Compare or Capture (CC) Channels in Timer/Counter 0**
- **Two Compare or Capture (CC) Channels in Timer/Counter 1**
- **Double Buffered Timer Period Setting**
- **Double Buffered Compare or Capture Channels**
- **Waveform Generation:**
  - **Single Slope Pulse Width Modulation**
  - **Dual Slope Pulse Width Modulation**
  - **Frequency Generation**
- **Input Capture:**
  - **Input Capture with Noise Cancelling**
  - **Frequency capture**
  - **Pulse width capture**
  - **32-bit input capture**
- **Event Counter with Direction Control**
- **Timer Overflow and Timer Error Interrupts and Events**
- **One Compare Match or Capture Interrupt and Event per CC Channel**
- **Supports DMA Operation**
- **Hi-Resolution Extension (Hi-Res)**
- **Advanced Waveform Extension (AWEX)**

16.2 Overview

XMEGA A3B has seven Timer/Counters, four Timer/Counter 0 and three Timer/Counter 1. The difference between them is that Timer/Counter 0 has four Compare/Capture channels, while Timer/Counter 1 has two Compare/Capture channels.

The Timer/Counters (T/C) are 16-bit and can count any clock, event or external input in the microcontroller. A programmable prescaler is available to get a useful T/C resolution. Updates of Timer and Compare registers are double buffered to ensure glitch free operation. Single slope PWM, dual slope PWM and frequency generation waveforms can be generated using the Compare Channels.

Through the Event System, any input pin or event in the microcontroller can be used to trigger input capture, hence no dedicated pins are required for this. The input capture has a noise canceller to avoid incorrect capture of the T/C, and can be used to do frequency and pulse width measurements.

A wide range of interrupt or event sources are available, including T/C Overflow, Compare match and Capture for each Compare/Capture channel in the T/C.

PORTC, PORTD and PORTE each has one Timer/Counter 0 and one Timer/Counter1. PORTF has one Timer/Counter 0. Notation of these are TCC0 (Time/Counter C0), TCC1, TCD0, TCD1, TCE0, TCE1 and TCF0, respectively.

18. Hi-Res - High Resolution Extension

18.1 Features

- **Increases Waveform Generator resolution by 2-bits (4x)**
- **Supports Frequency, single- and dual-slope PWM operation**
- **Supports the AWEX when this is enabled and used for the same Timer/Counter**

18.2 Overview

The Hi-Resolution (Hi-Res) Extension is able to increase the resolution of the waveform generation output by a factor of 4. When enabled for a Timer/Counter, the Fast Peripheral clock running at four times the CPU clock speed will be as input to the Timer/Counter.

The High Resolution Extension can also be used when an AWEX is enabled and used with a Timer/Counter.

XMEGA A3B devices have four Hi-Res Extensions that each can be enabled for each Timer/Counters pair on PORTC, PORTD, PORTE and PORTF. The notation of these are HIRESC, HIRESD, HIRESE and HIRESF, respectively.

30. Pinout and Pin Functions

The pinout of XMEGA A3B is shown in ”Pinout/Block Diagram” on page 3. In addition to general I/O functionality, each pin may have several functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the alternate pin functions can be used at time.

30.1 Alternate Pin Function Description

The tables below shows the notation for all pin functions available and describes its function.

30.1.1 Operation/Power Supply

VCC	Digital supply voltage
AVCC	Analog supply voltage
VBAT	Battery Backup Module supply voltage
GND	Ground

30.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

30.1.3 Analog functions

ACn	Analog Comparator input pin n
AC0OUT	Analog Comparator 0 Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
AREF	Analog Reference input pin

30.1.4 Timer/Counter and AWEX functions

OCnx	Output Compare Channel x for Timer/Counter n
$\overline{\text{OCnx}}$	Inverted Output Compare Channel x for Timer/Counter n
OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

30.1.5 Communication functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled

Table 30-3. Port C - Alternate functions (Continued)

PORT C	PIN #	INTERRUPT	TCC0	AWEXC	TCC1	USARTC0	USARTC1	SPIC	TWIC	CLOCKOUT	EVENTOUT
PC5	21	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PC6	22	SYNC		OC0DLS			RXD1	MISO			
PC7	23	SYNC		OC0DHS			TXD1	SCK		CLKOUT	EVOUT

Table 30-4. Port D - Alternate functions

PORT D	PIN #	INTERRUPT	TCD0	TCD1	USARTD0	USARTD1	SPID	CLOCKOUT	EVENTOUT
GND	24								
VCC	25								
PD0	26	SYNC	OC0A						
PD1	27	SYNC	OC0B		XCK0				
PD2	28	SYNC/ASYNC	OC0C		RXD0				
PD3	29	SYNC	OC0D		TXD0				
PD4	30	SYNC		OC1A			$\overline{SS}$		
PD5	31	SYNC		OC1B		XCK1	MOSI		
PD6	32	SYNC				RXD1	MISO		
PD7	33	SYNC				TXD1	SCK	CLKOUT	EVOUT

Table 30-5. Port E - Alternate functions

PORT E	PIN #	INTERRUPT	TCE0	TCE1	USARTE0	TWIE
GND	34					
VCC	35					
PE0	36	SYNC	OC0A			SDA/SDA_IN
PE1	37	SYNC	OC0B		XCK0	SCL/SCL_IN
PE2	38	SYNC/ASYNC	OC0C		RXD0	SDA_OUT
PE3	39	SYNC	OC0D		TXD0	SCL_OUT
PE4	40	SYNC		OC1A		
PE5	41	SYNC		OC1B		
TOSC2	42					
TOSC1	43					

Table 30-6. Port F - Alternate functions

PORT F	PIN #	INTERRUPT	TCF0	USARTF0
GND	44			
VCC	45			
PF0	46	SYNC	OC0A	
PF1	47	SYNC	OC0B	XCK0
PF2	48	SYNC/ASYNC	OC0C	RXD0
PF3	49	SYNC	OC0D	TXD0
PF4	50	SYNC	OC0A	
VBAT	51			

Bit Number	Signal Name	Module
125	PJ7.Bidir	PORT J
124	PJ7.Control	
123	PJ6.Bidir	
122	PJ6.Control	
121	PJ5.Bidir	
120	PJ5.Control	
119	PJ4.Bidir	
118	PJ4.Control	
117	PJ3.Bidir	
116	PJ3.Control	
115	PJ2.Bidir	
114	PJ2.Control	
113	PJ1.Bidir	
112	PJ1.Control	
111	PJ0.Bidir	
110	PJ0.Control	
109	PH7.Bidir	PORT H
108	PH7.Control	
107	PH6.Bidir	
106	PH6.Control	
105	PH5.Bidir	
104	PH5.Control	
103	PH4.Bidir	
102	PH4.Control	
101	PH3.Bidir	
100	PH3.Control	
99	PH2.Bidir	
98	PH2.Control	
97	PH1.Bidir	
96	PH1.Control	
95	PH0.Bidir	
94	PH0.Control	
93	PF7.Bidir	PORT F
92	PF7.Control	
91	PF6.Bidir	
90	PF6.Control	
89	PF5.Bidir	
88	PF5.Control	
87	PF4.Bidir	
86	PF4.Control	
85	PF3.Bidir	
84	PF3.Control	
83	PF2.Bidir	
82	PF2.Control	
81	PF1.Bidir	
80	PF1.Control	
79	PF0.Bidir	
78	PF0.Control	
77	PE7.Bidir	PORT E
76	PE7.Control	
75	PE6.Bidir	
74	PE6.Control	
73	PE5.Bidir	
72	PE5.Control	
71	PE4.Bidir	
70	PE4.Control	
69	PE3.Bidir	
68	PE3.Control	
67	PE2.Bidir	
66	PE2.Control	
65	PE1.Bidir	
64	PE1.Control	
63	PE0.Bidir	
62	PE0.Control	

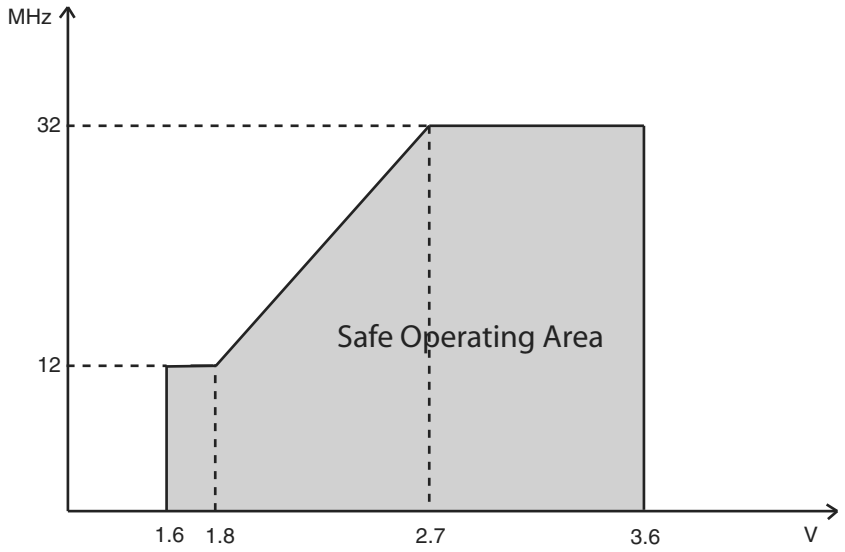
34.3 Operating Voltage and Frequency

Table 34-2. Operating voltage and frequency

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency of the XMEGA A3B devices is depending on V_{CC}. As shown in Figure 34-1 on page 66 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 34-1. Maximum Frequency vs. Vcc



34.5 ADC Characteristics

Table 34-5. ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
RES	Resolution	Programmable: 8/12	8	12	12	Bits
INL	Integral Non-Linearity	500 ksps		±2		LSB
DNL	Differential Non-Linearity	500 ksps		< ±1		
	Gain Error			< ±10		mV
	Offset Error			< ±2		
ADC_{clk}	ADC Clock frequency	Max is 1/4 of Peripheral Clock			2000	kHz
	Conversion rate				2000	ksps
	Conversion time (propagation delay)	(RES+2)/2+GAIN RES = 8 or 12, GAIN = 0 or 1	5	7	8	ADC_{clk} cycles
	Sampling Time	1/2 ADC_{clk} cycle	0.25			uS
	Conversion range		0		VREF	V
AVCC	Analog Supply Voltage		V_{cc}-0.3		V_{cc}+0.3	
VREF	Reference voltage		1.0		V_{cc}-0.6V	
	Input bandwidth					kHz
INT1V	Internal 1.00V reference			1.00		V
INTVCC	Internal V_{CC}/1.6			V_{CC}/1.6		
SCALEDVCC	Scaled internal V_{CC}/10 input			V_{CC}/10		
R_{AREF}	Reference input resistance			> 10		MΩ
	Start-up time			12	24	ADC_{clk} cycles
	Internal input sampling speed	Temp. sensor, V_{CC}/10, Bandgap			100	ksps

Table 34-6. ADC Gain Stage Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
	Gain error	1 to 64 gain			< ±1		%
	Offset error				< ±1		mV
Vrms	Noise level at input	64x gain	VREF = Int. 1V		0.12		
			VREF = Ext. 2V		0.06		
	Clock rate	Same as ADC				1000	kHz

34.14 VBAT and Battery Backup Characteristics

Table 34-20. VBAT and Battery Backup Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Vbat supply voltage range		Vbbbod		3.6	V
	Vbat power-on slope rate	Monotonic rising	0.2			V/ms
	Vcc Power-loss slope range	Monotonic falling			0.1	V/ms
	main BOD threshold voltage		1.8			V
	BBBOD required voltage change			1.2		V
	BBBOD threshold voltage			1.7	2.1	V
	BBBOD detection speed			1	2	s
	Battery Backup System current consumption	RTC enabled from 1 Hz TOSC with XOSC Failure Monitor enabled		530		nA
		RTC enabled from 1 Hz Hi ESR mode and XOSC Failure Monitor enabled		680		nA
	VBAT pin leackage	Powering Battery Backup module from Vcc			50	nA
	Delay from setting XOSCFDEN to setting XOSCEN		200			µS
	Missing crystal oscillator cycles before XOSCFAIL is set			32		cycles

35.7 Pin Thresholds and Hysteresis

Figure 35-27. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - I/O Pin Read as "1"

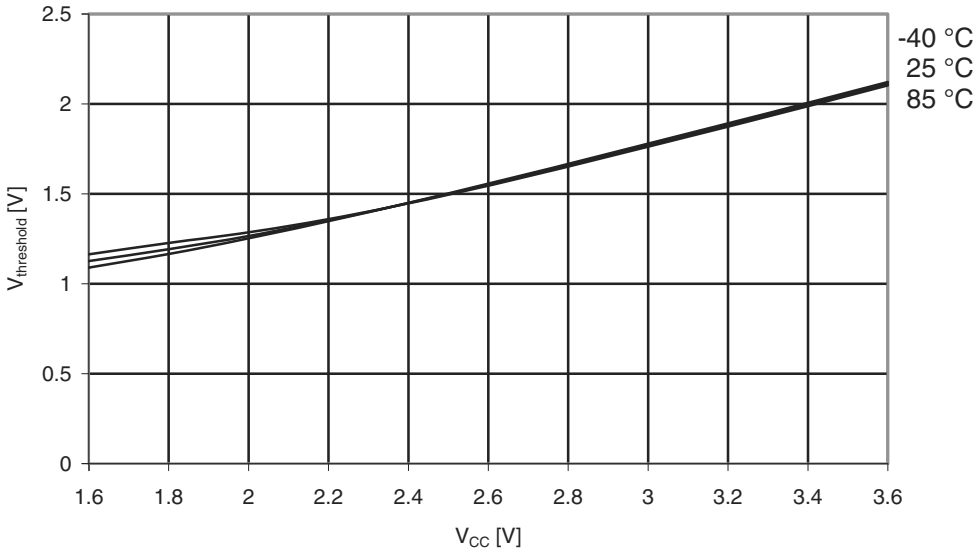
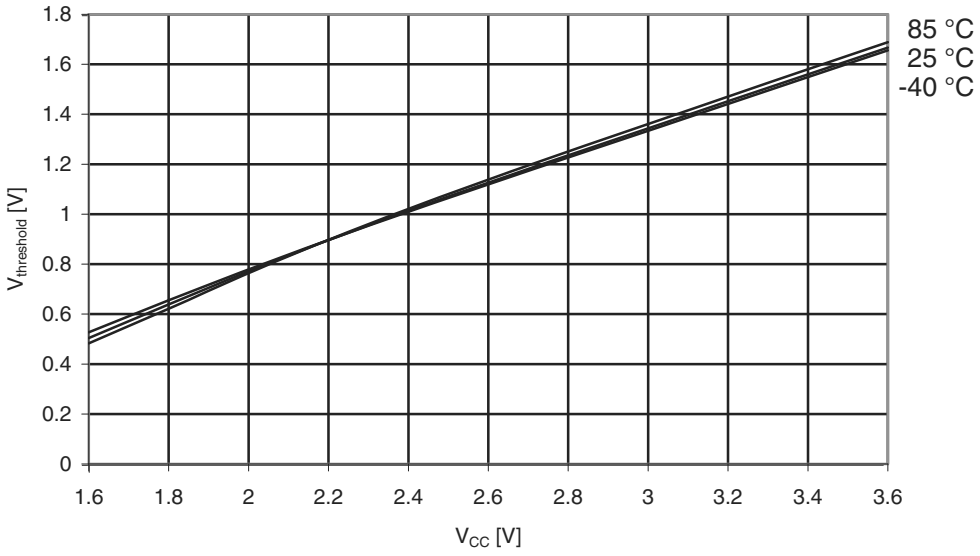


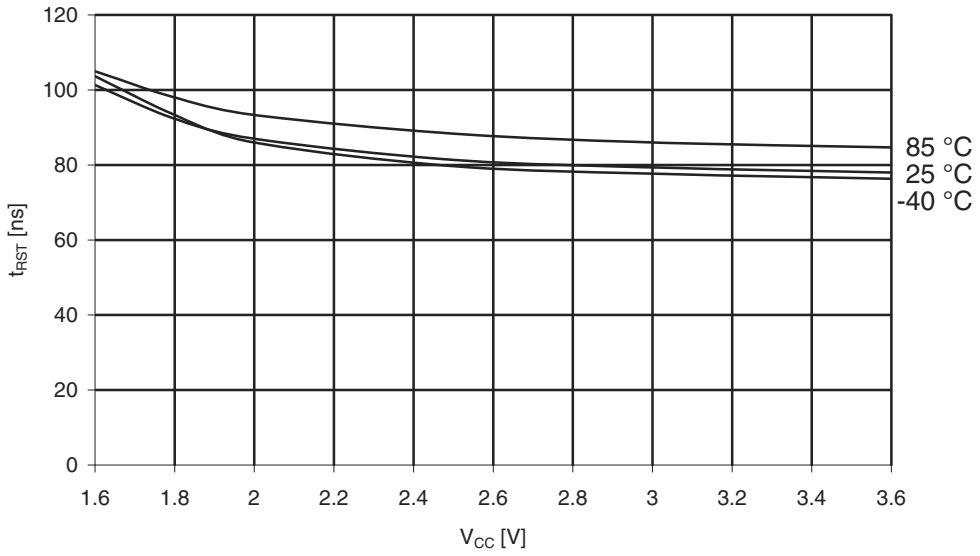
Figure 35-28. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} - I/O Pin Read as "0"



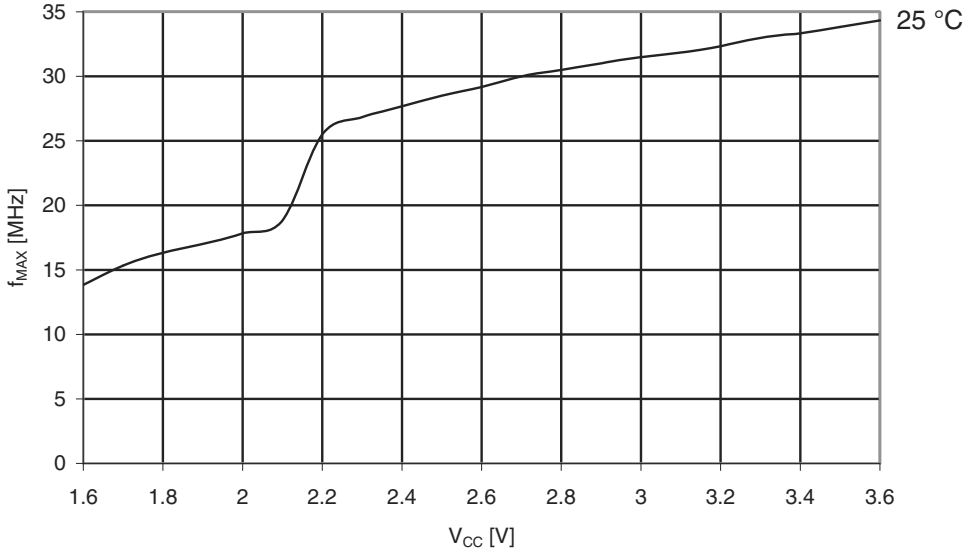
35.11 Reset Pulsewidth

Figure 35-41. Minimum Reset Pulse Width vs. Vcc



35.12 PDI Speed

Figure 35-42. PDI Speed vs. Vcc



12. DAC refresh may be blocked in S/H mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workaround

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

13. Conversion lost on DAC channel B in event triggered mode

If during dual channel operation channel 1 is set in auto trigged conversion mode, channel 1 conversions are occasionally lost. This means that not all data-values written to the Channel 1 data register are converted.

Problem fix/Workaround

Keep the DAC conversion interval in the range 000-001 (1 and 3 CLK), and limit the Peripheral clock frequency so the conversion internal never is shorter than 1.5 µs.

14. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

15. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

16. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

17. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

18. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768 kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA A Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

19. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

20. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

37. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

37.1 8116J - 06/13

1. Not recommended for new designs - Use ATxmega256A3BU

37.2 8116I - 09/10

1. Updated ”Errata” on page 95.

37.3 8116H - 08/10

1. Updated Footnote 2 of Figure 2-1 on page 3.
2. Updated ”Features” on page 28. Event Channel 0 output on port pin 7.
3. Updated ”Timer/Counter and AWEX functions” on page 50.
4. Updated ”Alternate Pin Functions” on page 52.
5. Updated Table 30-3 on page 52. Pin 15 is VCC.
6. Updated ”DC Characteristics” on page 64 by adding Icc for Flash/EEPROM Programming.
7. Added AVCC in ”ADC Characteristics” on page 68.
8. Updated Start up time in ”ADC Characteristics” on page 68.
9. Updated ”DAC Characteristics” on page 69. Removed DC output impedence.
10 Updated ”VBAT and Battery Backup Characteristics” on page 73.
11. Updated Figure 35-6 on page 76. Replaced the figure by a correct one.
12. Fixed typo in “Errata” section.
13. Editorial updates.

37.4 8116G - 05/10

1. Updated the device pin-out Figure 2-1 on page 3. PDI_CLK and PDI_DATA renamed only PDI.
2. Deleted page with duplicated information on Production Signature Row in ”Production Signature Row” on page 12.
3. Changed value for Crystal Oscillator from 32 kHz to 32.768 kHz in ”Clock Options” on page 18.
4. Updated ”DAC - 12-bit Digital to Analog Converter” on page 44. DAC uses internal 1.0 voltage.
5. Updated ”Timer/Counter and AWEX functions” on page 50.