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**Understanding Embedded - CPLDs (Complex Programmable Logic Devices)** 

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

#### **Applications of Embedded - CPLDs**

Details		
Product Status	Active	
Programmable Type	In System Programmable	
Delay Time tpd(1) Max	6.2 ns	
Voltage Supply - Internal	1.71V ~ 1.89V	
Number of Logic Elements/Blocks	1270	
Number of Macrocells	980	
Number of Gates	-	
Number of I/O	212	
Operating Temperature	0°C ~ 85°C (TJ)	
Mounting Type	Surface Mount	
Package / Case	256-BGA	
Supplier Device Package	256-FBGA (17x17)	
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm1270gf256c4n	

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

MII51006-1.6

#### **Software**

MAX® II devices are supported by the Altera® Quartus® II design software with new, optional MAX+PLUS® II look and feel, which provides HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, and device programming. Refer to the Design Software Selector Guide for more details about the Quartus II software features.

The Quartus II software supports the Windows XP/2000/NT, Sun Solaris, Linux Red Hat v8.0, and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink interface.

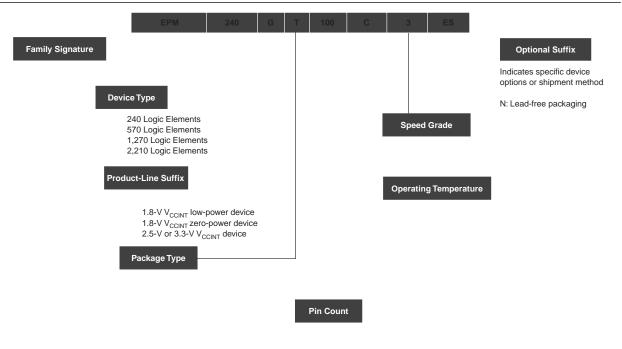
### **Device Pin-Outs**

Printed device pin-outs for MAX II devices are available on the Altera website (www.altera.com).

## **Ordering Information**

Figure 6–1 describes the ordering codes for MAX II devices. For more information about a specific package, refer to the *Package Information* chapter in the *MAX II Device Handbook*.

Figure 6–1. MAX II Device Packaging Ordering Information



## **Referenced Documents**

This chapter references the following document:

■ Package Information chapter in the MAX II Device Handbook

# **Document Revision History**

Table 6–1 shows the revision history for this chapter.

Table 6-1. Document Revision History

Date and Revision	Changes Made	Summary of Changes
August 2009, version 1.6	■ Updated Figure 6–1.	Added information for speed grade –8
October 2008, version 1.5	■ Updated New Document Format.	_
December 2007, version 1.4	<ul><li>Added "Referenced Documents" section.</li><li>Updated Figure 6–1.</li></ul>	Updated document with MAX IIZ information.
December 2006, version 1.3	Added document revision history.	_
October 2006, version 1.2	■ Updated Figure 6-1.	_
June 2005, version 1.1	Removed Dual Marking section.	_