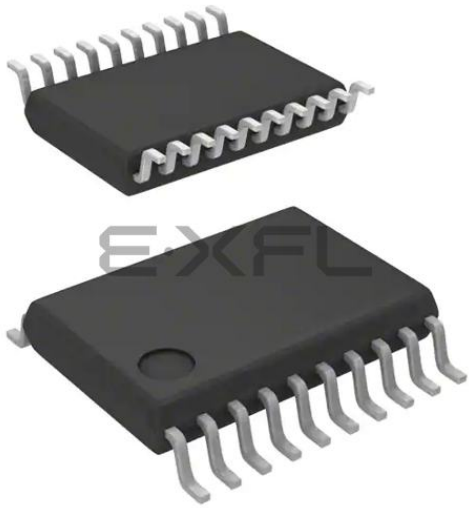
Renesas Electronics America Inc - M37548G3FP#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	740
Core Size	8-Bit
Speed	8MHz
Connectivity	SIO, UART/USART
Peripherals	LED, LVD, POR, WDT
Number of I/O	15
Program Memory Size	6KB (6K x 8)
Program Memory Type	QzROM
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m37548g3fp-u0

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7548 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0210-0202
Rev.2.02
Mar 31, 2009

DESCRIPTION

The 7548 Group is the 8-bit microcomputer based on the 740 family core technology.
The 7548 Group has an 8-bit timer, 16-bit timer, serial interface, A/D converter, power-on reset circuit and the low voltage detection circuit. Also, the Function set ROM is equipped.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.25 µs
  (at 8 MHz oscillation frequency, double-speed mode)
- Memory size
  - ROM ..... 2K, 4K, 6K bytes
  - RAM ..... 192/256 bytes
- Programmable I/O ports
  - I/O port 15
  - Output port 1
- Key-on wakeup 6
- LED direct drive port 8
- Interrupts ..... 12 sources, 12 vectors
- Timers ..... 8-bit × 2
  ..... 16-bit × 1
- Output compare ..... 3 channel
- Input capture ..... 1 channel
- Serial interface ..... 8-bit × 1
  (UART or clock synchronous)
- A/D converter ..... 10-bit resolution × 6-channel
- Clock generating circuit ..... Built-in type
  (connect to external ceramic resonator or quartz-crystal oscillator, 32 kHz quartz-crystal oscillation available)
- High-speed on-chip oscillator ..... Typ. : 4 MHz
- Low-speed on-chip oscillator ..... Typ. : 250 kHz
- Watchdog timer ..... 16-bit × 1
- Power-on reset circuit ..... Built-in type
- Low voltage detection circuit ..... Built-in type
- Power source voltage
  XIN oscillation frequency
  (at ceramic resonator, in double-speed mode)
  - At 8 MHz ..... 4.5 to 5.5 V
  - At 2 MHz ..... 2.4 to 5.5 V
  - At 1 MHz ..... 2.2 to 5.5 V

  XIN oscillation frequency
  (at ceramic resonator, in high-speed mode)
  - At 8 MHz ..... 4.0 to 5.5 V
  - At 4 MHz ..... 2.4 to 5.5 V
  - At 1 MHz ..... 1.8 to 5.5 V

  High-speed on-chip oscillator oscillation frequency
  - At 4 MHz ..... 4.0 to 5.5 V

  Low-speed on-chip oscillator oscillation frequency
  - At 250 kHz (typ. value at VCC = 5 V) ... 1.8 to 5.5 V
- Power dissipation ..... 30 mW
- Operating temperature range ..... -20 to 85°C

APPLICATION

Office automation equipment, factory automation equipment, home electric appliances, consumer electronics, etc.

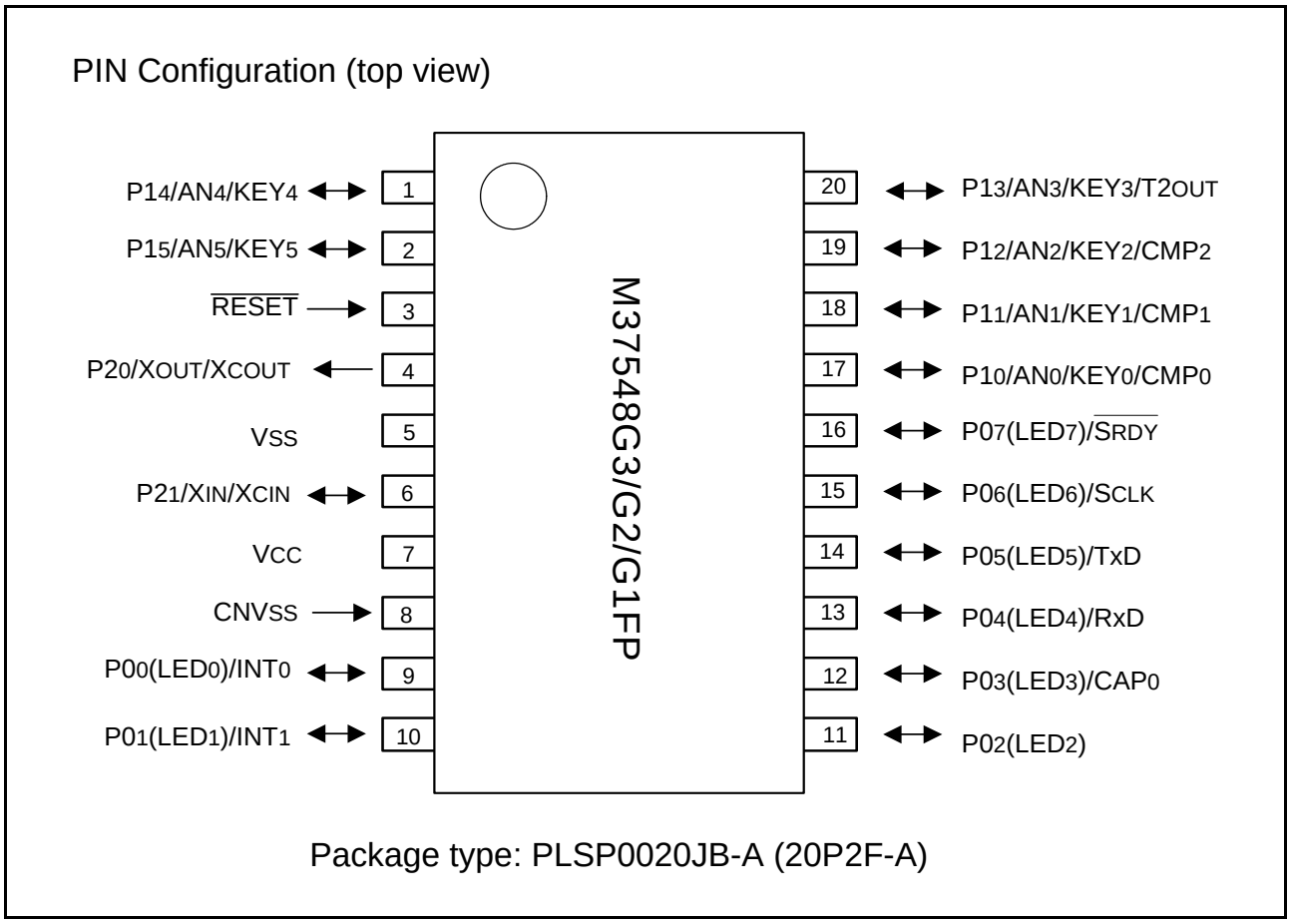


Fig 1. Pin configuration (PLSP0020JB-A type)

PERFORMANCE OVERVIEW

Table 1 Performance overview

Parameter			Function
Number of basic instructions			71
Instruction execution time			0.25 μs (Minimum instruction, oscillation frequency 8 MHz, double-speed mode)
Oscillation frequency			8 MHz (Maximum)
Memory sizes	ROM	M37548G1	2K bytes × 8 bits
		M37548G2	4K bytes × 8 bits
		M37548G3	6K bytes × 8 bits
	RAM	M37548G1	192 bytes × 8 bits
		M37548G2	256 bytes × 8 bits
		M37548G3	256 bytes × 8 bits
I/O port	$P0_0$-$P0_7$	I/O	1-bit × 8, LED direct drive ports
	$P1_0$-$P1_5$	I/O	1-bit × 6
	$P2_0$	Output	1-bit × 1
	$P2_1$	I/O	1-bit × 1
Interrupts	Source		12 sources, 12 vectors
Timer			8-bit × 2, 16-bit × 1
Output compare			3-channel
Input capture			1 channel
Serial interface			8-bit × 1 (UART or clock synchronous)
A/D converter			10-bit resolution × 6 channel
Watchdog timer			16-bit × 1
Power-on reset circuit			Built-in
Low voltage detection circuit			Built-in
Clock generating circuit			Built-in (external ceramic resonator or quartz-crystal oscillator, external 32-kHz quartz-crystal oscillator available) (built-in high/low-speed on-chip oscillator)
Function set ROM area	Function set ROM		Function set ROM is assigned to address $FFD8_{16}$ to $FFDA_{16}$. Valid/invalid of low voltage detection circuit can be selected. Oscillation mode can be selected. Enable/disable of watchdog timer and STP instruction can be selected.
	ROM code protect		ROM code protect is assigned to address $FFDB_{16}$. Read/write the built-in QzROM by serial programmer is disabled by setting “00” to ROM code protect.
Power source voltage (at ceramic resonator)	Double-speed mode	at 8 MHz oscillation	4.5 to 5.5 V
		at 2 MHz oscillation	2.4 to 5.5 V
		at 1 MHz oscillation	2.2 to 5.5 V
	High-speed mode	at 8 MHz oscillation	4.0 to 5.5 V
		at 4 MHz oscillation	2.4 to 5.5 V
		at 1 MHz oscillation	1.8 to 5.5 V
Power source voltage (at high-speed on-chip oscillator)	Double-speed mode	at 4 MHz oscillation	4.0 to 5.5 V
Power source voltage (at low-speed on-chip oscillator)	Double-speed mode	at 250 kHz oscillation	1.8 to 5.5 V
Power dissipation			30 mW (Typ.)
Operating temperature range			-20 to 85 °C
Device structure			CMOS silicon gate
Package			20-pin plastic molded SSOP (PLSP0020JB-A)

GROUP EXPANSION

Renesas plans to expand the 7548 group as follow:

Memory Type

Support for QzROM version and emulator MCU.

Memory Size

- ROM size ..... 2K to 6K bytes
- RAM size ..... 192 to 256 bytes

Packages

- PLSP0020JB-A .... 0.65 mm-pitch 20-pin plastic molded SSOP
- 42S1M ..... 42-pin shrink ceramic PIGGY BACK

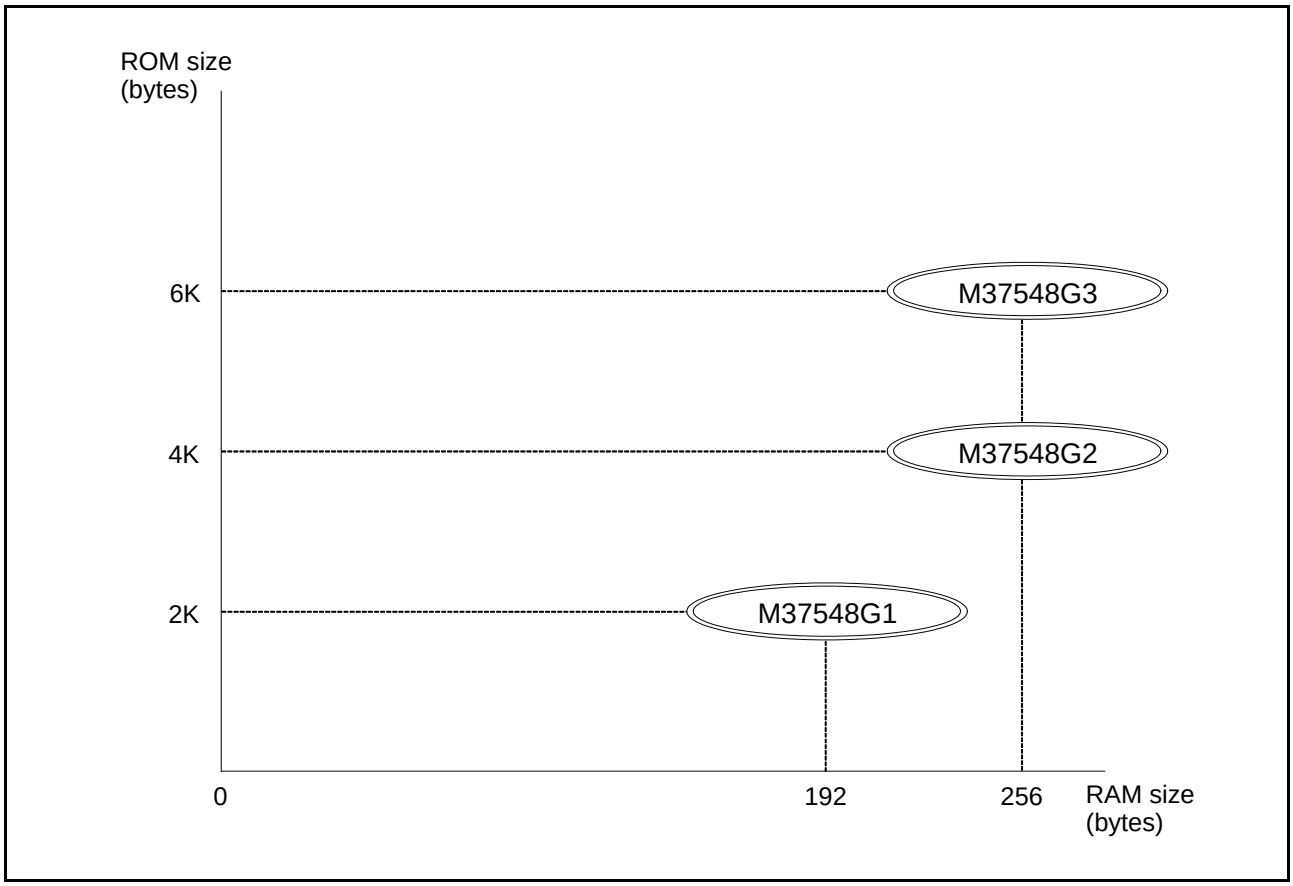


Fig 4. Memory expansion plan

Currently supported products are listed below.

Table 3 List of supported products

As of Mar. 2009

Part number	ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M37548G3-XXXFP	6144 (6014)	256	PLSP0020JB-A	QzROM version
M37548G3FP				QzROM version (blank)
M37548G2-XXXFP	4096 (3966)	256	PLSP0020JB-A	QzROM version
M37548G2FP				QzROM version (blank)
M37548G1-XXXFP	2048 (1918)	192	PLSP0020JB-A	QzROM version
M37548G1FP				QzROM version (blank)
M37549RLSS	–	256	42S1M	Emulator MCU

NOTE:
1. ROM size includes the function set ROM.

Memory

• Special Function Register (SFR) Area

The SFR area in the zero page contains control registers such as I/O ports and timers.

• RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

• ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.
The user area includes the function set ROM area.

• Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

• Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

• Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

• Function set ROM Area

[Renesas shipment test area]

Figure 8 shows the Assignment of Function set ROM area.
The random data are set to the Renesas shipment test areas (addresses $FFD4_{16}$ to address $FFD7_{16}$).
Do not rewrite the data of these areas.
When the checksum is included in the user program, avoid assigning it to these areas.

[Function set ROM data] FSROM0, FSROM1, FSROM2

Function set ROM data 0 to 2 (addresses $FFD8_{16}$ to $FFDA_{16}$) are used to set modes of peripheral functions.
By setting values to these areas, the operation mode of each peripheral function are set after releasing reset.
Refer to the descriptions of peripheral functions for the details of operation of peripheral functions.

- Clock generating circuit (page 46)
- Watchdog timer (page 42)
- Low voltage detection circuit (page 44)

[ROM code protect]

Address $FFDB_{16}$ of QzROM version is ROM code protect address and cannot be used for programming. "00_{16}" is written into this address when selecting the protect bit write by using a serial programmer and selecting protect enabled for writing shipment by Renesas Technology corp.. When "00_{16}" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to the corresponding area is disabled by a serial programmer.
As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.
As for the QzROM product shipped after writing, "00_{16}" (protect enabled) or "FF_{16}" (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing.
The writing of "00_{16}" or "FF_{16}" can be selected as ROM option setup ("MASK option" written in the mask file converter) when ordering.

<Notes>

(1) Because the contents of RAM are indefinite at reset, set initial values before using.
(2) Do not access to the reserved area.
(3) Random data is written into the Renesas shipment test area and the reserved ROM area. Do not rewrite the data in these areas. Data of these area may be changed without notice. Accordingly, do not include these areas into programs such as checksum of all ROM areas.
(4) The QzROM values in function set ROM data 0 to 2 set the operating modes of the various peripheral functions after an MCU reset is released. Do not fail to set the value for the selected function. Bits designated with a fixed value of 1 or 0 must be set to the designated value.

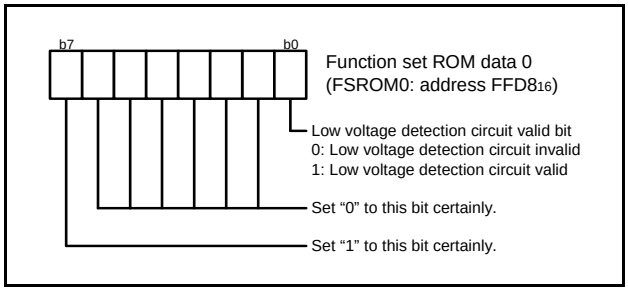
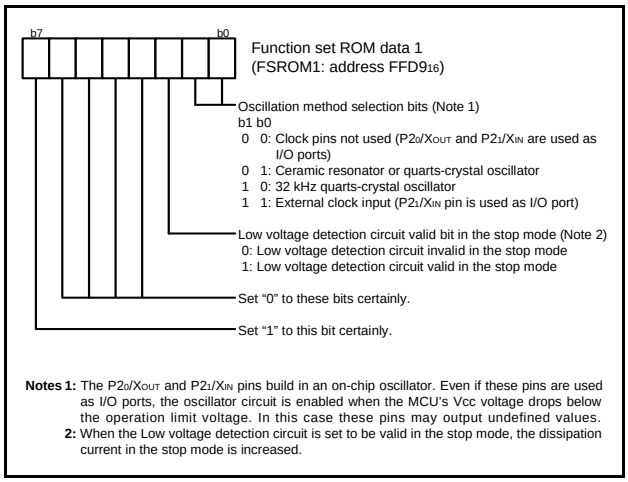
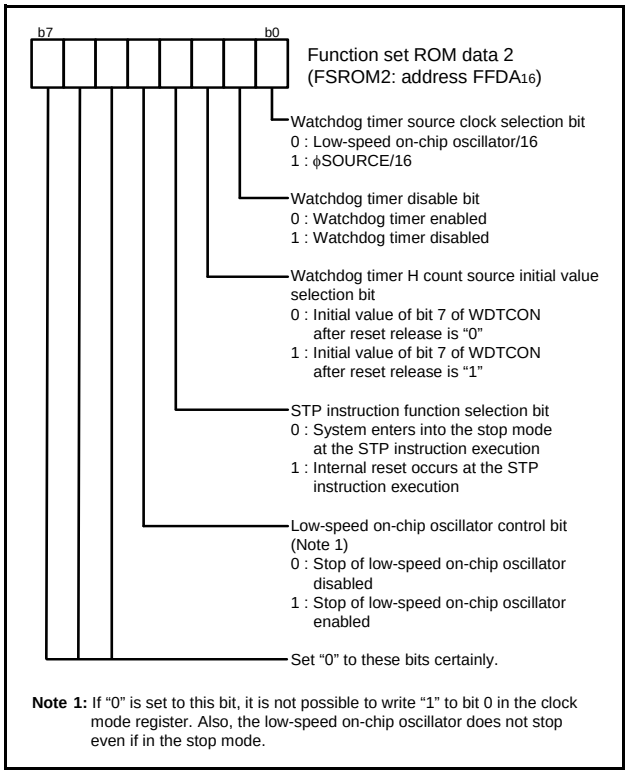


Fig 10. Structure of Function set ROM data 0



Notes 1: The P20/XOUT and P21/XIN pins build in an on-chip oscillator. Even if these pins are used as I/O ports, the oscillator circuit is enabled when the MCU's Vcc voltage drops below the operation limit voltage. In this case these pins may output undefined values.
2: When the Low voltage detection circuit is set to be valid in the stop mode, the dissipation current in the stop mode is increased.

Fig 11. Structure of Function set ROM data 1



Note 1: If “0” is set to this bit, it is not possible to write “1” to bit 0 in the clock mode register. Also, the low-speed on-chip oscillator does not stop even if in the stop mode.

Fig 12. Structure of Function set ROM data 2

Table 6 I/O port function table

Pin	Name	I/O format	Non-port function	SFRs related each pin
$P0_0(LED_0)/INT_0$ $P0_1(LED_1)/INT_1$	I/O port P0	CMOS compatible input level CMOS 3-state output	External interrupt input	Interrupt edge selection register Port P0 drive capacity control register Port P0 pull-up control register
$P0_2(LED_2)$				Port P0 drive capacity control register Port P0 pull-up control register
$P0_3(LED_3)/CAP_0$			Capture input	Capture/Compare port register Port P0 drive capacity control register Port P0 pull-up control register
$P0_4(LED_4)/RxD$			Serial interface input/ output	Serial I/O control register Port P0 drive capacity control register Port P0 pull-up control register
$P0_5(LED_5)/TxD$				Serial I/O control register UART control register Port P0 drive capacity control register Port P0 pull-up control register
$P0_6(LED_6)/SCLK$				Serial I/O control register Port P0 drive capacity control register Port P0 pull-up control register
$P0_7(LED_7)/\overline{SRDY}$				Serial I/O control register Port P0 drive capacity control register Port P0 pull-up control register
$P1_0/AN_0/KEY_0/CMP_0$ $P1_1/AN_1/KEY_1/CMP_1$ $P1_2/AN_2/KEY_2/CMP_2$	I/O port P1		Compare output Key input interrupt A/D conversion input	Capture/Compare port register Port P1 pull-up control register Key-on wakeup input selection register AD control register
$P1_3/AN_3/KEY_3/T2OUT$			Timer 2 output Key input interrupt A/D conversion input	Timer mode register Port P1 pull-up control register Key-on wakeup input selection register AD control register
$P1_4/AN_4/KEY_4$ $P1_5/AN_5/KEY_5$			Key input interrupt A/D conversion input	Port P1 pull-up control register Key-on wakeup input selection register AD control register
$P2_0/XOUT/XCOUT$	I/O port P2	CMOS 3-state output	Clock pin	Function set ROM data 1 (Note) Clock mode register
$P2_1/XIN/XCIN$		CMOS compatible input level CMOS 3-state output	Clock pin	Function set ROM data 1 (Note) Clock mode register

NOTE:
1. Function set ROM data 1 is included in the function set ROM area.

• Interrupt Request Generation, Acceptance, and Handling

Interrupts have the following three phases.

(i) Interrupt Request Generation
An interrupt request is generated by an interrupt source (external interrupt signal input, timer underflow, etc.) and the corresponding request bit is set to "1".

(ii) Interrupt Request Acceptance
Based on the interrupt acceptance timing in each instruction cycle, the interrupt control circuit determines acceptance conditions (interrupt request bit, interrupt enable bit, and interrupt disable flag) and interrupt priority levels for accepting interrupt requests. When two or more interrupt requests are generated simultaneously, the highest priority interrupt is accepted. The value of interrupt request bit for an unaccepted interrupt remains the same and acceptance is determined at the next interrupt acceptance timing point.

(iii) Handling of Accepted Interrupt Request
The accepted interrupt request is processed.

Figure 21 shows the time up to execution in the interrupt processing routine, and Figure 22 shows the interrupt sequence. Figure 23 shows the timing of interrupt request generation, interrupt request bit, and interrupt request acceptance.

• Interrupt Handling Execution

When interrupt handling is executed, the following operations are performed automatically.

(1) Once the currently executing instruction is completed, an interrupt request is accepted.

(2) The contents of the program counters and the processor status register at this point are pushed onto the stack area in order from 1 to 3.
1. High-order bits of program counter (PCH)
2. Low-order bits of program counter (PCL)
3. Processor status register (PS)

(3) Concurrently with the push operation, the jump address of the corresponding interrupt (the start address of the interrupt processing routine) is transferred from the interrupt vector to the program counter.

(4) The interrupt request bit for the corresponding interrupt is set to "0". Also, the interrupt disable flag is set to "1" and multiple interrupts are disabled.

(5) The interrupt routine is executed.

(6) When the RTI instruction is executed, the contents of the registers pushed onto the stack area are popped off in the order from 3 to 1. Then, the routine that was before running interrupt processing resumes.

As described above, it is necessary to set the stack pointer and the jump address in the vector area corresponding to each interrupt to execute the interrupt processing routine.

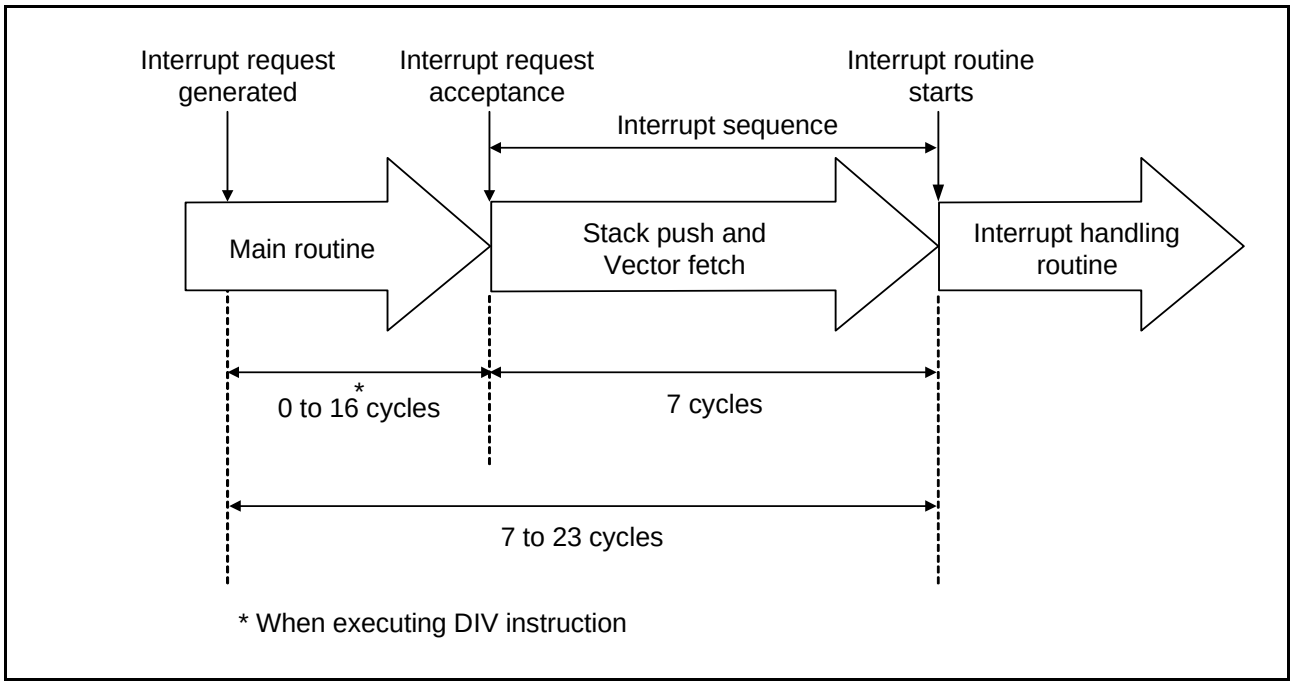


Fig 21. Time up to execution in interrupt routine

Key Input Interrupt (Key-On Wakeup)

A key-on wakeup interrupt request is generated by applying “L” level to any pin of port P1 that has been set to input mode. In other words, it is generated when the AND of input level goes from “1” to “0”. An example of using a key input interrupt is shown in Figure 24, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports P10 to P13 as input ports.

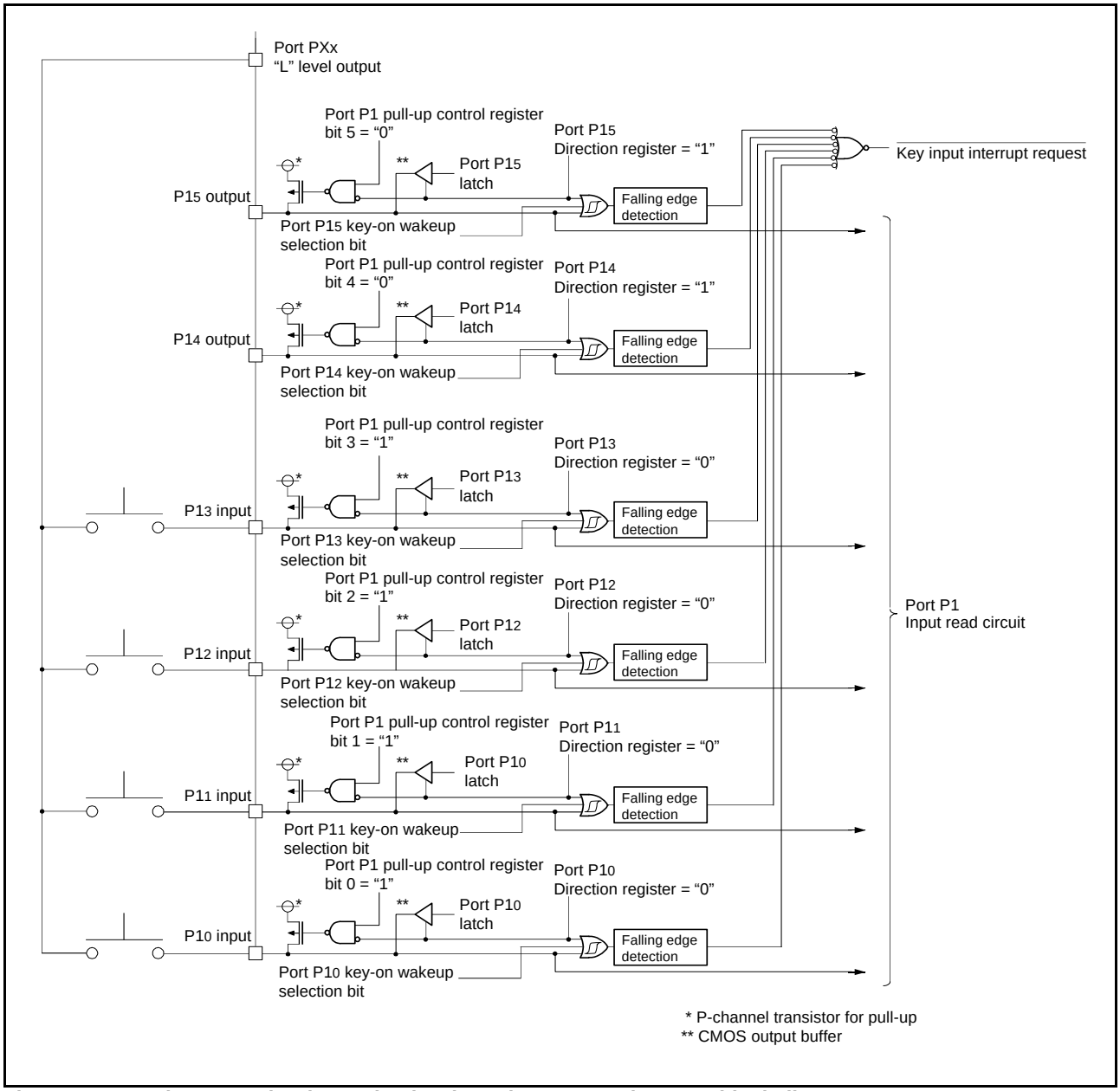


Fig 24. Connection example when using key input interrupt and port P1 block diagram

Timers

The 7548 Group has two 8-bit timers (timer 1 and timer 2) and one 16-bit timer (timer A).
Timer 1 and timer 2 share the same 8-bit prescaler (prescaler 12). Each timer and prescaler has a separate timer latch and prescaler latch.
The division ratio of every timer and prescaler is 1/(n+1), where n is the value of the timer latch or prescaler latch.
The timers decrement at each count clock input. When the count value reaches "0", an underflow occurs at the next count pulse. The value of the corresponding timer latch is reloaded into the timer at underflow and counting is continued. When a timer underflow occurs, the interrupt request bit corresponding to each timer is set to "1".

• Prescaler 12 (PRE12)

Prescaler 12 is an 8-bit prescaler that counts the signal selected by the prescaler 12 count source selection bit. The count source can be selected from ϕSOURCE/16 and XCIN input clock.
Writing to prescaler 12 writes the value to both the prescaler latch and prescaler.
Reading from prescaler 12 reads the prescaler 12 count value. The initial value is set to "FF_{16}" after reset.
The division ratio of prescaler 12 is 1/(n+1), where n is the setting value.
Prescaler 12 cannot stop counting by software.

• Timer 1 (T1)

Timer 1 is an 8-bit timer that counts the prescaler 12 output.
When Timer 1 underflows, the timer 1 interrupt request bit is set to "1".
Writing to timer 1 writes the value to both the timer 1 latch and timer 1.
Reading from timer 1 reads the timer 1 count value. The initial value is set to "01_{16}" after reset.
The division ratio of timer 1 is 1/(m+1), where m is the setting value. This gives that the division ratio of prescaler 12 and timer 1 is 1/((n+1) × (m+1)), where n is the prescaler 12 setting value and m is the timer 1 setting value.
Timer 1 cannot stop counting by software.

• Timer 2 (T2)

Timer 2 is an 8-bit timer that counts the signal selected by the timer 2 count source selection bit.
The count source can be selected from among ϕSOURCE/16, /256, prescaler 12 output, and timer A output signal.
Timer 2 counts the selected count source and sets the timer 2 interrupt request bit to "1" at underflow.
When writing to timer 2, the value of the timer 2 write control bit can be used to select a write to both the timer 2 latch and timer 2 or a write to only the timer 2 latch.
Reading from timer 2 reads the timer 2 count value.
Timer 2 starts counting from "FF_{16}" after reset.
The division ratio of timer 2 is 1/(n+1), where n is the timer 2 setting value. Timer 2 stops when the timer 2 count stop bit is set to "1".
When the P13/T2OUT output valid bit is set to "1", the polarity of the waveform output from the P13/T2OUT pin can be inverted at each timer 2 underflow. The output start level of the T2OUT pin can be selected using the T2OUT polarity switch bit. When this bit is set to 0, the output starts at "H" level. When this bit is set to "1", the output starts at "L" level.

• Notes

(1) Reading from and Writing to Timer 1 and 2 and Prescaler 12

If the timer/prescaler count source clock and ϕSOURCE are different clocks, the timers and prescaler cannot be read or written. Select the same clock to enable read and write operations.

Note that timer 2 can be read and written even using a different clock while its counting is stopped.

①Prescaler 12 and timer 1 cannot be read/written in the following conditions:

Prescaler 12 count source: XCIN input clock

ϕSOURCE: Clock other than XCIN input clock

②Timer 2 cannot be read/written during counting in the following conditions:

Timer 2 count source: Prescaler 12

Prescaler 12 count source: XCIN input clock

ϕSOURCE: Clock other than XCIN input clock

or

Timer 2 count source: Timer A underflow

Timer A count source: XCIN input clock

ϕSOURCE: Clock other than XCIN input clock

or

Timer 2 count source: Timer A underflow

Timer A count source: low-speed on-chip oscillator output

ϕSOURCE: Clock other than low-speed on-chip oscillator

(2) Count Source of Prescaler 12

The XCIN input clock can be selected as the prescaler count source only if the 32 kHz quartz crystal oscillator is selected by the oscillation method selection bit in FSROM1.

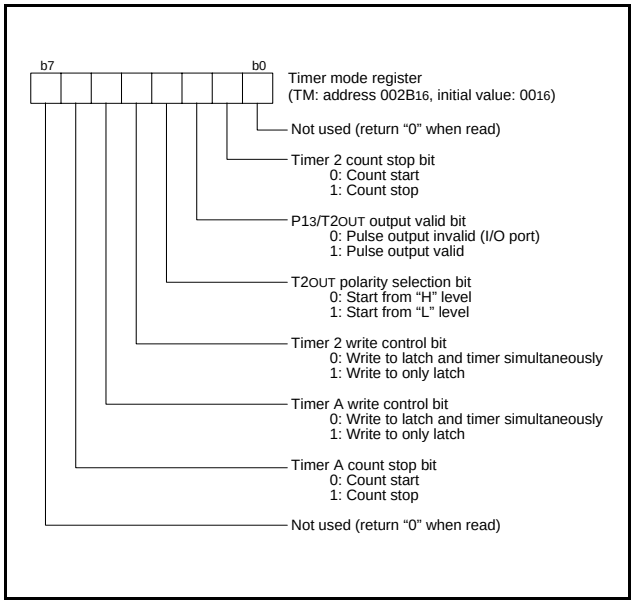


Fig 26. Structure of timer mode register

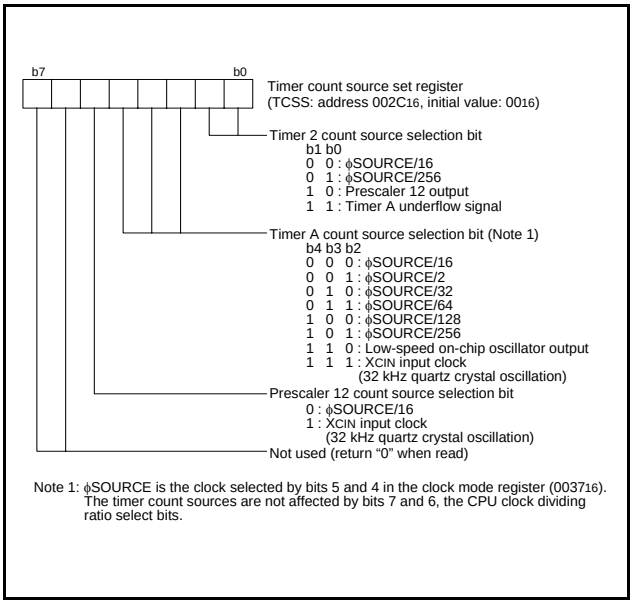


Fig 27. Structure of timer count source set register

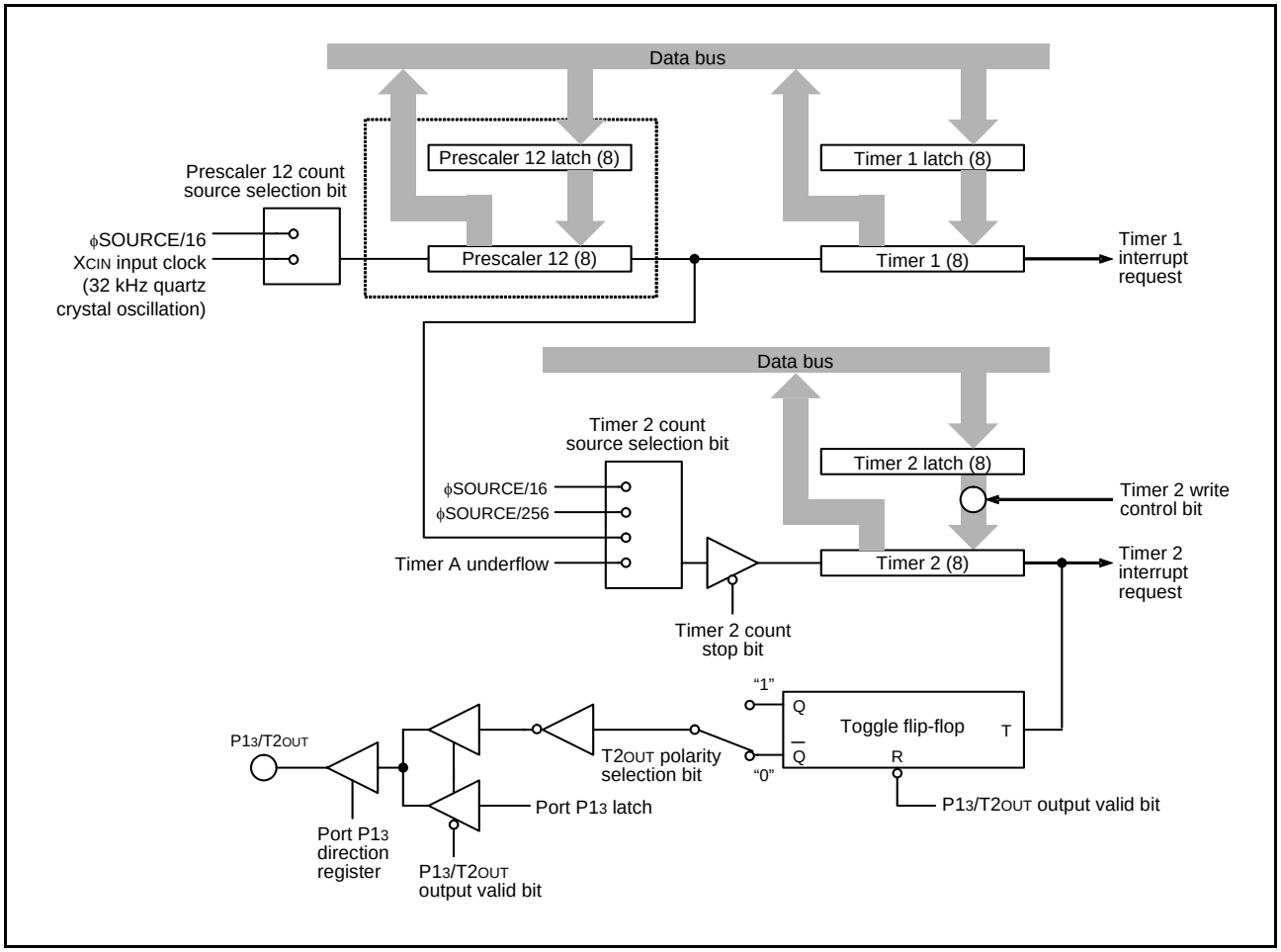


Fig 28. Block diagram of timer 1 and timer 2

Clock Generating Circuit

The clock generating circuit includes the XIN clock (ceramic oscillator or crystal oscillator can be used), XCIN clock (32 kHz oscillator can be used), external clock input, high-speed on-chip oscillator, and low-speed on-chip oscillator.
Pins P20/XOUT/XCOUT and P21/XIN/XCIN can be shared for the ports, XIN oscillation, and XCIN oscillation.
Use the oscillation method selection bits (bits 1 and bit 0 in function set ROM data 1 (FSROM1)) to set the function of these pins.

• Ceramic Resonator or Crystal Oscillator

Set the oscillation method selection bits (bits 1 and bit 0 in FSROM1) to "01$_2$", and connect the ceramic resonator (or the oscillator) and external circuit with the shortest wiring length possible.
The constants of the oscillator circuit differ depending on the resonator. Use the values recommended by the resonator manufacturer. (An external feedback resistor may be necessary under some conditions.)
Setting the XIN/XCIN oscillation control bit to "0" starts oscillation. This bit is sets to "0" after reset.

• 32 kHz Crystal Oscillator

Set the oscillation method selection bits to "10$_2$", and connect the 32 kHz crystal oscillator and external circuit with the shortest wiring length possible.
The constants of the oscillator circuit differ depending on the resonator. Use the values recommended by the resonator manufacturer. (An external feedback resistor may be necessary under some conditions.)
Setting the XIN/XCIN oscillation control bit to "0" starts oscillation. This bit is sets to "0" after reset.

• External Clock Input

Set the oscillation method selection bits to "11$_2$", and connect the clock source to the P20/XOUT pin. In this case, the P21/XIN pin can be used as an I/O port.

• High-Speed On-Chip Oscillator

The high-speed on-chip oscillator is stopped after reset.
Setting the high-speed on-chip oscillator oscillation control bit (bit 1 in CLKM) to "0" starts oscillation. This bit is sets to "1" after reset.

• Low-Speed On-Chip Oscillator

The low-speed on-chip oscillator automatically starts oscillating after reset.
Setting the low-speed on-chip oscillator oscillation control bit (bit 0 in CLKM) to "1" stops oscillation. This bit is sets to "0" after reset. If the low-speed on-chip oscillator control bit (bit 4 in FSROM2) is set to "0" and stopping the low-speed on-chip oscillator is disabled, the low-speed on-chip oscillator oscillation control bit cannot be set to "1" and oscillation cannot be stopped. Also, the oscillator does not stop even when the STP instruction is executed.

• Using No Oscillator Pins (P20 as output port and P21 as I/O port)

To use only an internal on-chip oscillator, set the oscillation method selection bits to "00$_2$". The P20/XOUT pin can be used as an output port and the P21/XIN pin can be used as an I/O port.

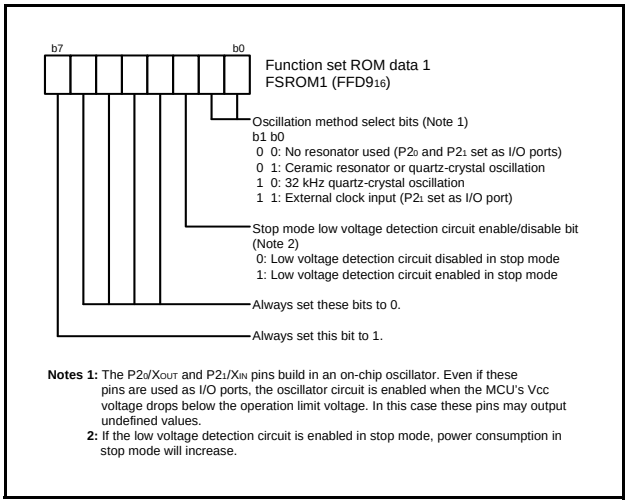


Fig 61. Structure of function set ROM data 1

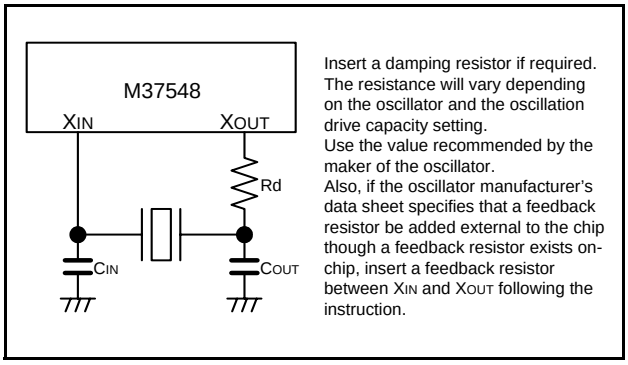


Fig 62. External circuit of ceramic resonator

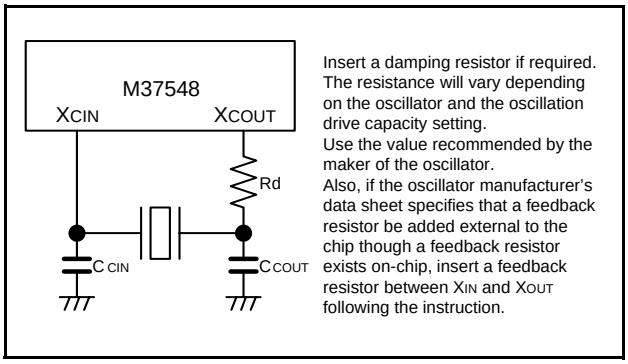


Fig 63. External circuit of 32 kHz quarts-crystal oscillator

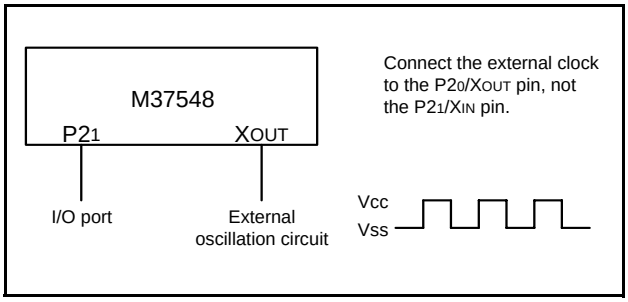


Fig 64. External clock input circuit

• Stop mode

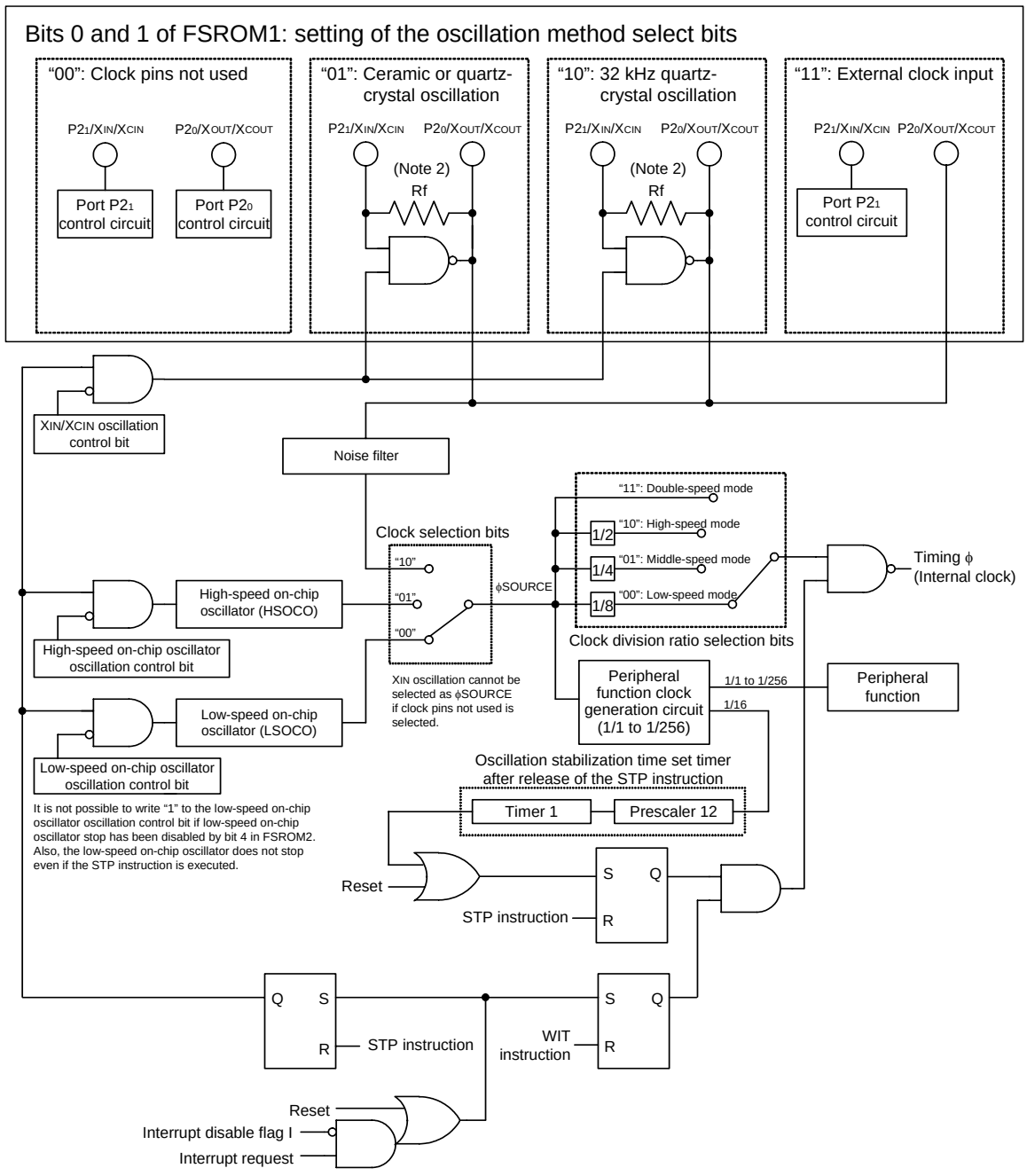
When the STP instruction is executed, the internal clock ϕ stops at an "H" level and the X_{IN}/X_{CIN} and on-chip oscillator stops. At this time, timer 1 is set to "01_{16}" and prescaler 12 is set to "FF_{16}" when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 12 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. When an external interrupt is accepted, oscillation is restarted but the internal clock ϕ remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock ϕ is supplied. This is because when a ceramic resonator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an "L" level to the $\overline{\text{RESET}}$ pin while oscillation becomes stable, or set the wait time by on-chip oscillator operation after system is released from reset until the oscillation is stabled.

• Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

• Note

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 12 after fully appreciating the oscillation stabilization time of the oscillator to be used.



Notes 1: The oscillation circuit is built in the P20/XOUT/XCOUT pin and the P21/XIN/XCIN pin. When the Vcc of the microcomputer is lower than the operation lower bound voltage even if these pins are used as I/O ports, the oscillation circuit is connected and undefined values may be output from these pins.

2: Although a feed-back resistor exists on-chip, an external feed-back resistor may be needed depending on conditions.

Fig 66. Block diagram of internal clock generating circuit

NOTES ON PROGRAMMING

(1) Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is "1". After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations. Initialize these flags at the beginning of the program.

(2) Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

(3) Decimal Calculations

- For calculations in decimal notation, set the decimal mode flag D to "1", then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.
- In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

(4) Ports

The values of the port direction registers cannot be read. That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.
For setting direction registers, use the LDM instruction, STA instruction, etc.

(5) A/D Conversion

Do not execute the STP instruction during A/D conversion.

(6) Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.
The frequency of the internal clock ϕ is the same as that of the ϕSOURCE in double-speed mode, twice the ϕSOURCE cycle in high-speed mode, 4 times the ϕSOURCE cycle in middle-speed mode and 8 times the ϕSOURCE cycle in low-speed mode.

(7) CPU Mode Register

The processor mode bits can be written only once after releasing reset. Always set them to "00_2". After written, rewriting any data to these bits is disabled because they are locked. (Emulator MCU is excluded.)

(8) State transition

Do not stop the clock selected as the operation clock because of setting of bits 0 to 2.

NOTES ON HARDWARE

(1) Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin). A ceramic capacitor of 0.01 μF to 0.1 μF is recommended.
Connect a capacitor across the power source pin and GND pin with the shortest possible wiring.

(2) Note on Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.
In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the supply voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

2. Connection of bypass capacitor across Vss line and Vcc line

Connect an approximately 0.1 µF bypass capacitor across the VSS line and the VCC line as follows:

- Connect a bypass capacitor across the VSS pin and the VCC pin at equal length.
- Connect a bypass capacitor across the VSS pin and the VCC pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for VSS line and VCC line.
- Connect the power source wiring via a bypass capacitor to the VSS pin and the VCC pin.

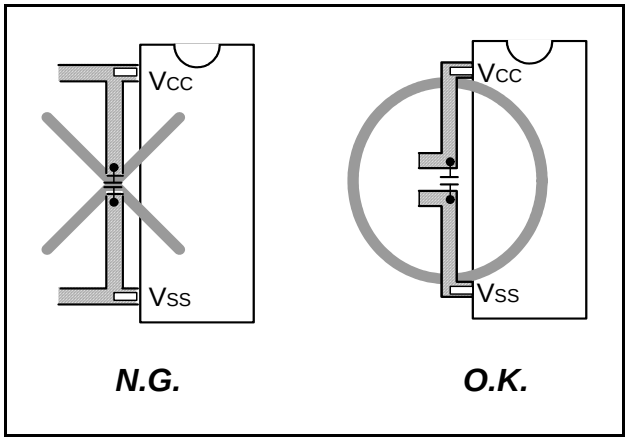


Fig 77. Bypass capacitor across the Vss line and the Vcc line

3. Wiring to analog input pins

The analog input pin is connected to the capacitor of a voltage comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A/D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A/D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

4. Oscillator concerns

Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

(1) Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

<Reason>

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

(2) Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

<Reason>

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

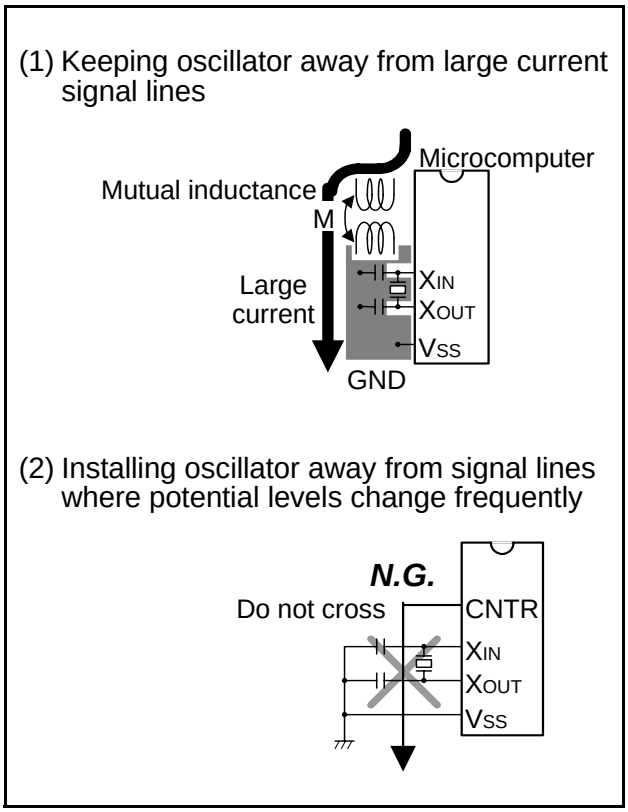


Fig 78. Wiring for a large current signal line/Writing of signal lines where potential levels change frequently

(3) Oscillator protection using VSS pattern

As for a two-sided printed circuit board, print a VSS pattern on the underside (soldering side) of the position (on the component side) where an oscillator is mounted.

Connect the VSS pattern to the microcomputer VSS pin with the shortest possible wiring. Besides, separate this VSS pattern from other VSS patterns.

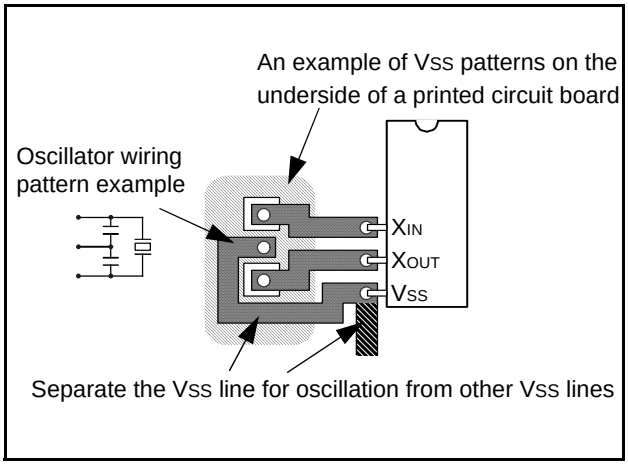
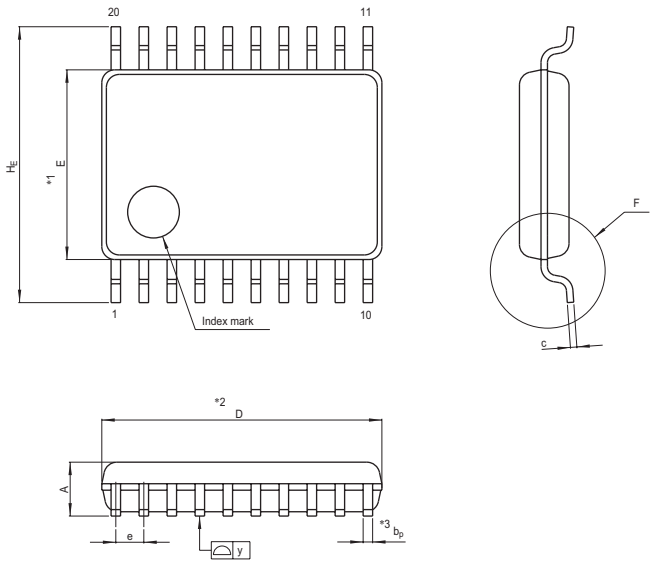


Fig 79. Vss pattern on the underside of an oscillator

PACKAGE OUTLINE

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	20P2F-A	0.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

Notes on Watchdog Timer

1. Watchdog Timer Underflow

The watchdog timer operates in wait mode. To prevent underflow, write to the watchdog timer control register.
The watchdog timer stops in stop mode, but starts counting at the same time as exiting stop mode. After exiting stop mode, it continues counting during oscillation stabilization time. To prevent underflow during the period, the watchdog timer H count source selection bit (bit 7) in the watchdog timer control register (address 003916) should be set to "0" before executing the STP instruction.
Note that the watchdog timer continues counting even if the STP instruction is executed in the following two conditions:

① Stopping the low-speed on-chip oscillator: Disabled (bit 4 in FSROM2)
Source clock of the watchdog timer: Low-speed on-chip oscillator/16 (bit 0 in FSROM2)

② Stopping the low-speed on-chip oscillator: Disabled (bit 4 in FSROM2)
Source clock of the watchdog timer: ϕSOURCE (bit 0 in FSROM2)
ϕSOURCE: Low-speed on-chip oscillator (bits 5 and 4 in CLKM)

2. STP instruction function selection bit

The function of the STP instruction can be selected by the bit 2 in FSROM2. This bit cannot be used for rewriting by executing the STP instruction.

- When this bit is set to "0", stop mode is entered by executing the STP instruction.
- When this bit is set to "1", internal reset occurs by executing the STP instruction.

Notes on RESET pin

1. Connecting capacitor

In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and V_{SS} pin.
And use a 1000 pF or more capacitor for high frequency use.
When connecting the capacitor, note the following:

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

<Reason>
If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

Note on Clock Generating Circuit

1. Switching to X_{IN}/X_{CIN} Oscillator

After a reset is cleared, operation starts using the low-speed on-chip oscillator. When switching to X_{IN}/X_{CIN} oscillator, make sure to set a sufficient wait duration with the on-chip oscillator to allow the X_{IN}/X_{CIN} oscillator to stabilize.

Note on Oscillation Control

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 12 after fully appreciating the oscillation stabilization time of the oscillator to be used.

Notes on Oscillation Stop Detection Circuit

(1) Do not execute the transition to "state 2'a" shown in Figure 69 State transition of oscillation stop detection circuit. In this state, no reset is triggered and the MCU is stopped even when the X_{IN} oscillation stops.

(2) After an oscillation stop detection reset, if this reset is enabled while bits X_{IN} oscillation stop detection function active and oscillation stop detection status are retained, a reset is triggered again.

(3) The oscillation stop detection status bit is initialized under the following conditions:
- External reset, power-on reset, low-voltage detection reset, watchdog timer reset, and reset by the STP instruction function.
- Write 0 to the X_{IN} oscillation stop detection function active bit

(4) While the oscillation stop detection function is in active, the oscillation stop detection status bit may set to 1 when the watchdog timer underflows or by a reset when the STP instruction is executed with the STP instruction function selection bit set to 1.
When an oscillation stop detection reset is triggered, reconfirm that oscillation is stopped.

(5) The oscillation stop detection circuit is not included in the emulator MCU "M37549RLSS".

Note on Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.
In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the supply voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

Note on Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin). A ceramic capacitor of 0.01 μF to 0.1 μF is recommended.
Connect a capacitor across the power source pin and GND pin with the shortest possible wiring.

Note on Memory

(1) Because the contents of RAM are indefinite at reset, set initial values before using.
(2) Do not access to the reserved area.
(3) Random data is written into the Renesas shipment test area and the reserved ROM area. Do not rewrite the data in these areas. Data of these area may be changed without notice. Accordingly, do not include these areas into programs such as checksum of all ROM areas.
(4) The QzROM values in function set ROM data 0 to 2 set the operating modes of the various peripheral functions after an MCU reset is released. Do not fail to set the value for the selected function. Bits designated with a fixed value of 1 or 0 must be set to the designated value.

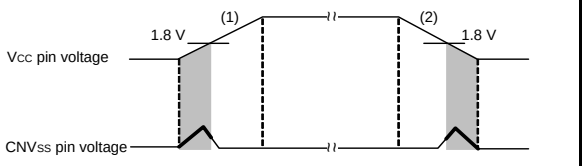
Notes on QzROM

1. Note on Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

2. Overvoltage

Take care not to apply the voltage above the Vcc pin voltage to other pins. Make sure that the voltage of the CNVSS pin (VPP power input pin for QzROM) does not change as shown in the bold-lined periods (Figure 92) when powering on and off. If the voltage changes as shown, the QzROM contents may be rewritten.



(1) The input voltage to other MCU pins rises before the Vcc pin voltage rises.
(2) The input voltage to other MCU pins falls before the Vcc pin voltage falls.
Note: If Vcc falls below the minimum value 1.8 V (shaded areas), the internal circuit becomes unstable. Take additional care to prevent overvoltage.

Fig 92. Timing Diagram (bold-lined periods are applicable)

3. QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .mask) which is made by the mask file converter MM.
Be sure to set the ROM option ("MASK option" written in the mask file converter) setup when making the mask file by using the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "00_{16}" and "FF_{16}" can not be accepted.
- Set "FF_{16}" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF_{16}" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

4. Data Required for QzROM Writing Orders

The following are necessary when ordering a QzROM product shipped after writing:
1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.