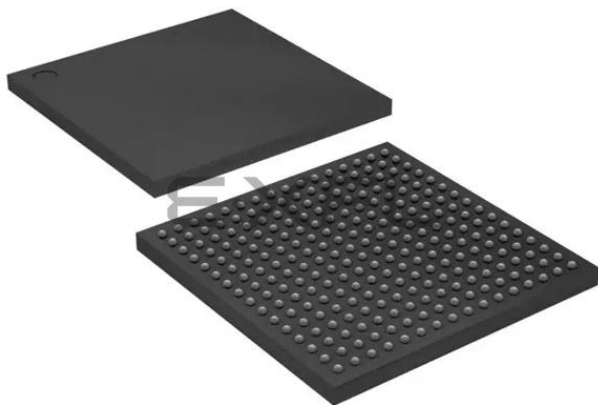




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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	645
Number of Logic Elements/Cells	10320
Total RAM Bits	423936
Number of I/O	179
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce10f17a7n

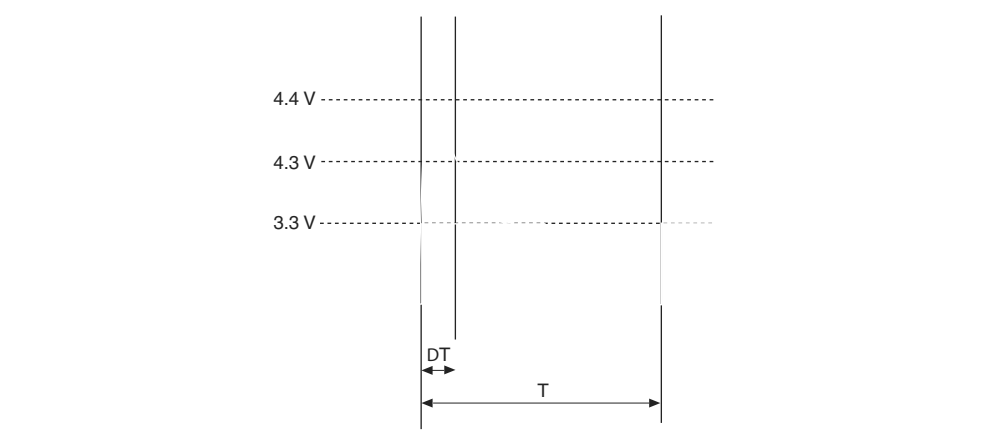
 A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit
V_i	AC Input Voltage	$V_i = 4.20$	100	%
		$V_i = 4.25$	98	%
		$V_i = 4.30$	65	%
		$V_i = 4.35$	43	%
		$V_i = 4.40$	29	%
		$V_i = 4.45$	20	%
		$V_i = 4.50$	13	%
		$V_i = 4.55$	9	%
		$V_i = 4.60$	6	%

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as $([\Delta T]/T) \times 100$. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

Figure 1–1. Cyclone IV Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone IV devices. Table 1–3 and Table 1–4 list the steady-state voltage and current values expected from Cyclone IV E and Cyclone IV GX devices. All supplies must be strictly monotonic without plateaus.

Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices ⁽¹⁾, ⁽²⁾ (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CCINT}^{(3)}$	Supply voltage for internal logic, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply voltage for internal logic, 1.0-V operation	—	0.97	1.0	1.03	V
$V_{CCIO}^{(3), (4)}$	Supply voltage for output buffers, 3.3-V operation	—	3.135	3.3	3.465	V
	Supply voltage for output buffers, 3.0-V operation	—	2.85	3	3.15	V
	Supply voltage for output buffers, 2.5-V operation	—	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	—	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	—	1.425	1.5	1.575	V
	Supply voltage for output buffers, 1.2-V operation	—	1.14	1.2	1.26	V
$V_{CCA}^{(3)}$	Supply (analog) voltage for PLL regulator	—	2.375	2.5	2.625	V
$V_{CCD_PLL}^{(3)}$	Supply (digital) voltage for PLL, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply (digital) voltage for PLL, 1.0-V operation	—	0.97	1.0	1.03	V
V_I	Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
		For extended temperature	–40	—	125	°C
		For automotive use	–40	—	125	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) ⁽⁵⁾	50 μ s	—	50 ms	—
		Fast POR ⁽⁶⁾	50 μ s	—	3 ms	—

Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA_GXB}	Transceiver PMA and auxiliary power supply	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Transceiver PMA and auxiliary power supply	—	1.16	1.2	1.24	V
V_I	DC input voltage	—	-0.5	—	3.6	V
V_O	DC output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	-40	—	100	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) ⁽⁷⁾	50 μ s	—	50 ms	—
		Fast POR ⁽⁸⁾	50 μ s	—	3 ms	—
I_{Diode}	Magnitude of DC current across PCI-clamp diode when enabled	—	—	—	10	mA

Notes to Table 1-4:

- (1) All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (2) You must connect V_{CCD_PLL} to V_{CCINT} through a decoupling capacitor and ferrite bead.
- (3) Power supplies must rise monotonically.
- (4) V_{CCIO} for all I/O banks must be powered up during device operation. Configurations pins are powered up by V_{CCIO} of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support V_{CCIO} of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the V_{CCIO} level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.
- (5) You must set V_{CC_CLKIN} to 2.5 V if you use $CLKIN$ as a high-speed serial interface (HSSI) $refclk$ or as a $DIFFCLK$ input.
- (6) The $CLKIN$ pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.
- (7) The POR time for Standard POR ranges between 50 and 200 ms. V_{CCINT} , V_{CCA} , and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.
- (8) The POR time for Fast POR ranges between 3 and 9 ms. V_{CCINT} , V_{CCA} , and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1-5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

Table 1-5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os

Symbol	Parameter	Passing Voltage	Unit
V_{ESDHBM}	ESD voltage using the HBM (GPIOs) ⁽¹⁾	± 2000	V
	ESD using the HBM (HSSI I/Os) ⁽²⁾	± 1000	V
V_{ESDCDM}	ESD using the CDM (GPIOs)	± 500	V
	ESD using the CDM (HSSI I/Os) ⁽²⁾	± 250	V

Notes to Table 1-5:

- (1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is ± 1000 V.
- (2) This value is applicable only to Cyclone IV GX devices.

DC Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone IV devices.

Supply Current

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used. Table 1-6 lists the I/O pin leakage current for Cyclone IV devices.

Table 1-6. I/O Pin Leakage Current for Cyclone IV Devices ^{(1), (2)}

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Unit
I_I	Input pin leakage current	$V_I = 0\text{ V to }V_{CCIOMAX}$	—	-10	—	10	μA
I_{OZ}	Tristated I/O pin leakage current	$V_O = 0\text{ V to }V_{CCIOMAX}$	—	-10	—	10	μA

Notes to Table 1-6:

- (1) This value is specified for normal device operation. The value varies during device power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).
- (2) The 10 μA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

Bus Hold

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1-7 lists bus hold specifications for Cyclone IV devices.

Table 1-7. Bus Hold Parameter for Cyclone IV Devices (Part 1 of 2) ⁽¹⁾

Parameter	Condition	V _{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus hold low, sustaining current	V _{IN} > V _{IL} (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	μA
Bus hold high, sustaining current	V _{IN} < V _{IL} (minimum)	−8	—	−12	—	−30	—	−50	—	−70	—	−70	—	μA
Bus hold low, overdrive current	0 V < V _{IN} < V _{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	μA
Bus hold high, overdrive current	0 V < V _{IN} < V _{CCIO}	—	−125	—	−175	—	−200	—	−300	—	−500	—	−500	μA

Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 2 of 2) ⁽¹⁾

Parameter	Condition	V _{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Note to Table 1–7:

(1) Bus hold trip points are based on the calculated input voltages from the JEDEC standard.

OCT Specifications

Table 1–8 lists the variation of OCT without calibration across process, temperature, and voltage (PVT).

Table 1–8. Series OCT Without Calibration Specifications for Cyclone IV Devices

Description	V_{CCIO} (V)	Resistance Tolerance		Unit
		Commercial Maximum	Industrial, Extended industrial, and Automotive Maximum	
Series OCT without calibration	3.0	±30	±40	%
	2.5	±30	±40	%
	1.8	±40	±50	%
	1.5	±50	±50	%
	1.2	±50	±50	%

OCT calibration is automatically performed at device power-up for OCT-enabled I/Os.

Table 1–9 lists the OCT calibration accuracy at device power-up.

Table 1–9. Series OCT with Calibration at Device Power-Up Specifications for Cyclone IV Devices

Description	V_{CCIO} (V)	Calibration Accuracy		Unit
		Commercial Maximum	Industrial, Extended industrial, and Automotive Maximum	
Series OCT with calibration at device power-up	3.0	±10	±10	%
	2.5	±10	±10	%
	1.8	±10	±10	%
	1.5	±10	±10	%
	1.2	±10	±10	%

Example 1–1 shows how to calculate the change of 50-Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

Example 1–1. Impedance Change

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$$

$$\Delta R_T = (85 - 25) \times 0.262 = 15.72$$

Because ΔR_V is negative,

$$MF_V = 1 / (3.83/100 + 1) = 0.963$$

Because ΔR_T is positive,

$$MF_T = 15.72/100 + 1 = 1.157$$

$$MF = 0.963 \times 1.157 = 1.114$$

$$R_{\text{final}} = 50 \times 1.114 = 55.71 \, \Omega$$

Pin Capacitance

Table 1–11 lists the pin capacitance for Cyclone IV devices.

Table 1–11. Pin Capacitance for Cyclone IV Devices ⁽¹⁾

Symbol	Parameter	Typical – Quad Flat Pack (QFP)	Typical – Quad Flat No Leads (QFN)	Typical – Ball-Grid Array (BGA)	Unit
C_{IOTB}	Input capacitance on top and bottom I/O pins	7	7	6	pF
C_{IOLR}	Input capacitance on right I/O pins	7	7	5	pF
C_{LVDSLR}	Input capacitance on right I/O pins with dedicated LVDS output	8	8	7	pF
C_{VREFLR} (2)	Input capacitance on right dual-purpose V_{REF} pin when used as V_{REF} or user I/O pin	21	21	21	pF
C_{VREFTB} (2)	Input capacitance on top and bottom dual-purpose V_{REF} pin when used as V_{REF} or user I/O pin	23 (3)	23	23	pF
C_{CLKTB}	Input capacitance on top and bottom dedicated clock input pins	7	7	6	pF
C_{CLKLR}	Input capacitance on right dedicated clock input pins	6	6	5	pF

Notes to Table 1–11:

- (1) The pin capacitance applies to FBGA, UBGA, and MBGA packages.
- (2) When you use the V_{REF} pin as a regular input or output, you can expect a reduced performance of toggle rate and t_{CO} because of higher pin capacitance.
- (3) C_{VREFTB} for the EP4CE22 device is 30 pF.

Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 1-12 lists the weak pull-up and pull-down resistor values for Cyclone IV devices.

Table 1-12. Internal Weak Pull-Up and Weak Pull-Down Resistor Values for Cyclone IV Devices ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option	V _{CCIO} = 3.3 V ± 5% ^{(2), (3)}	7	25	41	kΩ
		V _{CCIO} = 3.0 V ± 5% ^{(2), (3)}	7	28	47	kΩ
		V _{CCIO} = 2.5 V ± 5% ^{(2), (3)}	8	35	61	kΩ
		V _{CCIO} = 1.8 V ± 5% ^{(2), (3)}	10	57	108	kΩ
		V _{CCIO} = 1.5 V ± 5% ^{(2), (3)}	13	82	163	kΩ
		V _{CCIO} = 1.2 V ± 5% ^{(2), (3)}	19	143	351	kΩ
R _{PD}	Value of the I/O pin pull-down resistor before and during configuration	V _{CCIO} = 3.3 V ± 5% ⁽⁴⁾	6	19	30	kΩ
		V _{CCIO} = 3.0 V ± 5% ⁽⁴⁾	6	22	36	kΩ
		V _{CCIO} = 2.5 V ± 5% ⁽⁴⁾	6	25	43	kΩ
		V _{CCIO} = 1.8 V ± 5% ⁽⁴⁾	7	35	71	kΩ
		V _{CCIO} = 1.5 V ± 5% ⁽⁴⁾	8	50	112	kΩ

Notes to Table 1-12:

- (1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.
- (2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (3) $R_{PU} = (V_{CCIO} - V_I) / I_{R_{PU}}$
Minimum condition: -40°C; V_{CCIO} = V_{CC} + 5%, V_I = V_{CC} + 5% - 50 mV;
Typical condition: 25°C; V_{CCIO} = V_{CC}, V_I = 0 V;
Maximum condition: 100°C; V_{CCIO} = V_{CC} - 5%, V_I = 0 V; in which V_I refers to the input voltage at the I/O pin.
- (4) $R_{PD} = V_I / I_{R_{PD}}$
Minimum condition: -40°C; V_{CCIO} = V_{CC} + 5%, V_I = 50 mV;
Typical condition: 25°C; V_{CCIO} = V_{CC}, V_I = V_{CC} - 5%;
Maximum condition: 100°C; V_{CCIO} = V_{CC} - 5%, V_I = V_{CC} - 5%; in which V_I refers to the input voltage at the I/O pin.

Hot-Socketing

Table 1-13 lists the hot-socketing specifications for Cyclone IV devices.

Table 1-13. Hot-Socketing Specifications for Cyclone IV Devices

Symbol	Parameter	Maximum
I _{IOPIN(DC)}	DC current per I/O pin	300 μA
I _{IOPIN(AC)}	AC current per I/O pin	8 mA ⁽¹⁾
I _{XCVRTX(DC)}	DC current per transceiver TX pin	100 mA
I _{XCVRRX(DC)}	DC current per transceiver RX pin	50 mA

Note to Table 1-13:

- (1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |I_{IOPIN}| = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.



During hot-socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

Table 1-16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone IV Devices ⁽¹⁾

I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V) ⁽²⁾		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 x V _{CCIO} ⁽³⁾	0.5 x V _{CCIO} ⁽³⁾	0.52 x V _{CCIO} ⁽³⁾	—	0.5 x V _{CCIO}	—
				0.47 x V _{CCIO} ⁽⁴⁾	0.5 x V _{CCIO} ⁽⁴⁾	0.53 x V _{CCIO} ⁽⁴⁾			

Notes to Table 1-16:

- (1) For an explanation of terms used in Table 1-16, refer to “Glossary” on page 1-37.
- (2) V_{TT} of the transmitting device must track V_{REF} of the receiving device.
- (3) Value shown refers to DC input reference voltage, V_{REF(DC)}.
- (4) Value shown refers to AC input reference voltage, V_{REF(AC)}.

Table 1-17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone IV Devices

I/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)		V _{IH(AC)} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} (mA)	I _{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V _{REF} - 0.18	V _{REF} + 0.18	—	—	V _{REF} - 0.35	V _{REF} + 0.35	—	V _{TT} - 0.57	V _{TT} + 0.57	8.1	-8.1
SSTL-2 Class II	—	V _{REF} - 0.18	V _{REF} + 0.18	—	—	V _{REF} - 0.35	V _{REF} + 0.35	—	V _{TT} - 0.76	V _{TT} + 0.76	16.4	-16.4
SSTL-18 Class I	—	V _{REF} - 0.125	V _{REF} + 0.125	—	—	V _{REF} - 0.25	V _{REF} + 0.25	—	V _{TT} - 0.475	V _{TT} + 0.475	6.7	-6.7
SSTL-18 Class II	—	V _{REF} - 0.125	V _{REF} + 0.125	—	—	V _{REF} - 0.25	V _{REF} + 0.25	—	0.28	V _{CCIO} - 0.28	13.4	-13.4
HSTL-18 Class I	—	V _{REF} - 0.1	V _{REF} + 0.1	—	—	V _{REF} - 0.2	V _{REF} + 0.2	—	0.4	V _{CCIO} - 0.4	8	-8
HSTL-18 Class II	—	V _{REF} - 0.1	V _{REF} + 0.1	—	—	V _{REF} - 0.2	V _{REF} + 0.2	—	0.4	V _{CCIO} - 0.4	16	-16
HSTL-15 Class I	—	V _{REF} - 0.1	V _{REF} + 0.1	—	—	V _{REF} - 0.2	V _{REF} + 0.2	—	0.4	V _{CCIO} - 0.4	8	-8
HSTL-15 Class II	—	V _{REF} - 0.1	V _{REF} + 0.1	—	—	V _{REF} - 0.2	V _{REF} + 0.2	—	0.4	V _{CCIO} - 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	-0.24	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.24	0.25 x V _{CCIO}	0.75 x V _{CCIO}	8	-8
HSTL-12 Class II	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	-0.24	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.24	0.25 x V _{CCIO}	0.75 x V _{CCIO}	14	-14

Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices ⁽¹⁾ (Part 2 of 2)

I/O Standard	V _{CCIO} (V)			V _{ID} (mV)		V _{ICM} (V) ⁽²⁾			V _{OD} (mV) ⁽³⁾			V _{OS} (V) ⁽³⁾		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (Column I/Os)	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq 500 \text{ Mbps}$	1.80	247	—	600	1.125	1.25	1.375
						0.55	$500 \text{ Mbps} \leq D_{MAX} \leq 700 \text{ Mbps}$	1.80						
						1.05	$D_{MAX} > 700 \text{ Mbps}$	1.55						
BLVDS (Row I/Os) ⁽⁴⁾	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
BLVDS (Column I/Os) ⁽⁴⁾	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
mini-LVDS (Row I/Os) ⁽⁵⁾	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1.0	1.2	1.4
mini-LVDS (Column I/Os) ⁽⁵⁾	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1.0	1.2	1.4
RSDS [®] (Row I/Os) ⁽⁵⁾	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
RSDS (Column I/Os) ⁽⁵⁾	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS (Row I/Os) ⁽⁵⁾	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4
PPDS (Column I/Os) ⁽⁵⁾	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4

Notes to Table 1–20:

- (1) For an explanation of terms used in Table 1–20, refer to “Glossary” on page 1–37.
- (2) V_{IN} range: $0 \text{ V} \leq V_{IN} \leq 1.85 \text{ V}$.
- (3) R_L range: $90 \leq R_L \leq 110 \Omega$.
- (4) There are no fixed V_{IN}, V_{OD}, and V_{OS} specifications for BLVDS. They depend on the system topology.
- (5) The Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins.
- (6) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported for output pins.

Transceiver Performance Specifications

Table 1-21 lists the Cyclone IV GX transceiver specifications.

Table 1-21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2 V PCML, 1.5 V PCML, 3.3 V PCML, Differential LVPECL, LVDS, HCSL										
Input frequency from REFCLK input pins	—	50	—	156.25	50	—	156.25	50	—	156.25	MHz
Spread-spectrum modulating clock frequency	Physical interface for PCI Express (PIPE) mode	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PIPE mode	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
Peak-to-peak differential input voltage	—	0.1	—	1.6	0.1	—	1.6	0.1	—	1.6	V
V _{ICM} (AC coupled)	—	1100 ± 5%			1100 ± 5%			1100 ± 5%			mV
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise ⁽¹⁾	Frequency offset = 1 MHz – 8 MHz	—	—	–123	—	—	–123	—	—	–123	dBc/Hz
Transmitter REFCLK Total Jitter ⁽¹⁾		—	—	42.3	—	—	42.3	—	—	42.3	ps
R _{ref}	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clock											
cal_blk_clk clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/37.5 ⁽²⁾	—	50	2.5/37.5 ⁽²⁾	—	50	2.5/37.5 ⁽²⁾	—	50	MHz
Delta time between reconfig_clk	—	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down pulse width	—	—	1	—	—	1	—	—	1	—	μs

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 2 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (F324 and smaller package) ⁽¹⁵⁾	—	600	—	2500	600	—	2500	600	—	2500	Mbps
Data rate (F484 and larger package) ⁽¹⁵⁾	—	600	—	3125	600	—	3125	600	—	2500	Mbps
Absolute V _{MAX} for a receiver pin ⁽³⁾	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V _{MAX} for a receiver pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V _{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Peak-to-peak differential input voltage V _{ID} (diff p-p)	V _{ICM} = 0.82 V setting, Data Rate = 600 Mbps to 3.125 Gbps	0.1	—	2.7	0.1	—	2.7	0.1	—	2.7	V
V _{ICM}	V _{ICM} = 0.82 V setting	—	820 ± 10%	—	—	820 ± 10%	—	—	820 ± 10%	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
	150–Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PIPE, Serial Rapid I/O SR, SATA, CPRI LV, SDI, XAUI	Compliant									—
Programmable ppm detector ⁽⁴⁾	—	± 62.5, 100, 125, 200, 250, 300									ppm
Clock data recovery (CDR) ppm tolerance (without spread-spectrum clocking enabled)	—	—	—	±300 ⁽⁵⁾ , ±350 ^{(6), (7)}	—	—	±300 ⁽⁵⁾ , ±350 ^{(6), (7)}	—	—	±300 ⁽⁵⁾ , ±350 ^{(6), (7)}	ppm
CDR ppm tolerance (with synchronous spread-spectrum clocking enabled) ⁽⁸⁾	—	—	—	350 to –5350 ^{(7), (9)}	—	—	350 to –5350 ^{(7), (9)}	—	—	350 to –5350 ^{(7), (9)}	ppm
Run length	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	No Equalization	—	—	1.5	—	—	1.5	—	—	1.5	dB
	Medium Low	—	—	4.5	—	—	4.5	—	—	4.5	dB
	Medium High	—	—	5.5	—	—	5.5	—	—	5.5	dB
	High	—	—	7	—	—	7	—	—	7	dB

Table 1–24. Clock Tree Performance for Cyclone IV Devices (Part 2 of 2)

Device	Performance								Unit
	C6	C7	C8	C8L ⁽¹⁾	C9L ⁽¹⁾	I7	I8L ⁽¹⁾	A7	
EP4CE55	500	437.5	402	362	265	437.5	362	—	MHz
EP4CE75	500	437.5	402	362	265	437.5	362	—	MHz
EP4CE115	—	437.5	402	362	265	437.5	362	—	MHz
EP4CGX15	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX22	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX30	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX50	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX75	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX110	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX150	500	437.5	402	—	—	437.5	—	—	MHz

Note to Table 1–24:

(1) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades.

PLL Specifications

Table 1–25 lists the PLL specifications for Cyclone IV devices when operating in the commercial junction temperature range (0°C to 85°C), the industrial junction temperature range (–40°C to 100°C), the extended industrial junction temperature range (–40°C to 125°C), and the automotive junction temperature range (–40°C to 125°C). For more information about the PLL block, refer to “Glossary” on page 1–37.

Table 1–25. PLL Specifications for Cyclone IV Devices ^{(1), (2)} (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN} ⁽³⁾	Input clock frequency (–6, –7, –8 speed grades)	5	—	472.5	MHz
	Input clock frequency (–8L speed grade)	5	—	362	MHz
	Input clock frequency (–9L speed grade)	5	—	265	MHz
f_{INPFD}	PFD input frequency	5	—	325	MHz
f_{VCO} ⁽⁴⁾	PLL internal VCO operating range	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER_CCJ}$ ⁽⁵⁾	Input clock cycle-to-cycle jitter $F_{REF} \geq 100$ MHz	—	—	0.15	UI
	$F_{REF} < 100$ MHz	—	—	±750	ps
f_{OUT_EXT} (external clock output) ⁽³⁾	PLL output frequency	—	—	472.5	MHz
f_{OUT} (to global clock)	PLL output frequency (–6 speed grade)	—	—	472.5	MHz
	PLL output frequency (–7 speed grade)	—	—	450	MHz
	PLL output frequency (–8 speed grade)	—	—	402.5	MHz
	PLL output frequency (–8L speed grade)	—	—	362	MHz
	PLL output frequency (–9L speed grade)	—	—	265	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	1	ms

Table 1–25. PLL Specifications for Cyclone IV Devices ^{(1), (2)} (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or $\overline{areset}$ is deasserted)	—	—	1	ms
$t_{OUTJITTER_PERIOD_DEDCLK}$ ⁽⁶⁾	Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER_CCJ_DEDCLK}$ ⁽⁶⁾	Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER_PERIOD_IO}$ ⁽⁶⁾	Regular I/O period jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER_CCJ_IO}$ ⁽⁶⁾	Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	± 50	ps
t_{ARESET}	Minimum pulse width on $\overline{areset}$ signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 ⁽⁷⁾	—	SCANCLK cycles
$f_{SCANCLK}$	$scanclk$ frequency	—	—	100	MHz
$t_{CASC_OUTJITTER_PERIOD_DEDCLK}$ ^{(8), (9)}	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	425	ps
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz)	—	—	42.5	mUI

Notes to Table 1–25:

- (1) This table is applicable for general purpose PLLs and multipurpose PLLs.
- (2) You must connect V_{CCD_PLL} to V_{CCINT} through the decoupling capacitor and ferrite bead.
- (3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (4) The V_{CO} frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the V_{CO} post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.
- (6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.
- (7) With 100-MHz $scanclk$ frequency.
- (8) The cascaded PLLs specification is applicable only with the following conditions:
 - Upstream PLL— $0.59 \text{ MHz} \leq \text{Upstream PLL bandwidth} < 1 \text{ MHz}$
 - Downstream PLL—Downstream PLL bandwidth $> 2 \text{ MHz}$
- (9) PLL cascading is not supported for transceiver applications.

Table 1–29 lists the active configuration mode specifications for Cyclone IV devices.

Table 1–29. Active Configuration Mode Specifications for Cyclone IV Devices

Programming Mode	DCLK Range	Typical DCLK	Unit
Active Parallel (AP) ⁽¹⁾	20 to 40	33	MHz
Active Serial (AS)	20 to 40	33	MHz

Note to Table 1–29:

(1) AP configuration mode is only supported for Cyclone IV E devices.

Table 1–30 lists the JTAG timing parameters and values for Cyclone IV devices.

Table 1–30. JTAG Timing Parameters for Cyclone IV Devices ⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t _{JCP}	TCK clock period	40	—	ns
t _{JCH}	TCK clock high time	19	—	ns
t _{JCL}	TCK clock low time	19	—	ns
t _{JPSU_TDI}	JTAG port setup time for TDI	1	—	ns
t _{JPSU_TMS}	JTAG port setup time for TMS	3	—	ns
t _{JPH}	JTAG port hold time	10	—	ns
t _{JPCO}	JTAG port clock to output ^{(2), (3)}	—	15	ns
t _{JPZX}	JTAG port high impedance to valid output ^{(2), (3)}	—	15	ns
t _{JPXZ}	JTAG port valid output to high impedance ^{(2), (3)}	—	15	ns
t _{JSSU}	Capture register setup time	5	—	ns
t _{JSH}	Capture register hold time	10	—	ns
t _{JSCO}	Update register clock to output	—	25	ns
t _{JSZX}	Update register high impedance to valid output	—	25	ns
t _{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 1–30:

(1) For more information about JTAG waveforms, refer to “JTAG Waveform” in “Glossary” on page 1–37.

(2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.

(3) For EP4CGX22, EP4CGX30 (F324 and smaller package), EP4CGX110, and EP4CGX150 devices, the output time specification for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins is 16 ns. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 18 ns.

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/Os using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-V LVTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.

Table 1-31. RSDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (2), (4)} (Part 2 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{LOCK} ⁽³⁾	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1-31:

- (1) Applicable for true RSDS and emulated RSDS_E_3R transmitter.
- (2) Cyclone IV E devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated RSDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (3) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1-32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 1 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK} (input clock frequency)	×10	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×8	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×7	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×4	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×2	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×1	5	—	170	5	—	170	5	—	170	5	—	170	5	—	145	MHz
Device operation in Mbps	×10	100	—	170	100	—	170	100	—	170	100	—	170	100	—	145	Mbps
	×8	80	—	170	80	—	170	80	—	170	80	—	170	80	—	145	Mbps
	×7	70	—	170	70	—	170	70	—	170	70	—	170	70	—	145	Mbps
	×4	40	—	170	40	—	170	40	—	170	40	—	170	40	—	145	Mbps
	×2	20	—	170	20	—	170	20	—	170	20	—	170	20	—	145	Mbps
	×1	10	—	170	10	—	170	10	—	170	10	—	170	10	—	145	Mbps
t _{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
t _{RISE}	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps

Table 1–34. True LVDS Transmitter Timing Specifications for Cyclone IV Devices ⁽¹⁾, ⁽³⁾

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{HCLK} (input clock frequency)	×10	5	420	5	370	5	320	5	320	5	250	MHz
	×8	5	420	5	370	5	320	5	320	5	250	MHz
	×7	5	420	5	370	5	320	5	320	5	250	MHz
	×4	5	420	5	370	5	320	5	320	5	250	MHz
	×2	5	420	5	370	5	320	5	320	5	250	MHz
	×1	5	420	5	402.5	5	402.5	5	362	5	265	MHz
HSIODR	×10	100	840	100	740	100	640	100	640	100	500	Mbps
	×8	80	840	80	740	80	640	80	640	80	500	Mbps
	×7	70	840	70	740	70	640	70	640	70	500	Mbps
	×4	40	840	40	740	40	640	40	640	40	500	Mbps
	×2	20	840	20	740	20	640	20	640	20	500	Mbps
	×1	10	420	10	402.5	10	402.5	10	362	10	265	Mbps
t_{DUTY}	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	—	700	ps
t_{LOCK} ⁽²⁾	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1–34:

- (1) Cyclone IV E—true LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6.
Cyclone IV GX—true LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices ⁽¹⁾, ⁽³⁾ (Part 1 of 2)

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{HCLK} (input clock frequency)	×10	5	320	5	320	5	275	5	275	5	250	MHz
	×8	5	320	5	320	5	275	5	275	5	250	MHz
	×7	5	320	5	320	5	275	5	275	5	250	MHz
	×4	5	320	5	320	5	275	5	275	5	250	MHz
	×2	5	320	5	320	5	275	5	275	5	250	MHz
	×1	5	402.5	5	402.5	5	402.5	5	362	5	265	MHz
HSIODR	×10	100	640	100	640	100	550	100	550	100	500	Mbps
	×8	80	640	80	640	80	550	80	550	80	500	Mbps
	×7	70	640	70	640	70	550	70	550	70	500	Mbps
	×4	40	640	40	640	40	550	40	550	40	500	Mbps
	×2	20	640	20	640	20	550	20	550	20	500	Mbps
	×1	10	402.5	10	402.5	10	402.5	10	362	10	265	Mbps

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 2 of 2)

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{DUTY}	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	—	700	ps
t _{LOCK} ⁽²⁾	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1–35:

- (1) Cyclone IV E—emulated LVDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX—emulated LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–36. LVDS Receiver Timing Specifications for Cyclone IV Devices ^{(1), (3)}

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f _{HCLK} (input clock frequency)	×10	10	437.5	10	370	10	320	10	320	10	250	MHz
	×8	10	437.5	10	370	10	320	10	320	10	250	MHz
	×7	10	437.5	10	370	10	320	10	320	10	250	MHz
	×4	10	437.5	10	370	10	320	10	320	10	250	MHz
	×2	10	437.5	10	370	10	320	10	320	10	250	MHz
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	MHz
HSIODR	×10	100	875	100	740	100	640	100	640	100	500	Mbps
	×8	80	875	80	740	80	640	80	640	80	500	Mbps
	×7	70	875	70	740	70	640	70	640	70	500	Mbps
	×4	40	875	40	740	40	640	40	640	40	500	Mbps
	×2	20	875	20	740	20	640	20	640	20	500	Mbps
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	Mbps
SW	—	—	400	—	400	—	400	—	550	—	640	ps
Input jitter tolerance	—	—	500	—	500	—	550	—	600	—	700	ps
t _{LOCK} ⁽²⁾	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1–36:

- (1) Cyclone IV E—LVDS receiver is supported at all I/O Banks.
Cyclone IV GX—LVDS receiver is supported at I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

External Memory Interface Specifications

The external memory interfaces for Cyclone IV devices are auto-calibrating and easy to implement.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices ^{(1), (2)}

Parameter	Paths Affected	Number of Settings	Min Offset	Max Offset						Unit
				Fast Corner		Slow Corner				
				C6	I7	C6	C7	C8	I7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.313	1.209	2.184	2.336	2.451	2.387	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.208	2.200	2.399	2.554	2.446	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.438	0.404	0.751	0.825	0.886	0.839	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.713	0.682	1.228	1.41	1.566	1.424	ns

Notes to Table 1–44:

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices ^{(1), (2)}

Parameter	Paths Affected	Number of Settings	Min Offset	Max Offset						Unit
				Fast Corner		Slow Corner				
				C6	I7	C6	C7	C8	I7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.210	2.209	2.398	2.526	2.443	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.313	1.208	2.205	2.406	2.563	2.450	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.461	0.421	0.789	0.869	0.933	0.884	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.712	0.682	1.225	1.407	1.562	1.421	ns

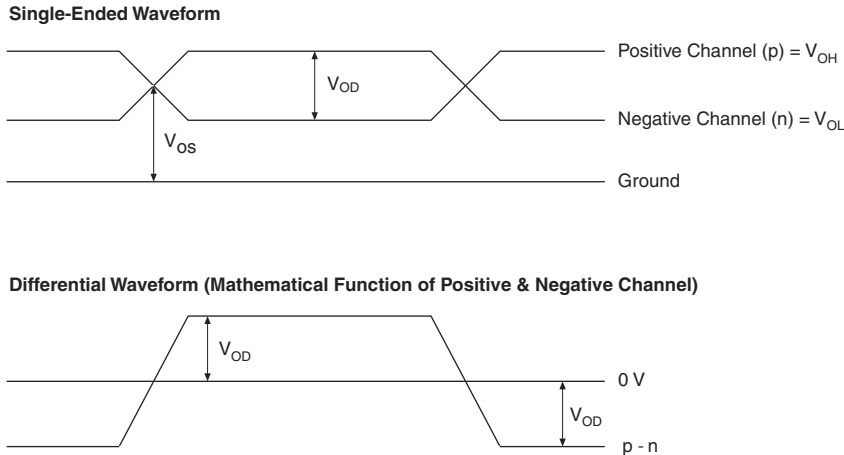
Notes to Table 1–45:

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software

Table 1-46. Glossary (Part 2 of 5)

Letter	Term	Definitions
J	JTAG Waveform	The diagram illustrates the JTAG waveform with the following timing parameters: t_{JCP}: Time from TCK rising edge to TDI setup. t_{JCH}: Time from TCK falling edge to TDI hold. t_{JCL}: Time from TCK rising edge to TDI latch. t_{JPSU_TDI}: Setup time for TDI before TCK rising edge. t_{JPSU_TMS}: Setup time for TMS before TCK rising edge. t_{JPH}: Hold time for TMS after TCK rising edge. t_{JPZX}: Time from TCK rising edge to TDO setup. t_{JPCO}: Time from TCK falling edge to TDO hold. t_{JPXZ}: Time from TCK falling edge to TDO latch. t_{JSSU}: Setup time for Signal to be Captured before TCK rising edge. t_{JSH}: Hold time for Signal to be Captured after TCK rising edge. t_{JSZX}: Time from TCK rising edge to Signal to be Driven setup. t_{JSCO}: Time from TCK falling edge to Signal to be Driven hold. t_{JSXZ}: Time from TCK falling edge to Signal to be Driven latch.
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Block	The following highlights the PLL specification parameters: The diagram shows the internal structure of the PLL block: Inputs: CLK (Core Clock), Core Clock. Internal Blocks: Switchover, PFD (Phase-Frequency Divider), CP (Charge Pump), LF (Loop Filter), VCO (Voltage-Controlled Oscillator), Counters C0..C4, and a Phase tap. Outputs: CLKOUT Pins (f_{OUT_EXT}), f_{OUT}, and GCLK. Parameters: f_{IN}, N, f_{INPFD}, f_{VCO}. Key: - Reconfigurable in User Mode
Q	—	—

Table 1-46. Glossary (Part 4 of 5)

Letter	Term	Definitions
T	t_C	High-speed receiver and transmitter input and output clock period.
	Channel-to-channel-skew (TCCS)	High-speed I/O block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
	t_{cin}	Delay from the clock pad to the I/O input register.
	t_{CO}	Delay from the clock pad to the I/O output.
	t_{cout}	Delay from the clock pad to the I/O output register.
	t_{DUTY}	High-speed I/O block: Duty cycle on high-speed transmitter output clock.
	t_{FALL}	Signal high-to-low transition time (80–20%).
	t_H	Input register hold time.
	Timing Unit Interval (TUI)	High-speed I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_C/w$).
	$t_{INJITTER}$	Period jitter on the PLL clock input.
	$t_{OUTJITTER_DEDCLK}$	Period jitter on the dedicated clock output driven by a PLL.
	$t_{OUTJITTER_IO}$	Period jitter on the general purpose I/O driven by a PLL.
	t_{pllcin}	Delay from the PLL inclk pad to the I/O input register.
	$t_{pllcout}$	Delay from the PLL inclk pad to the I/O output register.
	Transmitter Output Waveform	Transmitter output waveforms for the LVDS, mini-LVDS, PPDS and RSDS Differential I/O Standards: 
	t_{RISE}	Signal low-to-high transition time (20–80%).
	t_{SU}	Input register setup time.
U	—	—